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The current state of the art of space flight computing for deep space missions such as the Cassini mission to Saturn, involves the use of electronics subsystems that weigh over 50 kg (with structure support and cabling) and consumes over 50 watts of total peak power. Given that the Cassini spacecraft weighs 2150 kg (dry mass), consumes 750 Watts, and has a total volume of $88 m^3$ this proportion does not sound alarming. However, the recent US economic reality favors the design of smaller, less expensive and more frequent missions, as opposed to fewer missions that cost over a billion dollars. Therefore, NASA has recently initiated a series of small spacecraft studies and flight projects such as the Mars Environmental Study (MESUR) which will include a microrover; the Pluto Flyby mission; Asteroid Flybys, etc. The microrover electronics (analog and digital), for example, has a budget constraint of only 1.5 watts, and a mass constraint of 0.5 kg. The total mass of the microrover is 7 kg.

To meet these new design objectives for drastic reductions in mass, size, and power consumption, the Flight Computer Development Group at JPL is participating in a design study and development of a light-weight, small sized, low-power 3-1) Space Flight Computer. To identify the key computer technologies that would drive the design of this next-generation flight computer, a workshop was held on December 2nd at the University of Illinois to address this issue. The following 6 technologies were identified.

- Advanced Packaging architectures

- Low power electronics (CMOS)
- Standardization
- Commercialization
- Fault,-tolerant hardware and software architectures
- Real-time operating system

In this paper, we will present a detailed design and tradeoff study of the 3-1) flight, Computer proposed by the Flight Computer Development Group at JPL. It is characterized by the following attributes.

The complete flight computer that includes a commercially available processor such as the RAD6000 or the 1{113000; memory; I/O and a solid state recorder, will be packaged within the volume of 9 cu^3 ($3 \times 3 \times 1$) using a technique that stacks up to 12 Multi-Chip-Modules into a *stack of pancake* configuration. Dense 3D memory chip stacking is used for main memory and the solid state recorder. A standard format is selected for the MCM size which is compatible with on-going industry standards such as ISHM and IJ 'C. The MCM modules are interchangeable and any processor can be stacked within the computer as long as it complies with the format. The processor architecture is based on the IEEE 896.10 FutureBus+Space Standard which is vertically implemented between the MCMs. A real-time operating system such as VRTX, VxWorks, or Spectra is used, and fault-tolerant services (both hardware and software) are implemented on-top of the commercially available real-time system.

In this paper we will present a complete design of the MCMs, their size, weight and power consumption. Preliminary thermal models will also be discussed.