TOTAL IONIZING DOSE EFFECTS
IN 12-BIT SUCCESSIVE-APPROXIMATION ANALOG-TO-DIGITAL CONVERTERS*

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1. INTRODUCTION

Analog-to-digital (A/D) converters are critical components in many space and military systems, and there have been numerous advances in A/D converter technology that have increased the resolution and conversion time. The increased performance is due to two factors: (1) advances in circuit design and complexity, which have increased the number of components and the integration density; and (2) new process technologies, such as BiCMOS, which provide better performance, cost, and smaller size in mixed-signal circuits.

High-speed A/D converters, with conversion rates above 1 MHz, present a challenge to circuit designers and test engineers. Their complex architectures and high-performance specifications result in numerous possible failure modes when they are subjected to ionizing radiation. The dominant failure mode may depend on the specific application because the fundamental effects on MOS and bipolar transistors are strongly affected by bias conditions. This paper identifies the most critical parameters for two different processing technologies, and relates their failure modes to internal design.

2. DEVICE DESCRIPTION

Successive-approximation (SA) A/D converters are widely used in data acquisition applications because of their high resolution (up to 12-/l 6-bits) and high speed. A successive-approximation A/D converter contains several complex subfunctions, The most critical analog component is a high-resolution comparator, which must resolve input voltages of a few mV for a 12-bit converter. There is also an internal high-speed digital-to-analog (D/A) converter, which basically functions as a digitally selected precision voltage source. The inputs of the internal D/A converters are digital numbers at the outputs of the A/D converter. Most converters contain tri-state data outputs and byte controls to facilitate interfacing with microprocessors. Digitat subfunctions include a successive approximaion register (SAR), and control and timing logic. Some of the circuits use monolithic design (BiCMOS), while one uses a two-chip (LSI) hybrid approach that allows bipolar technology to be used for the analog section and digital subfunctions. A block diagram of a SA A/D converter is shown in Figure 1. The bold outlines show functions that require high analog precision. In addition to the analog requirements, they must also withstand higher voltage than the digital functions.

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The A/D converter accuracy, nonlinearity, and speed are primarily affected by the properties of the internal precision D/A converter, the reference, and the comparator. The settling time of the internal D/A converter and the response time of the internal comparator are considerably slower than the switching time of the digital circuitry. The integral and differential nonlinearities (INL/DNL) of the internal D/A converter will be directly reflected in the INL/DNL of the A/D converter. If the output of the internal D/A converter is non-monotonic, then one or more codes will be missing from the A/D converter's output range.

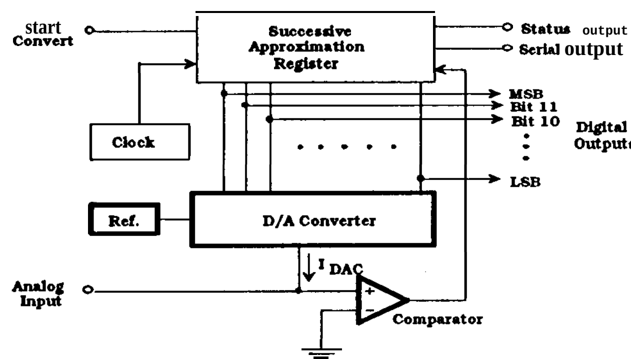

Figure 1. Block Diagram of SA A/D converter

3. TOTAL IONIZING DOSE (TID) TEST

L TID TEST SAMPLES

The converters that were tested used two basic processes. (1) The bipolar process which is used in classical linear devices such as operationat amplifiers and voltage regulators. This provides good analog accuracy, high speed, low noise, and high breakdown voltages. The disadvantages are poor logic capability, large size, and higher power requirements, (2) BiCMOS combines bipolar and CMOS technologies on one chip. It allows selective use of bipolar devices to improve artatog performance. This process is used most widely for present commercial A/D converters because it combines precision, low-noise, and high-speed bipolar circuitry with low power, high speed, and high-density CMOS logic.

A/D converters have a much higher voltage rating (~20V) compared to normal logic circuits. This requires that converter CMOS processes use lower doping levels and thicker gate oxides than digitat processes, which increases their sensitivity to ionizing radiation. This will be discussed further below.

The basic features of the 12-bit successive approximation A/D converters that were tested aresummarizedin Table 1. The Analog Devices AD674A contains two bipolar LSI chips in one hybrid packgage. Analog circuitry is processed with Flash

Table 1. 12-Bit Successive Approximation A/B converters

Type	Manufacturer	Process	Integration Level	Tgate ox (Å)	Tfield ox (Å)
AD674A	ADI	Bipolar Ii-Digital	Two Chips	NA	12600
		Bipolar (Flash)-Analog		NA	6000
AD674B	AD1	BiMOS	Single Chip	750	16500
M-X7672	Maxim	BiCMOS	Single Chip	900	11500
MX674A	Maxim	BiCMOS	Single Chip	900	11500

bipolar technology while digital circuitry is processed with Bipolar II technology, resulting in maximum performance and flexibility.

The Maxim converters, MX7672, attd MX674A are fabricated with BiCMOS processes. The Analog Devices AD674B design is also implemented using a BiMOS process (same as BiCMOS process). The BiCMOS process consists of precision bipolar components with low-power, high-speed CMOS logic. Their design is implemented with a single LSI chip containing both analog and digital circuitry.

11. TID TEST CONDITIONS

Initial radiation testing was performed using a Shepherd ^{60}Co room type irradiator with a source strength of 10 kCuries at a dose rate of 100 rad(Si)/sec. Later tests were done with some of the devices at dose rates as low as 0.1 rad(Si)/sec. All devices were irradiated and tested at room temperature.

Devices were tested with two different bias conditions: (1) dynamic, clocking the devices at high speed and performing conversions at a frequency of 6.4 kHz; and (2) static, which initialized the device to a known state, but did not allow it to perform active conversions during the irradiation. The tri-state outputs were tied to Vcc through a 10 k resistor to simulate a bus application. For the static bias case, some outputs remained in preinitialized logic states during the entire radiation cycle, whereas all of the outputs switched state periodically when the devices were tested in the dynamic case. Thus, conditions of the output circuitry were markedly different for the two bias conditions.

There were atso significant differences in the conditions of the internal circuitry. With static bias, the comparator was overdriven (saturated) throughout the irradiation, and some of the DAC bits remained in fixed states. With dynamic bias, the comparator was operating near the linear region, reducing the voltage across the collector-base junction compared to the static case. In addition, all of the DAC bits switched state periodically. As will be discussed later, the bias conditions had a strong effect on the total dose sensitivity. For parametric failure, static bias was the most sensitive mode for all of the technologies.

III. TID TEST RESULTS

There were large differences in the failure modes and total dose levels of the converters in this study. Some of the BiCMOS devices failed at levels as low as 6 krad(Si) under static bias at high dose rates, whereas the bipolar part was operational at levels above 100 krad(Si) under same bias conditions, There were also large differences in time-dependent effects between different devices. The failure modes and characteristics of the different technologies are discussed in more detail below. The TID test results are summarized in Table 2.

Table 2. Summary of Total Dose Test Results

Part Type	LDC	Dose Rate (rad(Si)/s)	Bias Condition	Parametric Failure Level (krad(Si))	Functional Failure Level (krad(Si))
MX7672	9241	0.1	Static	11	>27
		0.1	Dynamic	>27	>27
		100	Static	6	20
MX674A	9117	0,1	Static	>27	>27
		0.1	Dynamic	>27	>27
		100	Static	8	20
AD674A	8914	100	Static	8	>140
		100	Dynamic	50	>100
AD674B	9213	100	Static	10	12
		100	Dynamic	12	14

i. Bipolar Circuits

In general, the two-chip bipolar hybrid (AD 674A) exhibited the best radiation performance. Although small parametric changes were observed at about 8 krad(Si), the circuits remained functional up to the finat level of 140 krad(Si) during static mode bias condition. The dynamically biased devices showed parametric failures at 50 krad(Si) and remained functional up to the maximum test dose of 100 krad(Si).

All of the parameters specified for this device were measured, and most changed very little during irradiation until levels above 100 krad(Si). The most sensitive parameter was the integral nonlinearity (INL). INL is one of the most important A/D converter specifications. The INL of A/D converters is the deviation of the transfer function from the ideal straight line [1]. It describes how close the transition voltage endpoints are to a straight line drawn through them. These 12-bit converters guarantee ±1/2 least significant bit (LSB) linearity over whatever temperature range they are specified for.

The changes in INL with total ionizing dose irradiation for AD674A are shown in Figure 2. Surprisingly, this complex parameter changed in a smooth, regular way with radiation under static bias. Other parameters, differential nonlinearity (DNL) and bipolar offset, exhibited similar responses during irradiation under static bias.

From the basic functional block diagram of the converter and the marked difference in response under different bias conditions, the failure mode appears to be caused by gain degradation of transistors and/or leakages in the current switches in the internal D/A converter. Additional work will be performed using localized irradiation with a scanning electron microscope (SEM) [2] to determine the exact failure mode. These results will be included in the final paper.

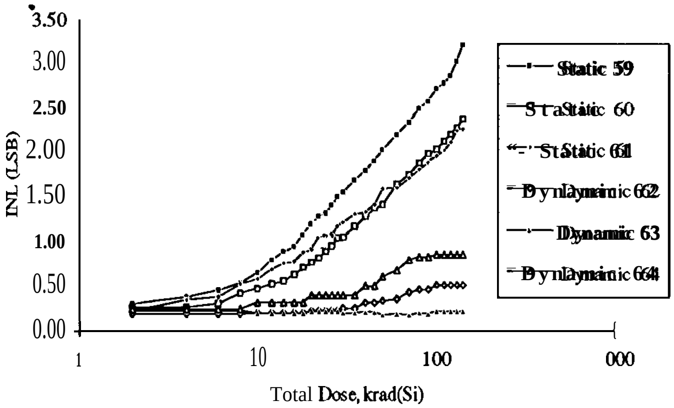

Figure 2. AD674A INL vs. Total Dose

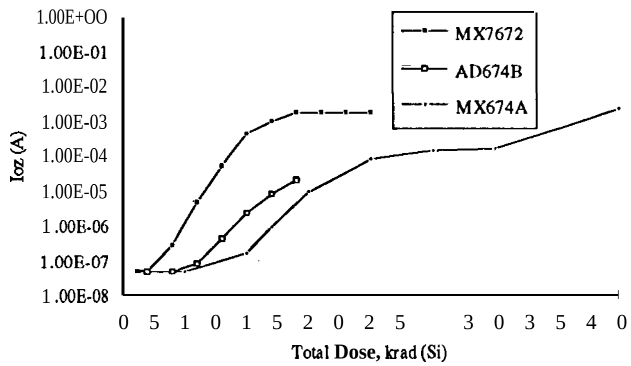

Figure 3. Radiation Induced Ioz in Static Biased BiCMOS Devices

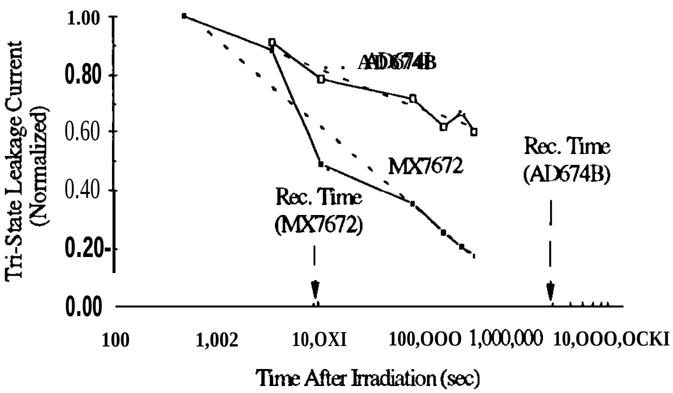

Figure 4. Recovery Time of A/D Converters

ii. BiCMOS Circuits

FortheBiCMOS circuits, all of thecomplexparameters that 'are directly involved in converter accuracy remained well within tolerance until the irradiation level was close to the level for total functional failure. The dominant failure mode was increase in the tri-state leakage current, Ioz, as shown in Figure 3 for statically biased devices. Ioz exceeded its specification limit (10 uA) at about 6 krad(Si) for the most sensitive process. This was only observed for the static bias condition, This result is rather surprising. It shows that the bipolar devices in the BiCMOS circuits are sufficiently tolerant to total dose so that all of the complex analog functions operate normally within the high tolerance limits required by these devices. The digital output stages are much more susceptible to radiation and the failure mode is similar to that of basic CMOS logic circuits,

Although large changes occurred in the Ioz parameter, only slight changes occurred in the power supply current until the circuit was irradiated at much higher total dose levels. Furthermore, the power supply current remained relatively low (approximately doubling from its initial value) even at 20 krad(Si). Thus, it appears unlikely that the output stage failure was due to field-oxide leakage.

Further evidence for the gate oxide mechanism is provided by comparing the failure level with the expected sensitivity of the gate oxide to radiation, Assuming 100 % hole trapping and transport [3] a 1-volt shift in threshold voltage will occur for a 900 Å gate oxide at 4.5 krad(Si), which is close to the observed 6 krad(Si) failure level for Ioz.

IV. TIME DEPENDENT EFFECTS (TDE)

i. Bipolar Device

The AD674A fully recovered parametrically during TDE tests. Devices were annealed under&tic bias condition at 25 "C for 168 hours, and all failed parameters recovered during the TDE testing.

ii. BiCMOS Devices

At room temperature, parametrically and functionally failed devices recovered after 168 hours. All devices were statically biased during annealing. Ioz which changed smoothly with radiation was used as an indicator of annealing. Figure 4 compares the recovery of Ioz for two different BiCMOS processes (annealing done at room temperature). Note that the recovery time of thetwoprocesses differs bymorethan two orders of magnitude, The rapid recovery of the Maxim process causes the reponse of this device to be strongly affected by the dose rate and the time required to make measurement between irradiations. The recovery time is fast enough so that different results would be obtained by different laboratories applying MIL-STD, Method 1019.4 [4] unless thetimeallotted formeasurements was more stringently controlled.

The oxide-trapped charge usually recovers with time and at high temperature [5]. Therefore, devices were TDE tested after annealing at 100 "C for another 168 hours to observe further recovery results. The devices showed even more recovery due to the results of the combined effects of annealing of the TID radiation induced interface traps and the oxide trapped charges.

V. DISCUSSION

The initial results for these A/D converters have shown that forBiCMOS technologies analogcircuitry degradation is masked by the extreme sensitivity of the ouput leakage current, but that the analog circuitry is the most sensitive part of the circuit for the bipolar devices. Changes in INL and DNL are consistent with a decrease in the effective resolution of the internal comparator and D/A converter circuitry.

The bipolar A/D converters are typically faster and consume more power (0.5-2 W) than MOS devices (-0.1 W). Most manufacturers have replaced bipolar converters with pin-to-pin compatible BiCMOS devices, It is desirable to use the bipolar A/ D converters because they are more resistant to radiation envi-

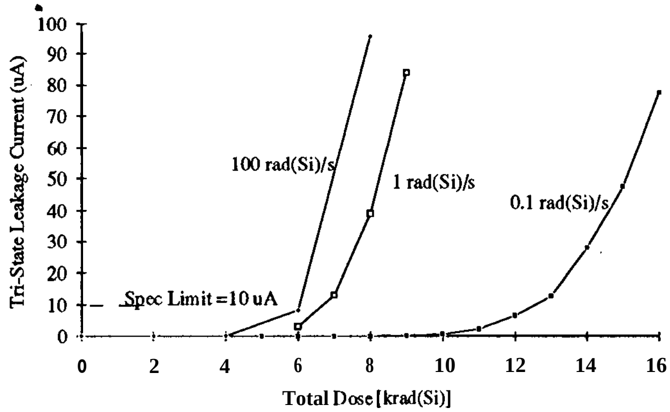

Figure 5. 10Z vs. Dose at Three Dose Rates for MX7672

ronments. However, the trend of the data conversion circuits] systems is to use BiCMOS A/D converters to interface with high-speed and high-resolution microprocessors in applications with very limited power requirements. Although BiCMOS devices can meet the performance requirements of 12-bit A/D converters, circuits with higher precision (16- 18 bits) may still require the use of bipolar circuitry.

For BiCMOS converters, the Ioz parametric failures are most likely caused by oxide traps in the output MOS transistors. This failure mode occurred for two different manufacturing technologies. The rapid recovery time observed for one of the BiCMOS processes caused the total dosehardness to be strongly affected by dose rate. Figure 5 shows the dependence of Ioz on doseat dose rates of 0.1,1, and 100 rad(Si)/sec for MX7672. As the dose rate decreases, the failure level increases significantly. In space applications, it appears likely that this part could be used at much higher radiation levels. Although interface states could limit the effectiveness of annealing in extending the radiation level, devices that were irradiated to 20 krad(Si) were fully within specification after annealing at high temperature.

The dominant failure mode of the BiCMOS devices caused them to fail functionally before significant degradation occurred in the analog functions. Thus, it is not possible to directly compare the radiation hardness of the bipolar analog sections, which were relatively resistant to radiation, with their counterparts in the BiCMOS circuits. Although the output stage leakage current of the BiCMOS devices was well above specification limits at low radiation levels, no significant changes in the performance specification parameters occurred at levels up to 20 krad(Si), which suggests that much harder BiCMOS designs are possible by using either a radiation hardened process, or by reducing the rather thick gate oxide.

All of the A/D converters were more sensitive when irradiated under static bias. When the devices are statically biased, the initialization circuit will set most of the outputs to high and some into low logic states. Statically biased converters showed more degradation than the dynamically biased devices, During low dose rate 0.1 rad(Si)/sec testing in dynamic bias mode, the converter outputs are constantly changing states, Thus, the output n-channel MOS transistors are switching continuously which means that during about half of the irradiation cycle, the outputs are in the off mode. This reduces the charge trapped at the gate oxide interface. Further, the output transistors may exhibit greater annealing during the switching mode.

Most of the new generation, low-power (50- 100 mV), high-speed (5-200 MHz), and high-resolution (16-/1 8-bit) A/D converters are fabricated with radiation sensitive commercial BiCMOS processes. The TID failure level for these types of converters will likely be even lower than the data presented in this paper because a very small change in internal parameters in precision/high performance applications will cause a failure on the internal circuit,

The final paper will further investigate the linearity errors for the major transition codes to study performances over the entire converter transfer function. Detailed circuit and failure analyses will be performed using a SEM to examine the bias dependent effects during ionizing dose irradiation. This should also allow resolution of uncertainties of internal subcircuits for specific parametric failure modes on the bipolar A/D converter. For the BiCMOS devices, the output stage of the converters will be tested and characterized to verify the tri-state leakage current degradation.

VI. SUMMARY

Commercially processed BiCMOS, high-resolution A/D converters are very sensitive to ionizing dose irradiation. Most of them failed parametrically at 6-8 krad(Si) and functionally at 10-14 krad(Si) because of increased leakage in internal MOS transistors. This failure appears to be due to gate oxide threshold voltage in the thick gates used in these designs rather than field-oxide inversion.

The bipolar device is much more tolerant in TID radiation environment and is very strongly dependent on bias conditions. The most important specification parameter for the bipolar device wasthelinearity error (INL). The results ofmoredetailed failure mechanism studies for both device types will be provided in the final paper,

VII. REFERENCES

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