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SEU/SRAM AS A PROCESS MONITOR

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ABSTRACT

The SEU/SRAM is a 4-kbit Static Random Access Memory (SRAM) designed to detect Single-Event Upsets (SEUs) produced by high energy particles. This device was used to determine the distribution in the memory Cell spontaneous flip potential. The variance in this potential was determined to be due to the variation in the n-MOSFET threshold voltage. For a 1.2-μm CMOS process, the standard deviation was found to be 8 mV. Using cumulative distribution and residual plots, stuck cells and non-normally distributed cells are easily identified.

INTRODUCTION:

The usc of matrixed test structures has been shown to be an effective approach to collecting statistical data with respect to inverter threshold voltages [1], metal steps [?] , linewidths [2], and contact resistances [3] . such structures require analog instruments such as a digital voltmeter to determine the measured value.

The SEU/SRAM can be used to obtain analog information using externally forced voltages and on-chip latches (memory cells). This allows more rapid measurements of analog parameters. The structure used in this study is the RADMON (RADiation MONitor), shown in Figure 1. Its primary purpose is to detect single-event upset particles and total dose radiation. The version used in this study is an updated version of a previously fabricated 1.6-μm CMOS chip [4]. It consists of an SEU/SRAM and two total dose p-FETs.

In this study the SEU/SRAM is evaluated as a process control test structure. The size of the RADMON, as shown in Figure 1, is small portion, 2.7 mm^2, of the stepper field of 200 mm^2. The memory cell layout is shown in Figure 2. The SRAM was fabricated with 1.2-μm n-well CMOS process at a MOSIS brokered foundry,

The SRAM cell schematic, shown in Figure 3, has a six-transistor memory cell with an offset voltage, V_o, that is used to evaluate the spontaneous cell flip potential. The dimensions of the MOSFETs in the cell are listed in Table 1. The timing diagram for the operation of the cell is shown in Figure 4. This diagram shows that the cell has three modes of operation: Read, Write, and Stare. In the Read and Write cycles, V. = 5 v. Initially all the cells are written into the initial state which is described in Figure 3. Then the cells are operated in the Stare cycle in which V. is gradually lowered to a potential V_0(stare). In this state ionizing particles that deposit sufficient charge will flip individual cells. If V. is lowered sufficiently, the memory cells will flip spontaneously. This is the behavior that will be analyzed in this paper for its usefulness as a process monitor. It will be shown that the spontaneous flip potential is a measure of the uniformity of the threshold voltage of inverter #1, VT_{i1}.

MEMORY CELL MODEL:

The cell spontaneous flip behavior is explained by the SRAM transfer curves shown in Figure 5. These curves were generated using a simple model for the MOSFET drain current which does not include channel length modulation [5]. The inverter has an input voltage, Vin, and output voltage, V_{out}. The CMOS inverter transfer curve is divided into five regions [G] . These regions arc described with respect to VT_n = n-FET threshold voltage, VT_p = p-FET threshold voltage, and VT_i = inverter threshold voltage.

in Region I, $0 < V_{irl} < VT_n$ and $I_n = I_p = 0$ and $V_{out} = VDD$. In Region 11, $Vl_n < Vi_n < VT_i$ and $I_{nsat} = I_{plin}$. In Region 111, $V_{in} = V_{out}$, $I_{nsat} = I_{psat}$. In Region IV, $VT_i < Vi_{rl} < VDO - VT_p$, $I_{nlin} = I_{psat}$. In Region V, $VDD - Vlp < Vi_{rl} < VDD$, $I_{rl} = I_p = 0$ and $V_{out} = 0$.

The MOSFET drain currents arc:

(1) $I_{nlin} = \beta_n(V_{in}-VT_n-V_{out}/2)V_{out}$

(2) $I_{nsat} = (\beta_n/2)(V_{in}-VT_n)^2$

(3) $I_{pl\,in} = \beta_p(VDD-V_{in}-VT_p-(VDD-V_{out})/2) \cdot (VDD-V_{out})$

(4) $I_{psat} = (\beta_p/2)\,(VDD-V_{in}-VT_p)^2$

where $\beta = KP \cdot W_e/L_e$ and VT is the threshold voltage. For p-FETs VT is the magnitude of the threshold voltage. Also $KP = \mu \cdot C_{ox}$ where μ is the channel mobility, and C_{ox} is the gate oxide capacitance/area. Finally $W_e = W-\Delta W$ and $L_e = l-\Delta L$ where W and L are the as-drawn channel width and length respectively, ΔW and ΔL are the channel width and length correction factors, respectively. The MOSFET values used in the following analysis are shown in Table 2.

The memory cell has two stable states located at the upper-left and lower-right corners of the chart shown in Figure 5. As V_o decreases from 5 V, the upper-left stable point follows a path described by the circles shown in Figure 5. When V_o = 1.5 V, the cell flips to the lower-left stable point.

EXPERIMENTAL RESULTS:

The memory cell V_o distributions are shown in figure 6 for eleven chips from Wafer #1. As seen in Figure 6, the SRAMs have a distribution of offset voltages at which the cells flip. The data was acquired by lowering the offset voltage, V_o, and counting the number of flipped cells at that V_o value. The memory was then reset and the offset voltage lowered to a V_o that is 1 mV lower than the previous value and again the number of flipped cells determined. This process is repeated until all 4096 cells flip. Note that these curves are completely deterministic. That is for a given V_o, the same cells flip.

The distributions shown in Figure 6 are Gaussian in nature and can be characterized by the normal distribution with a mean of $V_{o\mu}$ and a standard deviation of V_{oo}. The cumulative distribution plots for the chips shown in Figure 6 are shown in Figure 7.

The data is characterized by the cumulative probability function using:

(5) $P(V_{oi}>V_o) = 100 \cdot (N-0.5)/N_t$

where N is the number of flipped cells at V_o and for this memory N_t = 4096. The analytical formula that describes the cumulative distribution is:

(6) $N = N_t\{1-erf[(V_o - V_{o\mu})/V_{oo}\sqrt{2}]\}/2$

where crf is the error function. The result of a least squares fit to each of the curves shown in Figure 7 is listed in Table 3. The entire range of data was fitted. Notice that the curves with the largest standard deviations, namely chips #2 and #4, have cells that deviate significantly from the main distribution. The standard deviations for the distributions is the tightest observed to date being about 8 mV. Previously observed standard deviation values for a 1.6-μm CMOS process were shout 10 mV [4],

Selected chips are examined in detail in Figures 8 to 10 where the cumulative and residual distributions are shown. The cumulative distribution allows a critical examination of the tails of the distribution. The residual distribution allows a critical examination of the cells near the mean of the distribution. An example of a stuck column is shown in Figure 8 and a stuck cell is shown in Figure 9. Acceptable behavior is shown is shown in Figure 10.

The results were simulated with a normally distributed sample. As seen in Figure 11., several data points fall slightly below the fitted line in the tails of the distribution. This same behavior is shown in Figure 10.

A summary of the results from all the wafers included in this study are shown in Figure 12. These samples came from four wafers and are tightly clustered. The mean offset voltage has a span of 30 mV and the standard deviation of the offset voltage varies from 7 to 9 mV. This is considered excellent cell distributions for cells located (a) within a chip, (b) between chips, and (c) between wafers.

DATA ANALYSIS:

The interpretation of results follows from observing the nature of the transfer curves shown in figure 5, A close examination of this figure reveals that the spontaneous flip point is determined when V_o reaches the threshold voltage of inverter #1, VT_{i1}. The CMOS inverter threshold voltage is determined by the conditions given in Region III described above:

$$(7)\quad VT_i = \frac{VDD + VT_n\sqrt{\beta_r} - VT_p}{1 + \sqrt{\beta_r}}$$

where VT_n is the n-MOSFET threshold voltage, and VT_p is the magnitude of the p-MOSFET threshold voltage. The Beta factor is:

$$(8)\quad \beta_r = \frac{\beta_n}{\beta_p} = \frac{KP_n(W_n - \Delta W_n)(L_p - ALP)}{KP_p(W_p - \Delta W_p)(L_n - AL_n)}$$

The inverter threshold equation is plotted in Figure 13 and shows that for $\beta_r \to 0$, $VT_i = VDD - VT_p$ and for $\beta_r \to \infty$, $VT_i = VT_n$.

Using propagation of error analysis, the variance of the inverter threshold voltage is:

$$(9)\quad VT_{io}^2 = \frac{VT_{po}^2}{(1 + \sqrt{\beta_r})^2} + \frac{\beta_r VT_{no}^2}{(1 + \sqrt{\beta_r})^2} + \frac{\beta_r(VDD - VT_n - VT_p)^2}{4(1 + \sqrt{\beta_r})^4}\cdot G$$

where

$$(10)\quad G = \frac{W_{no}^2}{W_{en}^2}, \frac{W_{po}^2}{W_{ep}^2}, \frac{L_{no}^2}{L_{en}^2} + \frac{L_{po}^2}{L_{ep}^2}$$

These equations show that for $\beta_r = 0$, $V_{li} = (VDD - VT_{p\mu}) \pm VT_{po}$ and for $\beta_r = \infty$, $VT_i = VT_{n\mu} \pm VT_{no}$.

The spontaneous flip point, $V_{\circ}$, was determined to be equal to the inverter threshold voltage of inverter #1. This conclusion was reached as follows. The Beta factors for the two inverters in the memory cell are: $\beta_{r1} = 10.7$ and $\beta_{r2} = 15.1$. Introducing these values into Eq, (7) leads to the inverter thresholds: $VTi_1 = 1.48$ V and $V_{li2} = 1.39$ V. The $VT_{i1} = 1.48$ V is the spontaneous flip point shown in the simulation given in Figure 5. This value is close to the experimentally observed V. values clusc to 1.72 V summarized in Figure 12. The discrepancy between 1.48 and 1.72 is easily explained by the simplistic MOSFET model given in Eqs. (l)-(4). If channel length modulation was included in the MOSFET model, then the transfer curve for INVT#1 would have a finite slope at the mid-point. This will increase the modeled spontaneous flip point from 1.48 V and bring the result closer to the experimental value of 1.72 V.

The standard deviation of $\sigma_{\circ}$, is mainly due to the variation in the n-FET threshold voltage. This conclusion was reached as follows. Introducing the FET model parameters listed in Table 2 into Eqs. (9) and (10) leads to:

$$(11)\quad VT_{io}^2 = 0.055\cdot VT_{po}^2 + 0.586\cdot VT_{no}^2 + 0.008\cdot G$$

for inverter #1. This equation shows that VT_{no} is the dominant parameter.

Now the results in Figure 12 and Table 3 can be interpreted as follows. The mean offset voltage is:

$$(12)\quad V_{o\mu} \approx VT_{i1}$$

and

$$(13)\quad V_{\circ\circ} \approx VT_{no1}$$

The conclusion, given in Eq. (13), is determined by the layout of INV#1 where $\beta_{r1} = 10.7$. Thus by changing the layout of the cells, various features of the cells can be sensed.

CONCLUSION:

The SEU/SRAM provides data on the uniformity of a CMOS process. The 4-kbit SRAM memory cell offset voltages were found to be normally distributed. The offset voltage depends on the threshold voltage of inverter #1 and its distribution depends on the variation in VT_{n1}. Cumulative distribution plots reveal SRAMs with stuck bits which appear in the tails of the distribution. Residual plots reveal SRAMs with bits that do not flip according to a normal distribution near the mean of the distribution. The observed variances were about 8 mV. This result is considered excellent behavior within a chip, chip-to-chip, and wafer-to-wafer. This result provides a measure of excellence to be met by future CMOS foundry runs.

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Table 1. Dimensions of SEU/SRAM MOSFETs.

FET	L (μm)	W (μm)	Ad (μm^2)	B ($\mu A/V^2$)
Mn1	1.?	2.4	17.92	180.8
Mn2	1.2	3.?	74.88	16.9
Mp1	3,2	2.4	14,08	255.5
Mp2	3.?	2.4	12,16	16.9
Mt1	1.2	2.4	-----	
Mt2	1.2	2.4	-----	

Table 2. MOSFET Model Parameters (Run N26D, 1_o = 20°C).

PARAM	UNITS	MEAN	STDEV
n-FET RESULTS			
VT_o		0.69	± 0.0101
KP_o	$\mu A/V^2$	69.00	± 1.2000
ΔW	μm	0.46	± 0.0200
AL	μm	0.46	± 0.0116
p-FET RESULTS			
Vl_o	V	0.95	± 0.0087
KP_o	$\mu A/V^2$	23.00	± 0.5200
ΔW	μm	0.30	± 0.0310
Al	μm	0.35	± 0.0180

Table 3. SEU/SRAM V. results.

CHIP	WAFER NO.1 $V_{0\mu}$ ± V_{00}
#l	1.7246±0.0076
#2	1.7202?0.0091
#3	1.7226±0.0081
#4	1.731930.0092
#5	1.7209±0.0078
#6	1.7224$0.0075
#7	1.7247±0.0077
#8	1.7099±0.0089
#9	1.7236%0.0084
#lo	1.7108*O.OO79
#11	1.7205*0.0078

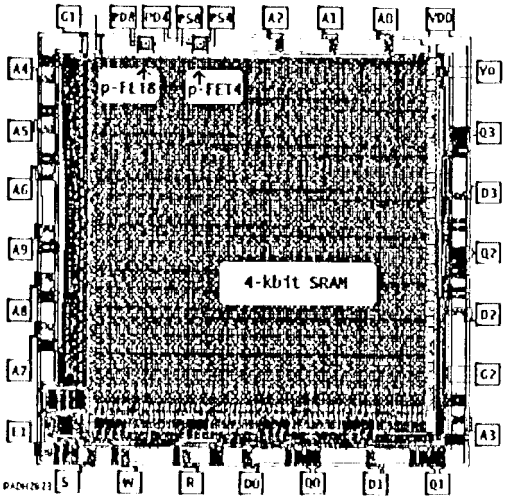

Figure 1. RADMON: 1.6 mm x 1.7 mm.

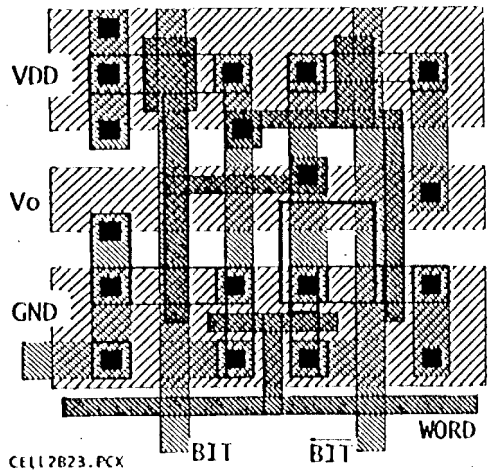

Figure 2. Memory cell: 33.6 μm x 36.0 μm. The n-well and n- and p-select layers are omitted.

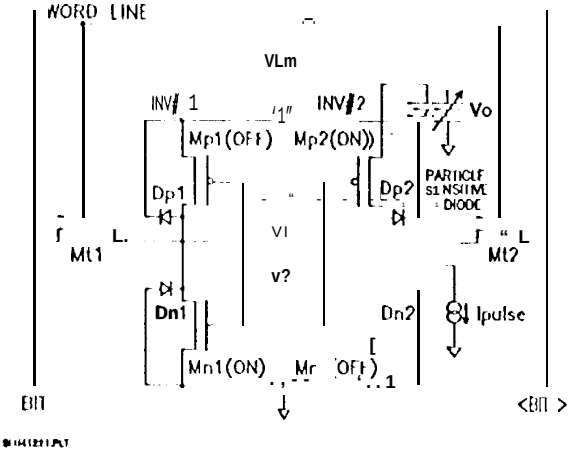

Figure 3. SRAM memory cell circuit.

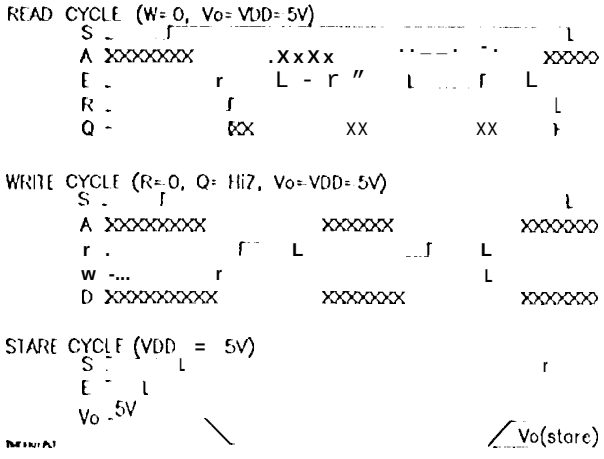

Figure 4. SRAM memory cell timing diagram.

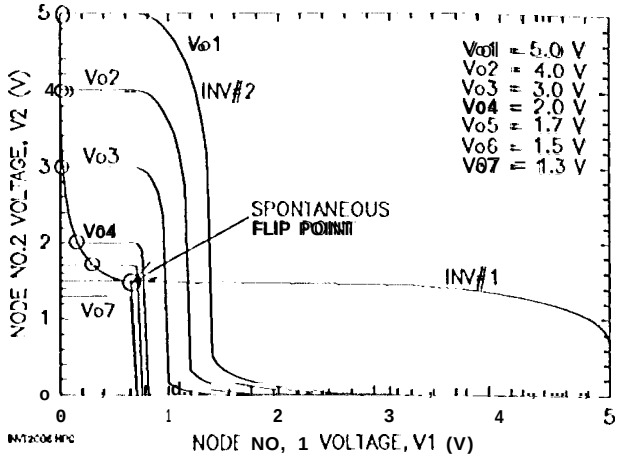

Figure 5. SRAM transfer curves showing the variation in the stable point, indicated by circles, as the offset voltage, V_o, is lowered to the spontaneous flip point.

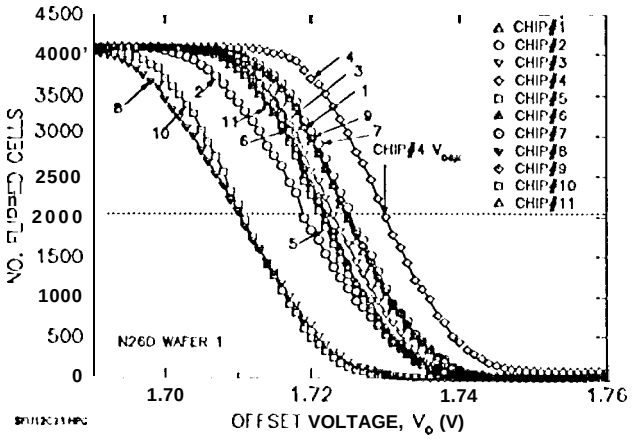

Figure 6. SEU/SRAM spontaneous flip response from eleven chips taken from 1.6-μm CMOS Wafer#1.

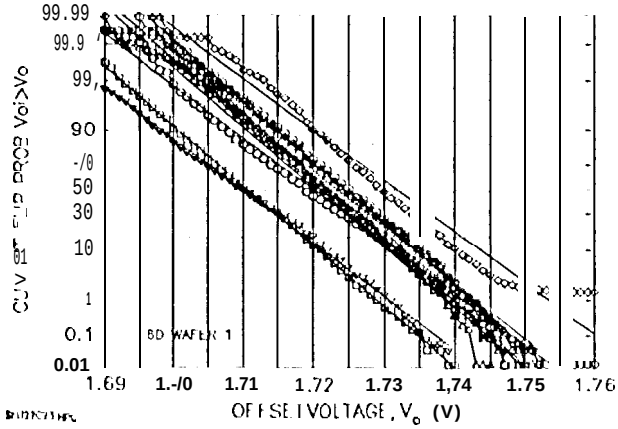

Figure 7. Cumulative distribution plots for the chips shown in Figure 6.

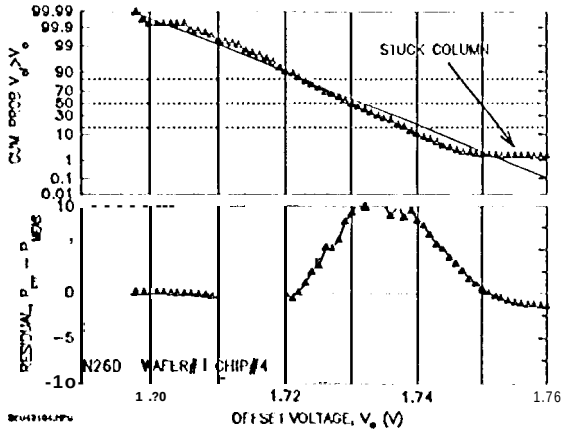

Figure 8. Results from Chip#4 Figure 6) showing a stuck column.

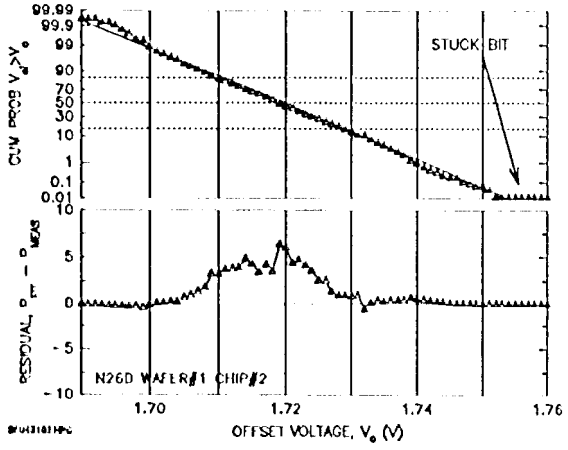

Figure 9. Results from Chip#2 (Figure 6) showing a stuck bit.

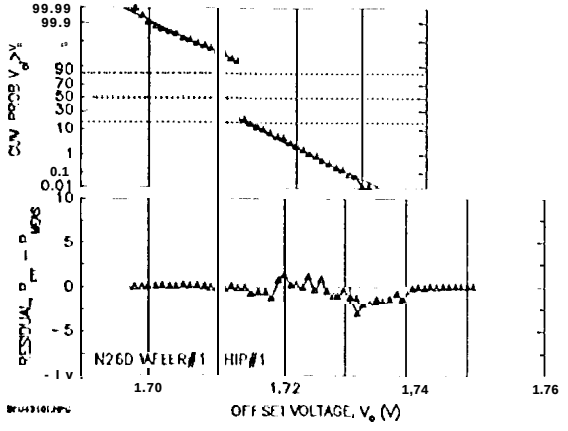

Figure 10. Results from Chip#1 (Figure 6) showing acceptable behavior.

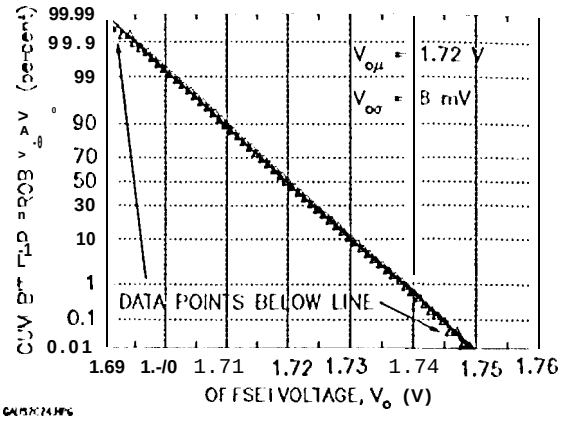

Figure 11, Ideal cumulative distribution plot for $V_{o\mu}$ = 1.72 V and V_{oo} = 8mV.

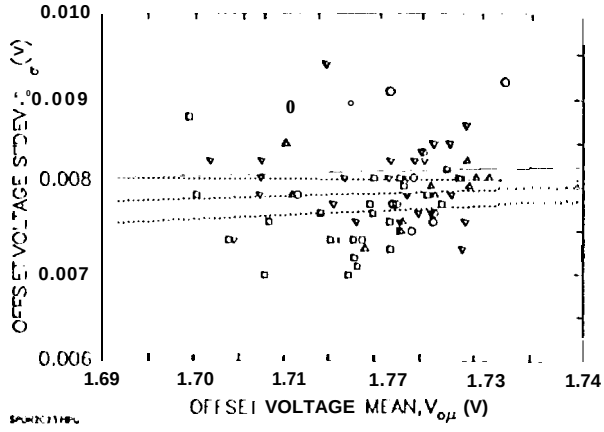

Figure 12. Standard deviation vs mean offset voltage for chips fabricated on four wafers. The lines are linear regression fits to data from each wafer,

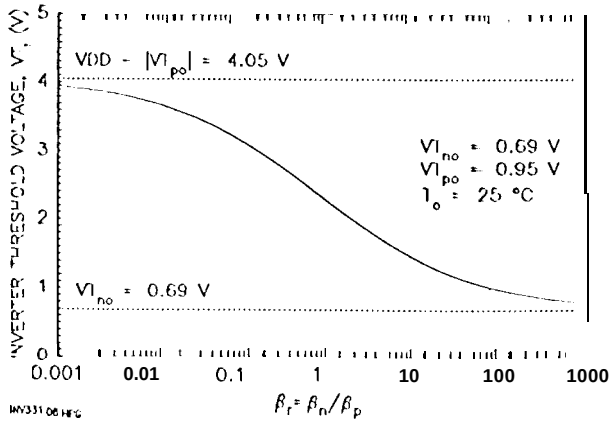

Figure 13. Inverter threshold voltage dependence on the MOSFET geometry factor β_r.