DEVELOPMENT OF A SOLID STATE POWER SWITCH FOR THE CASSINI SPACECRAFT

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ABSTRACT

The Cassini Spacecraft uses a new hybrid device to replace the load switching relays used on previous missions. These hybrid devices provide additional functions such as circuit breaking, controlled voltage turn-on and current limiting features. The current limiting, function makes an uninterruptible power system possible. This hybrid, the Solid State Power Switch (SSPS), performs the function of connecting the 192 Cassini loads to the spacecraft power bus in response to commands from the Command and Data Subsystem. Each SSPS is capable of carrying and switching up to a 3 Amp (90 Watt) load. The power and return sides of the spacecraft loads are "switched" utilizing solid state components. The internal circuitry resembles two independent switches cross-strapped for redundancy. The SSPS acts as a circuit breaker by monitoring the current drawn by each load and continually comparing that value to an externally selected trip level and an internal fail-safe trip level. If the load current exceeds either trip point for approximately 1 mS, then the SSPS will turn the load off. The SSPS controls the load voltage at turn-ON in a linear fashion, rising from O to 30 Volts in approximately 100 mS. In the event of a load fault, within 50 μS the SSPS will limit the current to 6 Amps and maintain that value until the switch turns OFF.

INTRODUCTION

Background

The long lineage of spacecraft power system designs from the Jet Propulsion Laboratory (JPL) includes, Voyager I and 11, and most recently, Magellan, and Galileo. JPL power system engineers began the first steps in defining what was to become the Cassini Power System in 1984. The need to produce a highly reliable, cost-efficient, generic spacecraft power system led to an autonomous, fault tolerant, "uninterruptible" power system, The uninterruptible power system was defined as a system where "electrical faults on power user 'x' would be transparent (at least from a power point of view) to all other power users". Previous power system designs were fault tolerant and recoverable after a fault, but they did not achieve the goal of maintaining power bus integrity under all possible load fault conditions.

Definition of the "uninterruptible" power system led to the need for a new device; a device that could perform the functions of power switching and fault protection. The motivation to develop a solid state device was provided by previous JPL experience with the procurement of S-level relays and the fact that the traditional relay/fuse combination was not optimum for the uninterruptible power system. Additionally, a solid state device would provide the option of restarting a faulted load, which is not possible on conventional relay/fuse based systems. The new device combined fault protection and power switching and came to be known as the SSPS.

The Mariner Mark II Power System

'Cassini's predecessor, the Mariner Mark II (MMII) spacecraft, was intended to be a generic deep space vehicle, adaptable to a variety of missions, The first two missions were to be Comet Rendezvous Astroid Flyby and Cassini.

The MMII power system consisted of two Radioisotope Thermoelectric Generator power sources; a regulated main power bus; redundant batteries for load leveling and transient capability; a p-processor for autonomous power management and fault protection; and a power distribution section containing 256 Solid State Power Switches (SSPSs).

The MMII power system utilized the SSPS to achieve "distributed fault protection". The regulated main power bus was allocated to the power users through individual SSPSs. Each SSPS provided load-fault protection, giving rise to the term "distributed fault protection'. Electrical faults on the user end could be detected, controlled and subsequently removed while maintaining continuous uninterrupted power to all the other users,

SSPS DEVELOPMENT

Derivation of SSPS Functional Requirements

The definition of the MMII power system led directly to a set of functional requirements for the SSPS.

The SSPS must remove faulty loads from the power bus. Load faults are detected by monitoring load current and comparing the measured current to an expected maximum value. If the measured current exceeds the expected value for a given period of time, the load has faulted, The expected maximum value is called the *trip current* and the time period is called the *trip time*. If the trip time is too short, the device could be sensitive to random noise. If the trip time is too long, the internal transistors could be damaged due to excessive heat, A trip time of 1 mS was selected for the SSPS. Thus, if the load current were to continuously exceed the trip current for 1 mS the SSPS would interrupt the flow of power to the load. The trip current could be commanded to one of eight values from 0.6 Amps to 4 Amps. Eight trip current values were provided to support more precise spacecraft power management.

Since load faults of zero impedance can theoretically occur instantly, the SSPS must provide some form of current limiting to prevent the bus voltage from falling to zero during the 1 mS trip time interval. The SSPS current limiting requirement is called the *clamp current*. The minimum clamp current must always be greater than the maximum trip current plus worst case tolerances. The maximum clamp current is also limited by transistor stress requirements and safe operating area guidelines. Excessive clamp current could destroy the SSPS transistors, Additionally, the time required for the SSPS circuitry to respond to a short is important. Given an instantaneous short, current will exceed the clamp value until the circuit reacts to bring the current under control. The *transient recovery time* must be short, compared to 1 mS, in order to prevent excessive stress. The SSPS clamp current requirement was specified as 10 Amps with a 50 μS transient recovery time.

Closing a switch to initialize a load will generate an inrush current. Inrush currents resulting from relay load initialization have been blamed for 'bus jump" (voltage excursions on the power bus). Bus jump in the extreme case can result in unexpected glitches in spacecraft digital circuits. Additionally, capacitive loads must be provided with inrush current limiting circuitry. The SSPS was designed with internal inrush limiting to prevent bus jump, and to allow the SSPS to be used on capacitive loads without external inrush circuitry. Incorporating the inrush limiting function in the SSPS increased the complexity of the SSPS, but because external discrete components were eliminated, the overall result was a decrease in the power system's mass and volume. The SSPS inrush current limit feat ure is described by the *soft start* requirement. When the SSPS is commanded ON into a 30Ω resistive load, voltage is required to rise linearly from zero to full value over a 100 mS time period. The load current rise time is a function of the type of load, but in all cases the SSPS soft start yields significantly slower current rise times than a relay closure, Thus, the SSPS avoids the problems caused by relay "noise" and the bus jump phenomenon.

Since fault protection was of paramount importance, all fault protection features, clamp current, over current trip, OFF command capability, etc., were required to remain functional, given any single fault within the SSPS. The requirement was satisfied by utilizing two independent Mocks of switching circuit ry; one block switches the load power line and the second block switches the load return line. Connected in series and cross-strapped for command

redundancy, the two blocks guarantee that fault protection will work even if one block has been rendered inactive due to a failure. A functional block diagram of the SSPS is shown in Figure 1.

The desire for improved power management led to SSPS requirements for monitoring load current, trip level and switch state (ON, OFF,TRIPPED). The SSPS was required to provide two continuous analog and three digital signal outputs for processing by the p-processor and forwarding to the spacecraft computer for use in downlink telemetry. This information was expected to greatly facilitate spacecraft power management. Prior to M MII, individual load power status was not directly available and had to be derived from global current and voltage measurements,

The MMII command system utilized two independent redundant command data busses. A unique 8 bit address was assigned to each SSPS. When a command was transmit ted, the appropriate SSPS would respond. Thus, the SSPS was required to include an internal address decoder and command processor. Combining the command decoder in the SSPS increased the complexity of the SSPS, but the external circuit ry was substantially simplified and fault tolerance was greatly improved over that of a comparable external decoder.

A serial command format was chosen to reduce the need for SSPS 1/0 pins, and to simplify external circuitry. Additionally, two independent command ports were incorporated for command redundancy.

The SSPS was required to reset itself to the OFF state, upon initial ization of spacecraft power. This was accomplished by providing a ***power on reset*** pin on the SSPS. This requirement was needed to simplify power system initialization and to facilitate system assembly and test.

With 256 SSPS on the MMII spacecraft, SSPS power dissipation was a significant concern. If each SSPS were to dissipate 1 Watt, then 256 Watts of spacecraft power would be required to operate the SSPSS! Power dissipation consists of two components: (1) I^2R loss from the flow of current through the switch, this component is load dependent, and (2) standby power consumption due to circuitry within the SSPS. The ***ON-State Resistance*** and ***Standby Power*** requirements were established at O.15Ω and 25 mW respectively, to limit power losses.

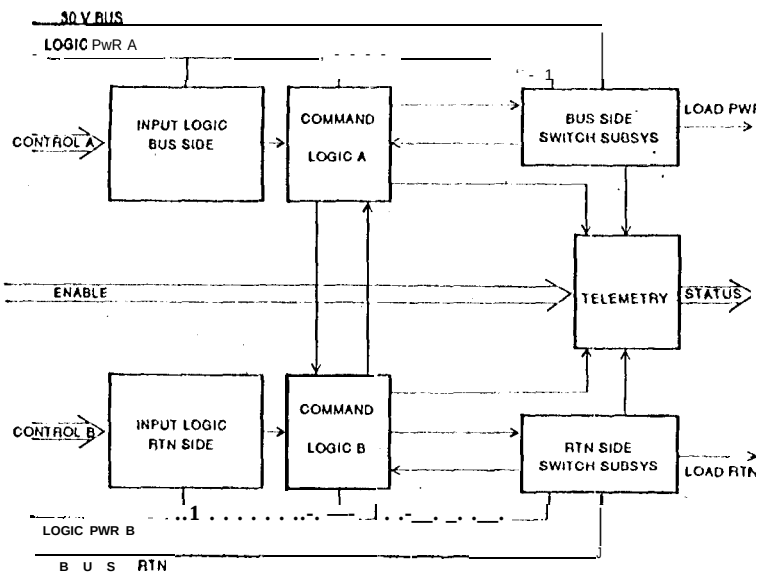

Figure 1. Functional Block Diagram of SSPS

MMII to Cassini Redesign and Impact on SSPS

A project-level decision was made to build a mission specific Cassini spacecraft instead of the MMII spacecraft. 'I'he resulting changes, which occurred relatively late in the design cycle, had a significant impact on the SSPS. Preliminary circuits had been simulated, breadboarded and tested at this point. Many of these circuits needed to be modified to accommodate the Cassini specific power system.

The MMII concept included a battery, however, the battery was eliminated from the Cassini spacecraft. The elimination of the battery had a great impact on the SSPS design. The MMII battery supplied the 10 Amps of "clamp current" needed to "hold up" the bus during a load fault. The only source for clamp current on Cassini was the bus (filter) capacitance. The energy available from the bus capacitance was much less than that available from a battery, Consequently, the current available during a load fault was much smaller, If the uninterruptible power concept was to be preserved, the clamp current requirement had to be changed. The clamp current requirement was changed from 10 Amps to 6 Amps and, a worst case tolerance of ± 1 Amp was levied over all voltage and temperature ranges, radiation and aging inclusive. The effect of the change was a total redesign of the clamp circuit which resulted in the

addition of a considerable number of components.

The MMII definition of uninterruptible power did not include "source faults" (faults within the power system). When source faults were added to the Cassini definition, a decree was issued that *all* loads, including the power system electronics, would be connected to the power bus through SSPSs. Some of the SSPSS had to initialize to the ON state upon initial application of bus power, Thus, a *power on reset ON* function was added to the SSPS requirements. The end result was a redesign of the digital section of the SSPS resulting in additional components and the addition of two more power on reset pins.

The p-processor was eliminated in the Cassini Power System. On the MMII system, trip levels were embedded in the SSPS command word and were adjustable in flight. Removal of the processor was combined with a new Cassini requirement that trip levels be hardwired (and not adjustable in flight). The ability to precisely manage spacecraft power was degraded, The eight SSPS over-current trip levels and the trip level monitor were retained. The SSPS decoder circuit was modified and three pins were added to the package to facilitate external selection of the trip level.

A maximum dV/dt specification was added to the turn-OFF requirement. The end result was the addition of circuitry and a nagging stability problem in the SSPS analog circuitry.

The standby power requirement was increased from 25 mW to 70 mW to accommodate the additional circuitry.

Upon the completion of the requirements definition and preliminary bread boarding phases, the "worst case" design method was used to generate a comprehensive electrical design. The worst case design method entailed using worst case parts parameters in design calculations. The worst case parts parameters included the effects of radiation, age and temperature. The end result was a very robust electrical circuit, Formal worst case analysis confirmed the effectiveness of the method when no major performance problems surfaced. The elect rical design was translated to a printed circuit board and tested. Following, successful functional testing, the hybridization effort was started.

Hybrid Development and Test

The SSPS will be the first known flight qualified hybrid to be fabricated in accordance and in compliance with MIL-H-38534A, K level requirements. The primary contractor was CTSM of Indiana, The manufacturer was required to design the hybrid and generate the official SSPS hybrid design documentation. The digital ehxtronics(31 digital ICs) were implemented with two redundant gate-arrays. The gate-arrays were fabricated by UTMC of Colorado.

Since the SSPS had been designed, analyzed, bread-boarded and tested by JPL using discrete components the hybridization effort had to provide early proof that the hybrid version would comply with performance requirements.

Six "form, tit, function" developmental units were fabricated, in sets of two, and delivered to JPL for test and evaluation. This enabled both JPL and the CTSM to verify hybrid performance and also allowed for hybrid design adjustments. Indeed, a few material, hybrid design and hybrid performance issues did arise. Upon completion of the developmental phase, a Critical Design Review was conducted at JPL.

Following the Critical Design Review, thirty five (35) flight like (MIL-H-38534A) Design Verification Units were fabricated on a Class K compliant line. These, flight like, "first-off" production units were used to prove and demonstrate the hybrid's compliance to the rigorous flight qualification requirements. Following electrical test ing, twenty-two (22) were placed on an extended life test of 2000 Hours at 125°C under power and with some dynamics. The extended life test will also be performed on flight units and will extend into and beyond the fabrication phase. The remainder of the Design Verification Units were allocated for a variety of JPL tests such as radiation, residual gas analysis, destructive part analysis and load-switching.

Fabrication of flight qualified hybrids was supposed to occur after the conclusion of the Design Verification Unit evaluation. 1 Iowever, due to schedule constraints, the fabrication effort began before the conclusion of the Design Verification Unit effort.

JPL and CTSM have both developed automatic-test-equipment to characterize the hybrids. Manual testing

of a hybrid had been proven to consume several days of time. The JPL automatic-test-equipment was designed for thoroughly characterizing the hybrids in a developmental environment. CTSM's automat ic-test-equipment was designed for testing flight hybrids in a manufacturing, Class K compliant environment. CTSM's automated test system took less than an hour to test the hybrid over nine different temperat ure and voltage ranges.

RESULTS

SSPS Hybrid Description

The SSPS hybrid "utilizes a five-layered Alumina based substrate with all gold metalization. Resistors are screened thick film. The thermal performance of the SSPS package was a critical design parameter, The two MOSFETs, along with two 60 mΩ current sensing resistors, were mounted on the Alumina base of the network to enhance thermal conductivity. The FET substrate area is gold coated (two layers) and the FETs are epoxied to the substrate. The 60 mΩ current sensing resistors are thick film on Alumina, manufactured to spec by CTSM. One and 2 mil gold wires and 8 mil Al wires are used for bonding.

All devices and the network are Epoxy attached. The epoxy is cured at 95*C to 105°C for 60 to 65 min. and 190°C to 200"C for 60 to 65 min. All of the screened resistors are laser trimmed with 12 resistors being actively trimmed to meet specified parameters. Following the epoxy attach and before wire-bonding, the hybrids are plasma cleaned. Each hybrid is mounted in a specially designed carrier. The hybrid stays in the carrier for most of the fabrication steps and the hybrids are delivered to JPL in the carrier. Following fabrication and before final test, the hybrids are burned-in for at least 260 hours at 125°C to 135°C.

Reference Figure 2, hybrid attributes are as follows: Kovar package and lid (seam welded); 35 active components (IC dice); 26 chip resistors and capacitors; 181 screened resistors; 12 actively trimmed resistors; 466 wire bonds of which 391 are 1 mil Gold.

SSPS Packaging

The hybrid SSPS is packaged in a low thermal impedance, Kovar package with 36 glass sealed leads on the each long sides of the package (72 leads total). Physical dimensions are: 5.07 cm long, 4.27 cm wide, 0.43 cm high (1.995" x 1.680" x 0.170").

The mass was specified as 34 g maximum and the first Design Verification Units were (measured) approximately 31.5 g.

Fabrication Results

The SSPS hybrid fabrication effort is well under way as this paper goes to print. Fifteen units have successfully completed the 2000 Hour extended life test. Additional units will be placed on life test at the end of May and June of 1994. One-hundred and Seventy-Nine (179) flight hybrids are currently at JPL and the remainder (321) units are expected to be delivered by mid-June 1994.

Cassini Power System Attributes

The Cassini Power System supplies power to 192 spacecraft loads and uses the Solid State Power Switch to help isolate the loads from each other. The power system achieves the goal of uninterruptible power, even if the fault is within the power system. The SSPS helped reduce the overall system size and cost by consolidating internal redundant command decoding and inrush current limiting, over-current trip and load current monitoring into a hybrid package. The Cassini Power System will self-start to facilitate system integration and test and, although there is no known failure that would cause such a loss, the Cassini Power System will recover if power is interrupted for an indeterminate period time and subsequently restored.

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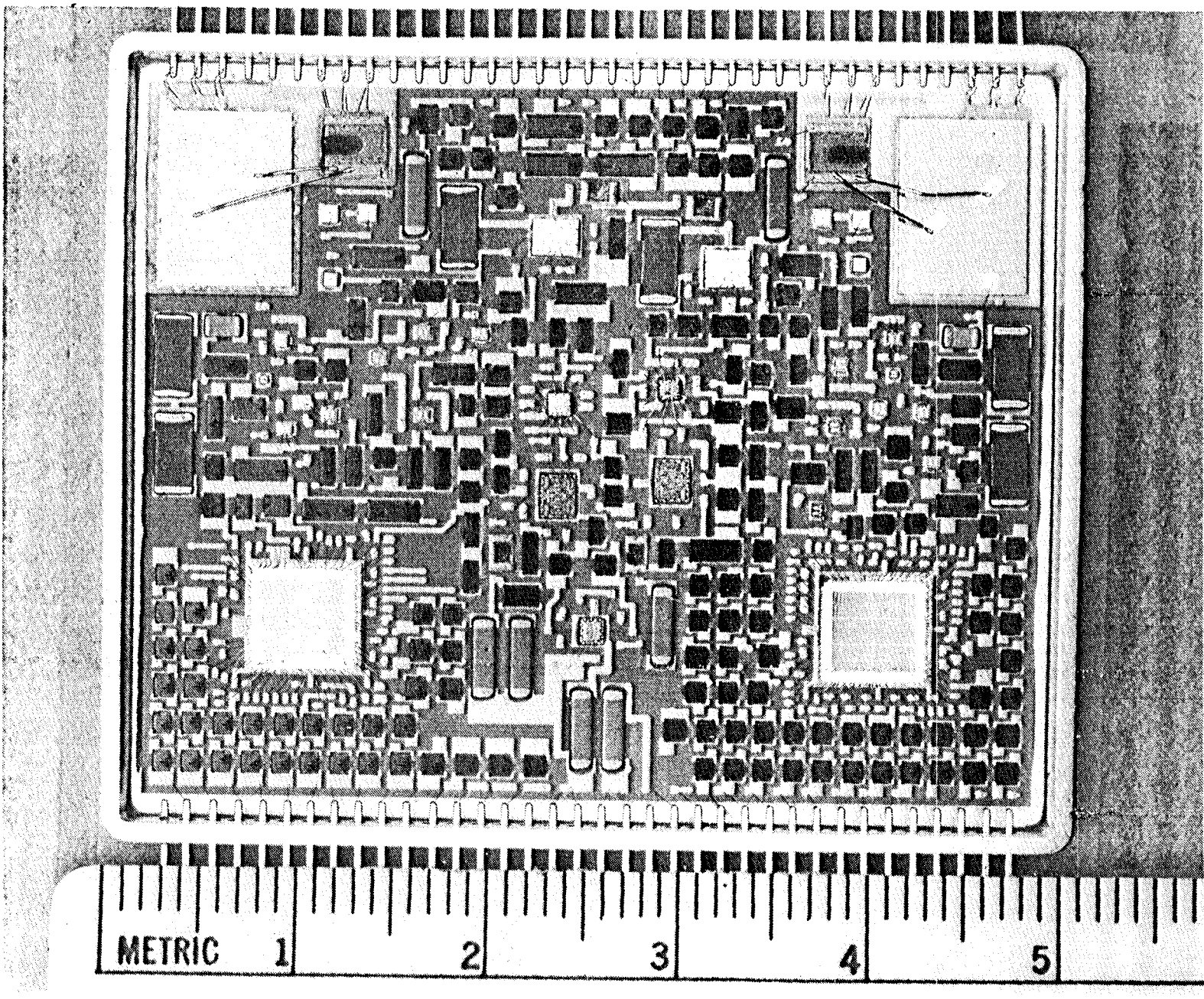

Figure 2. Hybrid Solid State Power Switch