lligh-Density Vertical Bloch Line Data Storage Chips for Small Satellite Applications

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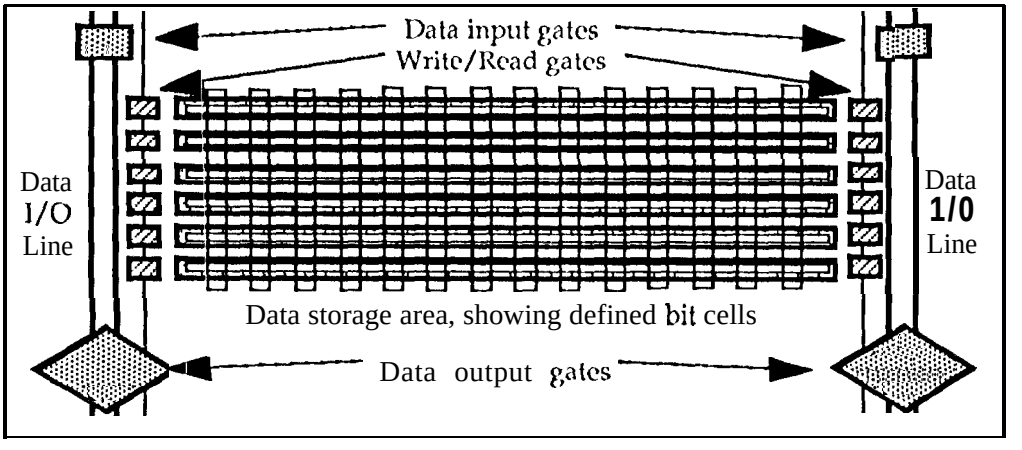
Vertical Bloch Line (VBL) storage is an emerging technology which has the potential for offering a number of desired data storage attributes in a single chip for space and commercial applications. VBL technology[1,2,3] potentially offers high areal storage density, ranging, as shown in ~'able I, from 25 Mbits/cm^2 to greater than 1 Gbit/cm^2. In addition, VBL technology offers nonvolatility and reduced power consumption, radiation hardness, and rapid mass erasability, Current activities are aimed at integrating storage chip functions into prototype chips with capacities of 16 Mbits to 256 Mbits over the next 1 to 3 years. As shown in Figure 1, data arc stored in a VBL chip using the presence or absence of micromagnetic VBL pairs in bit cells defined along magnetic domain walls. Data arc written into the chip and placed into the magnetic data storage domain walls using a current-access major line and write gates. Data arc read from the magnetic data storage domain walls using read gates which arc common to the write gates, and are amplified and read out of the chip by a magnetoresistive sensor.

Table I. Potential VBL Areal Storage Density Performance:

Magnetic Storage Domain Width	Lithography: 1 µm	Lithography: 0.5 µm	Lithography: 0.25 µm	Lithography: 0.1 µm
5 µm	10 Mbits/cm^2	20 Mbits/cm^2	40 Mbits/cm^2	100 Mbits/cm^2
2 µm	25 Mbits/cm^2	50 Mbits/cm^2	100 Mbits/cm^2	250 Mbits/cm^2
1 µm	50 Mbits/cm^2	100 Mbits/cm^2	200 Mbits/cm^2	500 Mbits/cm^2
0.5 µm	200 Mbits/cm^2	400 Mbits/cm^2	800 Mbits/cm^2	2,000 Mbits/cm^2
0.25 µm	400 Mbits/cm^2	800 Mbits/cm^2	1,600 Mbits/cm^2	4,000 Mbits/cm^2

Figure. 1. Schematic VBL architecture:



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