

# Highly accurate tracking system for a laser communications link

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## ABSTRACT

A high frame rate CCD camera with interface to a digital signal processor has been developed for a pointing control loop for laser communications. The CCD array is operated in a windowed-read mode with the digital signal processor controlling the vertical and horizontal shifts in the image and storage planes. Development of the camera and interface hardware for a demonstration of precision beam pointing is presented.

## 1. INTRODUCTION

This paper describes the development of a high frame rate CCD camera and a digital signal processor (DSP) interface electronics for a steering mirror pointing control loop<sup>2,4</sup>. The CCD array is used to obtain centroids of a transmit laser spot and a beacon laser spot at frame rates of up to 2 KHz for closed loop control of the transmit/receive point-ahead angle. In order to achieve a high frame rate, the CCD array is operated in a windowed-read mode where only the windows of interest in the array containing the transmit and beacon laser spots are read out and processed, and the rest of the pixels are bypassed. A DSP processor is used to operate the CCD camera in the windowing mode and perform all the functions necessary for precision beam pointing, including centroid processing and control loop compensation. The operation of the CCD camera and the steering mirror by the DSP processor is done through an interface electronics which will be described,

## 2. CAMERA AND INTERFACE HARDWARE

Figure 1 illustrates the windowing operation of the CCD array. After transferring the image from the CCD image plane to storage plane, a rapid vertical transfer is performed in the storage plane to get to the first line of the window of interest. A rapid horizontal line transfer is then performed to get to the first pixel in the window. The pixels within the window of interest are then read out and processed without being stored in memory, and subsequently a vertical shift is performed to get to the next line in the window. The above process is repeated until all the pixels in the window are read out and processed.

A block diagram of the CCD camera electronics is shown in figure 2. The camera electronics includes the image and storage plane clock drivers, the CCD chip, output amplifier, double correlative sampling to reduce black level fluctuation, and a 12-bit analog to digital converter. Control of the clocking for vertical and horizontal shifts in the CCD array is provided by a TMS320C40 DSP board shown in figure 3. The DSP operating software is loaded in SRAM on the local bus, and the global bus is used for interfacing to the CCD camera and the steering mirror. Figure 4 is the block diagram of the interface electronics between the DSP and the CCD camera and steering mirror. The horizontal line transfer in the CCD output shift register is initiated by a programmable gate array after each vertical shift. A 10-MHZ 512x12-bit first-in-first-out (FIFO) buffer is used to synchronize the CCD readout to the DSP processing. The interface electronics also includes a pair of 16-bit digital to analog converters to provide the pointing control signal to the steering mirror,

The CCD array is controlled by a series of shift pulses applied at the appropriate times. After integration of the light onto the CCD array (timed by the processor), a vertical transfer of the charge is accomplished with a write instruction from the DSP processor. This results in a shift of the charge from the image plane to the storage plane with the number of shifts controlled by a direct memory access (DMA) channel of DSP. After completely shifting the image plane to the storage plane, further vertical shifts in the storage plane position the window area in the horizontal shift register where the data is shifted, double-correlative sampled, and converted to 12-bit digital words corresponding to the accumulated charge. The use of a 12-bit word makes maximum use of the dynamic range and signal to noise ratio of the detector.

The A/D output is amplified with RS 422 drivers and delivered to the interface electronics as a series of 12-bit words with all the data of the CCD line that is being processed. A clock pulse is also delivered along with each pixel word. The interface board is also loaded with a word corresponding to the number of leading pixels that are of no interest. These data words are not written into the FIFO buffer. Only the pixels of interest are read into the FIFO and reading of the FIFO continues until the next vertical shift is requested by the processor.

The DSP completely controls the transfer of CCD data and computes the centroids of the two windows without the necessity of storing the pixel data in RAM. The DSP calculates the point-ahead error based on the transmit and beacon centroids and generates a pointing control signal which is applied to the steering mirror via the two 16-bit digital to analog converters.

A commercial CCD array (Thomson 7863A) with a form factor of 384x288 was used in the camera because of reduced cost. The DSP control of the CCD camera operation that was described above allowed using only a 100x100 area of the array and the windowed-read operation in order to achieve an update rate of up to 2KHz. The CCD camera hardware, DSP processor, interface electronics, and the steering mirror were used in a demonstration of closed loop control of point-ahead angle that is described in reference 2.

### 3. CONCLUSION

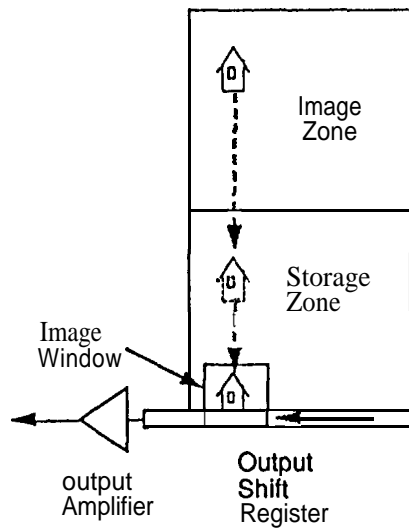
In conclusion, this paper described the development of a CCD camera and interface electronics for a CCD-based pointing control loop.

### 4. ACKNOWLEDGMENTS

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### 5. REFERENCES

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- 1 Transfer image into storage zone
- 2 Rapid vertical transfer until the first line of the window is in the horizontal shift register
- 3 Rapid horizontal transfer until the first pixel to be read is at the output gate
- 4 Read out the desired number of pixels in the line
- 5 Vertical shift when last pixel of the window is read
- 6 Repeat 3-5 for every line in the window

Fig. 1 Windowed operation of the CCD array.

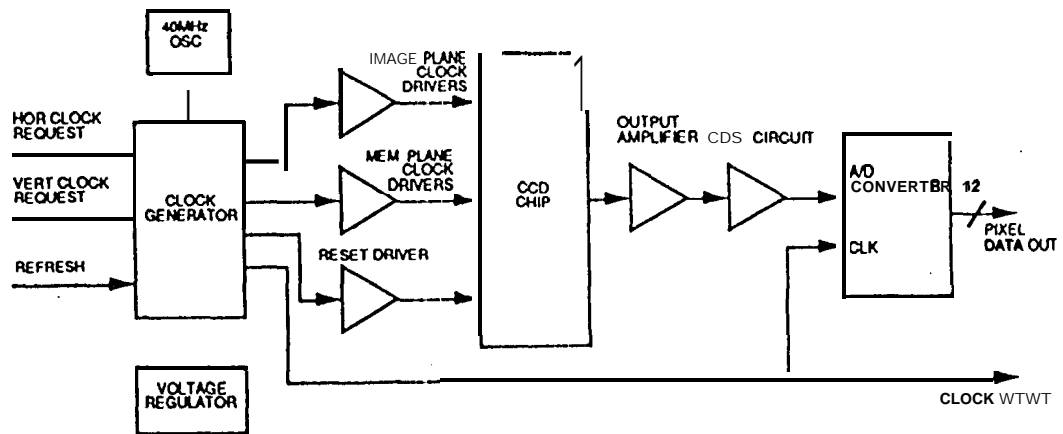


Fig. 2 Block diagram of CCD camera electronics.

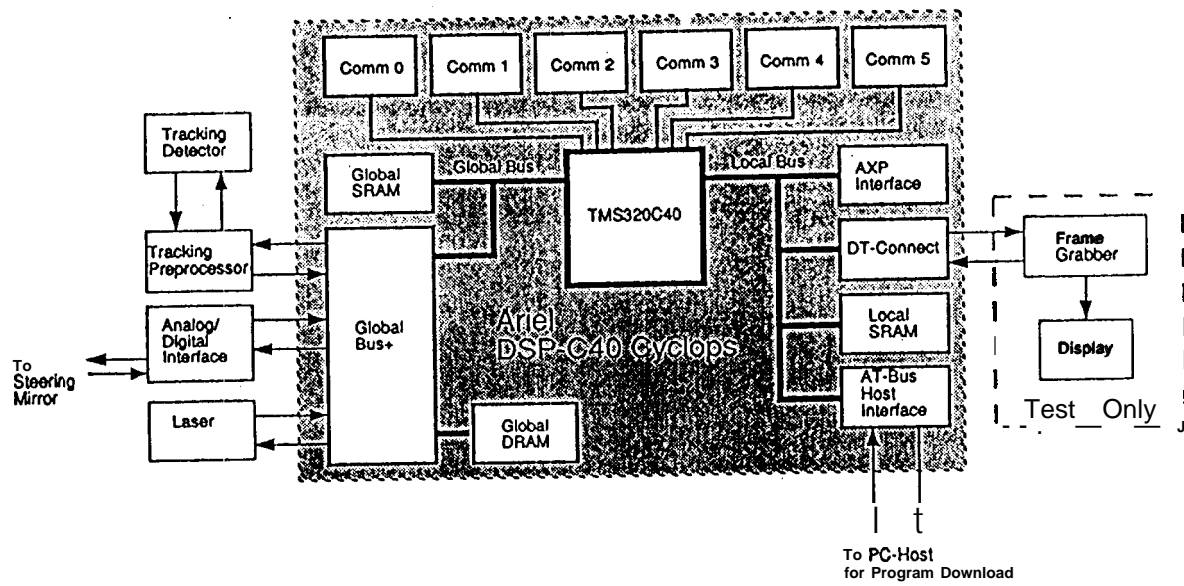


Fig. 3 Block diagram of DSP processor.

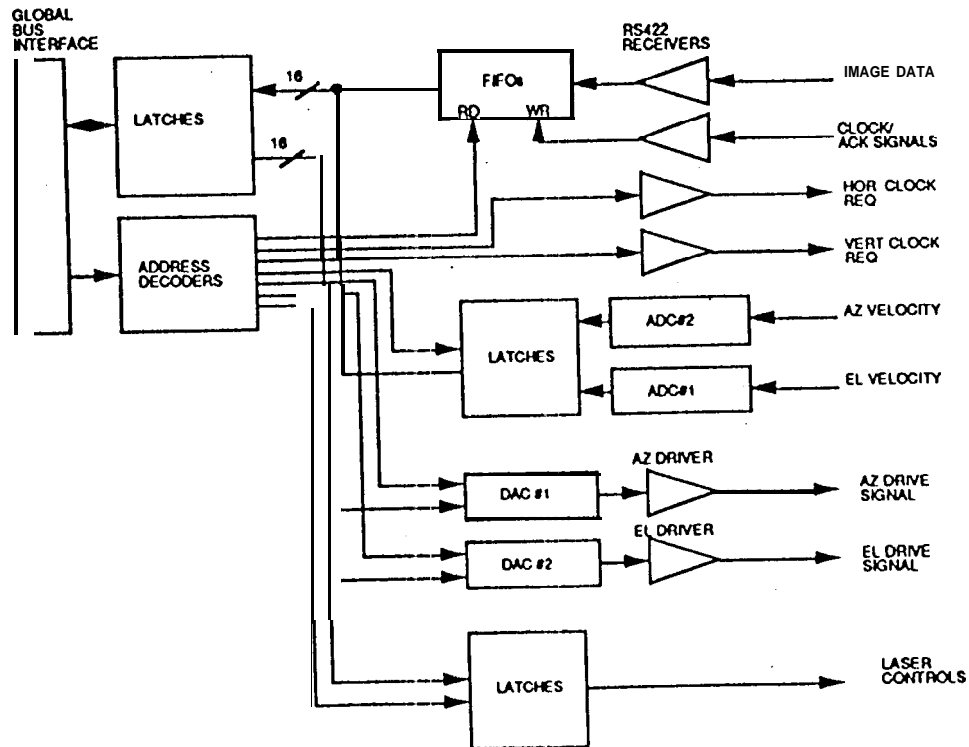


Fig. 4 Block diagram of camera and mirror interface to DSP processor.