

CAPACITIVE EDGE SENSOR DESIGN FOR SELENE SEGMENTED PRIMARY MIRROR

Linda M. Miller, William J. Kaiser, Thomas Kenny and Thomas VanZandt

Jet Propulsion Laboratory, California Institute of Technology, Pasadena, CA 91109

OBJECTIVE

The objective of this project is to produce a proof-of-concept demonstration of an edge sensor for the Space Laser Energy (SELENE) program. The operational specifications are:

$\pm 200 \mu\text{m}$ full range in the z
10 nm resolution in z
 $100 \mu\text{m} \pm 5 \mu\text{m}$ gap width between segments
sign information
30 kHz bandwidth

where z is the direction normal to the reflective surface of the mirror segment. Fabrication cost constraints also require that the edge sensor is affordable, easy to align, and integrable with segment materials. The small dimension of each hexagonal segment (3 cm from flat to flat, 1 cm thick) also requires that the sensor is small,

INTRODUCTION

In the SELENE telescope, the primary mirror design consists of more than 200,000 segments which must be precisely aligned to correct for distortions in the optical train. Because the mirror is segmented, however, phase discontinuities naturally arise from translation differences, Δz , between adjacent segments and normal to the reflective surface of the primary mirror. To minimize these phase discontinuities, sensors can be placed at the edges of adjacent segments to fine tune each segment's position.

The proposed capacitive position sensor is based on a moving plate capacitor design and, based on noise calculations of the circuit design, is capable of resolving displacements of 1 part in 10^5 (0.4 nm for 400 μm full scale). The sensor geometry guarantees a measurement insensitive to gap variations, and all alignments during installation are non-critical. The feedback and output signal circuitry provides a 30 kHz bandwidth and a dc output of the relative translation. The geometry and circuitry design is described here with experimental proof-of-concept using off-the-shelf electronic components and breadboard circuits. Small translations were attempted with a piezoelectric test apparatus. Linearity, sign information and noise measurements are discussed.

SENSOR GEOMETRY

The edge sensor geometry, shown conceptually in Fig. 1, is fabricated on the opposing edges of adjacent mirror segments. In this figure, each rectangle represents a metal electrode, which has been photolithographically patterned onto the insulating segment edge. The overlap of the electrodes corresponds to a parallel sliding plate capacitor scheme as shown schematically in Fig. 2. In the starting null position, shown in the left most portion of Fig. 2, the overlapping areas, A_1 and A_2 , are equal. If however, one segment moves a distance, Δz , with respect to the other segment, then $A_1 > A_2$. By measuring the difference signal, $V \propto A_1 - A_2$, both the sign and the magnitude of the relative translation can be obtained.

Reflective Surface

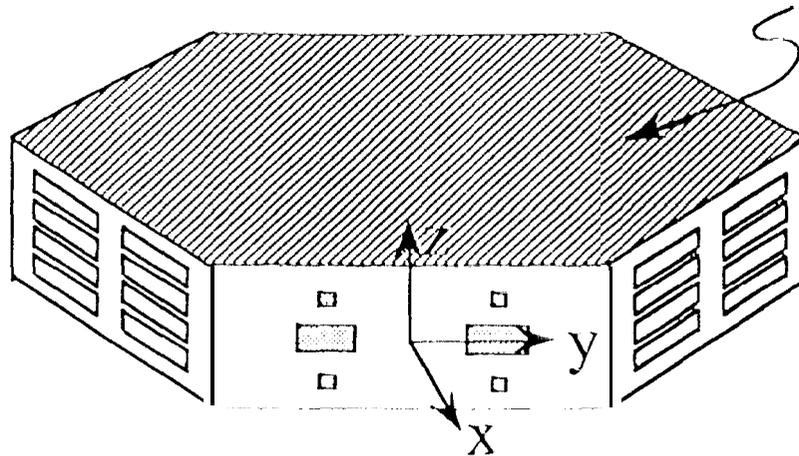


Figure 1. Schematic of single segment of SFLINE segmented primary mirror with implementation of capacitive edge sensors.

It is very important that the signal, V , represents only relative translations in z . Since each segment displacement can include tip, tilt and piston, translations in x , y and rotation around x , y or z must either be eliminated automatically or must be easily measured and fed to the control system for post-measurement correction. The parallel plate capacitors in the four corners of Fig. 2, labeled 1.1, 1.3, R1, and R3, are designed to partially meet these objectives. Because the shaded electrode in each of these respective pairs is small enough to remain within the area of the larger electrode through any translation of the full $\pm 200 \mu\text{m}$, the overlap area of each pair remains constant. Therefore, any change in the capacitance, of these electrode pairs is a direct result of changes in the gap spacing between the adjacent mirror segments. For example, rotation around the z axis would result in an output signal proportional to

$$C_{1.1} - C_{1.2} = \epsilon_0 A \left(\frac{1}{d_{1.1}} - \frac{1}{d_{1.2}} \right) \quad (1)$$

where C is the capacitance, ϵ_0 is the permittivity of free space, A is the overlap area (equal for all four corners of the electrode configuration), and d is the gap spacing between the electrodes. Likewise for rotation around the y axis,

$$C_{1.1} - C_{1.3} = \epsilon_0 A \left(\frac{1}{d_{1.1}} - \frac{1}{d_{1.3}} \right). \quad (2)$$

Signals proportional to the capacitance differences in Eqs. 1 and 2, are fed to the control system and must be used in the final analysis of the z translation measurement. This is not, however, a disadvantage since this information can be useful in the fine tuning of the entire mirror assembly.

Rotation around the x axis was discounted in the early proposal stages of this design since this rotation is expected to be insignificant. In the first design stage of this project the shaded electrodes in Fig. 2 were round to accommodate rotations around the x axis. However, by utilizing a rectangular geometry, linearity is improved.

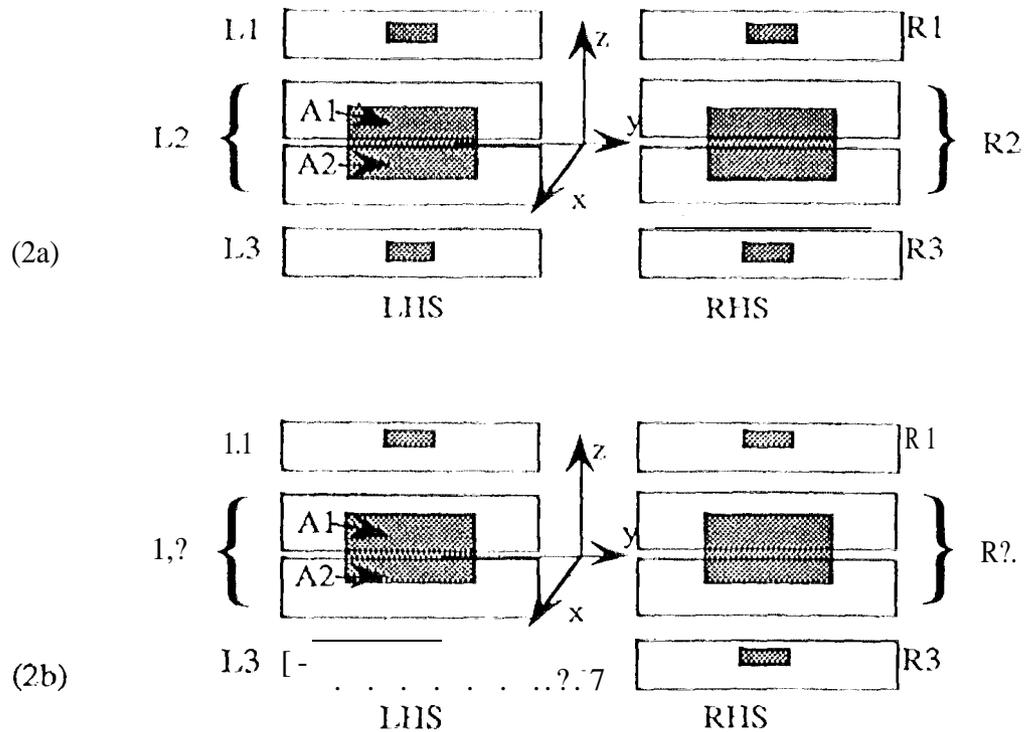


Figure 2. Schematic of capacitive edge sensor at (2a) null position ($A_1 = A_2$) and (2b) with relative translation, Δz ($A_1 > A_2$).

In addition to rotational information, the edge sensor measurement must be insensitive to translation along the x and y axes. Immunity from gap spacing variations, i.e., x translation, is inherent in the difference measurement which will be discussed in detail in the next section on drive circuitry. Translation along the y axis is irrelevant since the y dimension of the shaded electrodes is chosen such that the largest y translation] dots not change the overlap areas of any of the sliding plate pairs.

In summary, the electrode configuration in Figs. 1 and 2 provide a relative z translation measurement between adjacent segments which includes sign information (i.e. which segment is "higher") and which is immune to other Notational or translational variations. The circuit design is discussed next.

CIRCUIT DESIGN

In the capacitive edge sensor, the primary measurement is that of the capacitance difference from the center sliding plate capacitors labeled L2 and/or R2 in Fig. 2. (L2 and R2 are redundant measurements.) The relative z positions of adjacent segments is therefore reliant on the precise measurement of very small changes in capacitance. For example, electrode dimensions which would fit comfortably on the edge of a 1 cm thick hexagonal segment, 3 cm from flat to flat, might be:

Electrode Description (Ref Fig. 2)	Dimension (cm ²)	Overlap Capacitance (pF)
L1, L3, R1, R3-white rectangles	0.74 x 0.82	
L1, L3, R1, R3-shaded	0.16 x 0.74	1.05
L2, R2-white	0.24 X 0.82	
L2, R2-shaded	0.195 x 0.74	1.28

where the overlap capacitance corresponds to the overlap between approximately half the area of the shaded electrode and one of the white electrodes in Fig. 2. Changes of 10 nm in a $\pm 200 \mu\text{m}$ span then correspond to a change in C for L2 of -10.5 pF . This value is much smaller than most stray capacitances common in even the quietest circuit designs. To achieve this task the circuit block diagram, shown in Fig. 3, is used to implement the measurement. In the first stage of this circuit, the capacitances, C1 and C2, which correspond to the overlap areas, A 1 and A2 respectively, are converted to a voltage. The C to V transfer function is designed to eliminate the effects of stray capacitance and resistances as well as the effect of temperature variations if optimized. This will be clarified briefly. The voltages V1 and V2 are directly proportional to C1 and C2, such that the ratio between the difference and the sum of these signal results in the signal:

$$\frac{V1 - V2}{V1 + V2} \propto \frac{C1 - C2}{C1 + C2} = \frac{\epsilon_0 y}{d} \frac{(z1 - z2)}{(z1 + z2)} \quad (3)$$

Note that variations in the gap spacing between adjacent segments has been completely eliminated in the limit that $y, z \gg d$. Also note that the measurement is immune to variations in air quality, i.e. ϵ_0 drops out as well.

Due to symmetry, the sum of the z positions in Eq. 3 remains constant. Therefore, the summation signal can be fed back into the feedback loop and compared to a set reference level corresponding to the calibrated value of the sum. This method relaxes requirements on the fabrication since the reference value can be set by simply laser trimming a resistor value prior to operation of the primary mirror.

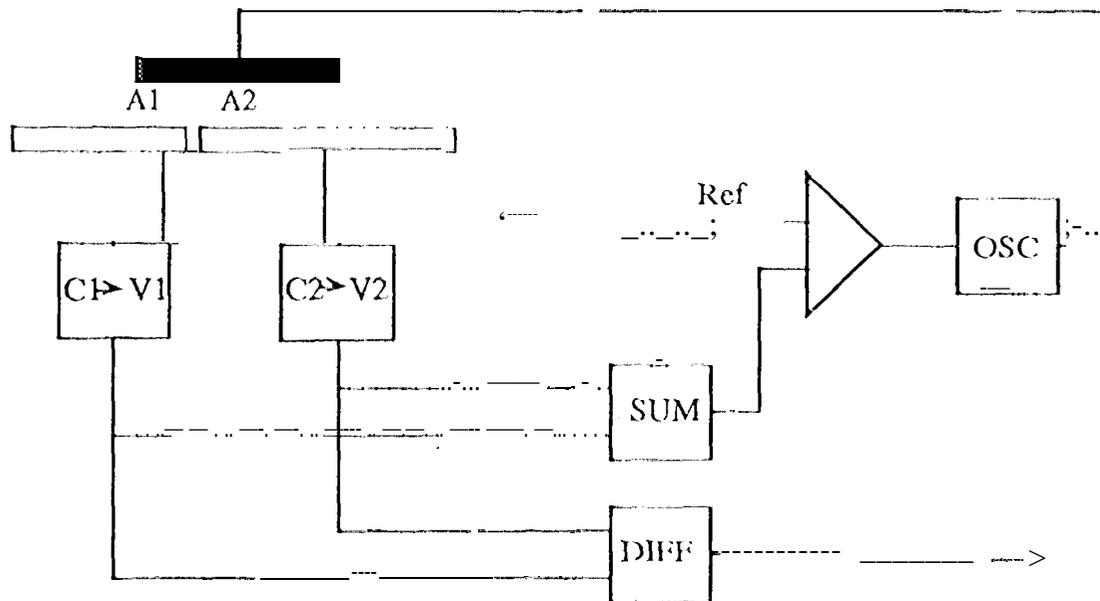


Figure 3. Circuit block diagram for capacitive edge sensor. This circuit produces a difference measurement corresponding to the relative z positions of two adjacent mirror segments.

The C to V converter is shown schematically in Fig. 4. A square wave signal, V_{osc} (0 to $-SV$), is fed into the common electrode of the sliding plate capacitor of Fig. 3. The opposing electrode with overlap area, A 1, is then connected to the inverting input of the virtual ground circuit with feedback capacitance, C_f . The output from this circuit is:

$$V1 = - \frac{C1}{Cf} Vosc. \quad (4)$$

Note that this transformation is directly from capacitance to voltage with no dependence on drive frequency. Also note that if the temperature coefficients of C1 and Cf are matched, then effects of temperature variation are also eliminated automatically. The most interesting feature of this design, however, lies in the virtual ground aspect: any stray capacitances or resistances to ground between the measured capacitance and the op amp are effectively shorted to ground. This allows for the precise measurement of very small capacitances. The limiting factor in determining the resolution of this design lies in the input offset voltage noise of the op amp.

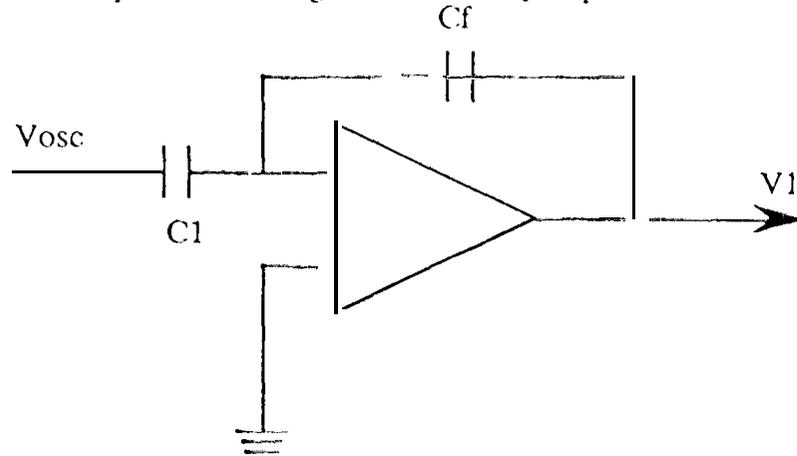


Figure 4. Schematic diagram of C to V converter for capacitive edge sensor design.

A detailed schematic of the C to V converter is shown schematically in Fig. 5. A CMOS switch is added in parallel with the feedback capacitor to discharge the capacitor during the low portion of the square wave pulse. The clock used to control this switch is synchronous with the drive signal. The sample and hold operation occurs after the initial integration, with the modified inverse clock signal (modified to eliminate extraneous switching noise of the switch used in the prototype) which has a shorter pulse width than the clock signal. The voltage follower acts simply as a buffer for the C to V converter.

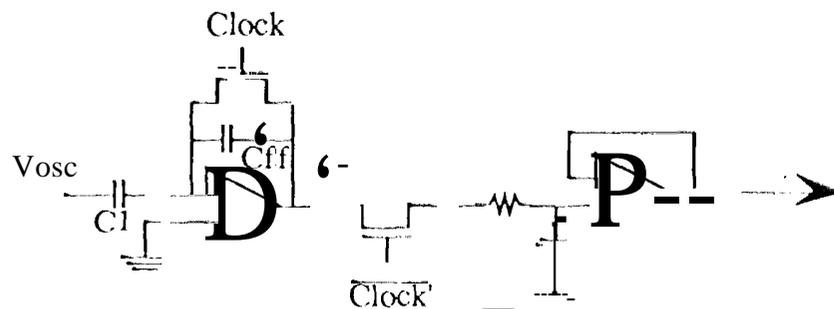


Figure 5. Schematic diagram of C to V converter stage including sample and hold circuitry.

In summary, the circuitry described in the section converts a precise measurement of a high impedance capacitance difference signal to a low impedance drive voltage by utilizing a virtual ground C to V converter input stage and a feedback controlled drive signal amplitude. This design results in the precise measurement of very small capacitances while eliminating stray capacitance and resistance effects. The optimized implementation of this circuit also provides measurements immune to temperature variations. The output signal is insensitive to changes in the gap spacing

between adjacent segments, and immune to environmental changes which result in changes in the permittivity. A prototype sensor and circuit are described in the next section.

EXPERIMENT / RESULTS

The experimental demonstration of proof of-concept for the capacitive edge sensor was carried out in two parts. In the first part, air gap capacitors were used to simulate the overlap capacitances described in the previous section. The linearity and noise spectra of the circuit were evaluated. In the second part of the experiment, a silicon micromachined sensor was fabricated and assembled on a bimorph test fixture to analyze the feasibility of this type of sensor design.

A photograph of the prototype breadboard circuit and sensors is shown in Fig. 6. This circuitry contains its own square wave generator, a feedback loop to control the amplitude of the square wave from the sum of the capacitance values and the demodulation circuitry to produce a difference output. This circuitry is composed strictly from off-the-shelf components. All op amps are of the 3140 variety, although improvements in noise spectra could be achieved by using low noise electronics. The air gap capacitors are located on the breadboard in the bottom right of the photo. This placement was necessary to access the adjustment screws of the air gap capacitors. In the bottom center portion of the photo is the micromachined sensor and bimorph test fixture. On the left breadboard, outside of the chassis box, is a circuit enhancement added later in the design to modify the pulse width of the inverted clock pulse of the C to V converter stage.

Circuit Response

During this stage of the proof-of-concept demonstration, the air gap capacitors were connected to the breadboard circuitry and the difference output signal was monitored using first a digital voltmeter for linearity and sign information measurements, then to a spectrum analyzer for noise spectra analysis. Prior to the linearity and sign information demonstration, each air gap capacitor was measured with a calibrated capacitance meter. The air gap capacitors were then connected to virtually identical input stages, shown schematically in Fig. 7 (air gap capacitors are labeled CL and CR), and adjusted to their smallest capacitance values. The output signal was zeroed using one of the potentiometers on the left of the grounded chassis box. Capacitance values and output signal levels were recorded after each capacitance adjustment. The circuit showed excellent linearity for all values of capacitances. Sign information was also demonstrated as expected, i.e. for $C_L > C_R$, V_{diff} was positive, and for $C_L < C_R$, V_{diff} was negative.

Note that the air gap capacitors in Fig. 7 are connected in parallel with a 100 pF capacitor. This configuration was designed to produce a gain of -1 in the C to V converter stage while simulating small changes in the overall capacitance value. In the actual capacitive edge sensor, the feedback capacitor would be matched both thermally and numerically to the sensor overlap capacitance.

The noise spectra for this circuit is shown in Fig. 8 for frequencies up to 25 kHz. From this figure, the estimated noise is 150 μ V for a 30 kHz bandwidth. To achieve 10 nm resolution over a 400 μ m full range with a ± 15 V output signal, the noise floor required is 750 μ V which is well above the noise floor obtained in this measurement.

This circuit was also analyzed for noise contributions due to pick-up effects expected from the long, unshielded signal lines near the oscillator and the large, unshielded potentiometers. The drive and output signals for this circuit are shown in Fig. 9. This measurement was taken up to 100 kHz, beyond the 50 kHz drive frequency and the 30 kHz circuit bandwidth. Note that the large peaks in the drive signal are also reflected in the output signal, indicating a large level of pick-up. This noise can be minimized by optimizing the circuit layout, replacing the potentiometers with laser trimmed resistors and by replacing the breadboard with a printed circuit board and ground plane.

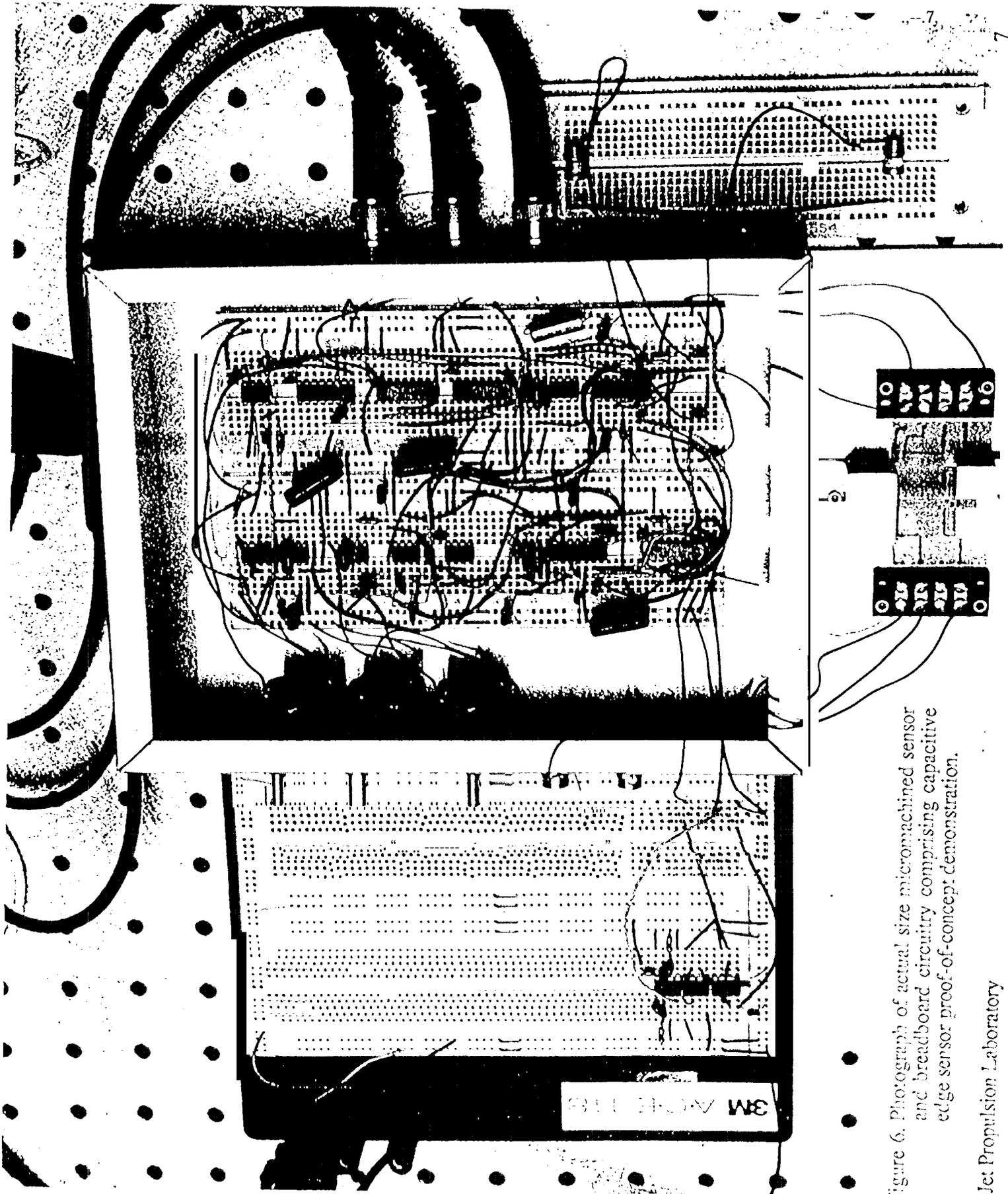
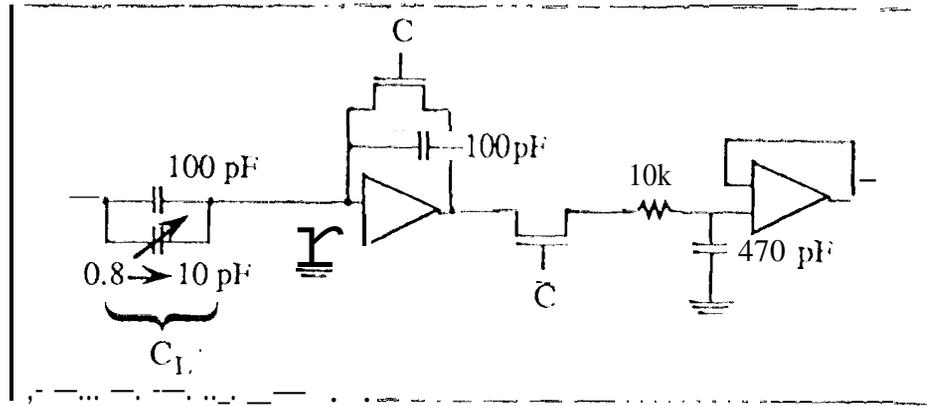


Figure 6. Photograph of actual size micromachined sensor and breadboard circuitry comprising capacitive edge sensor proof-of-concept demonstration.

$C \rightarrow V$



$C \rightarrow V$

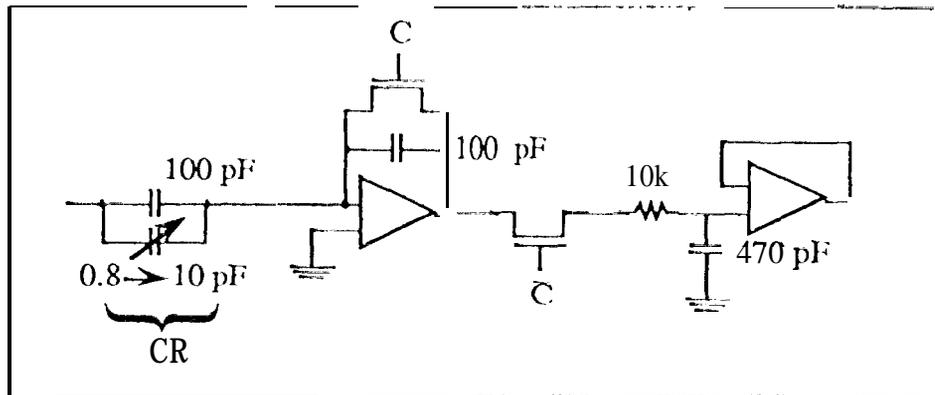


Figure "i. Schematic diagram of C to V converter stage including sample and hold circuitry and air gap capacitors, C_1 and CR.

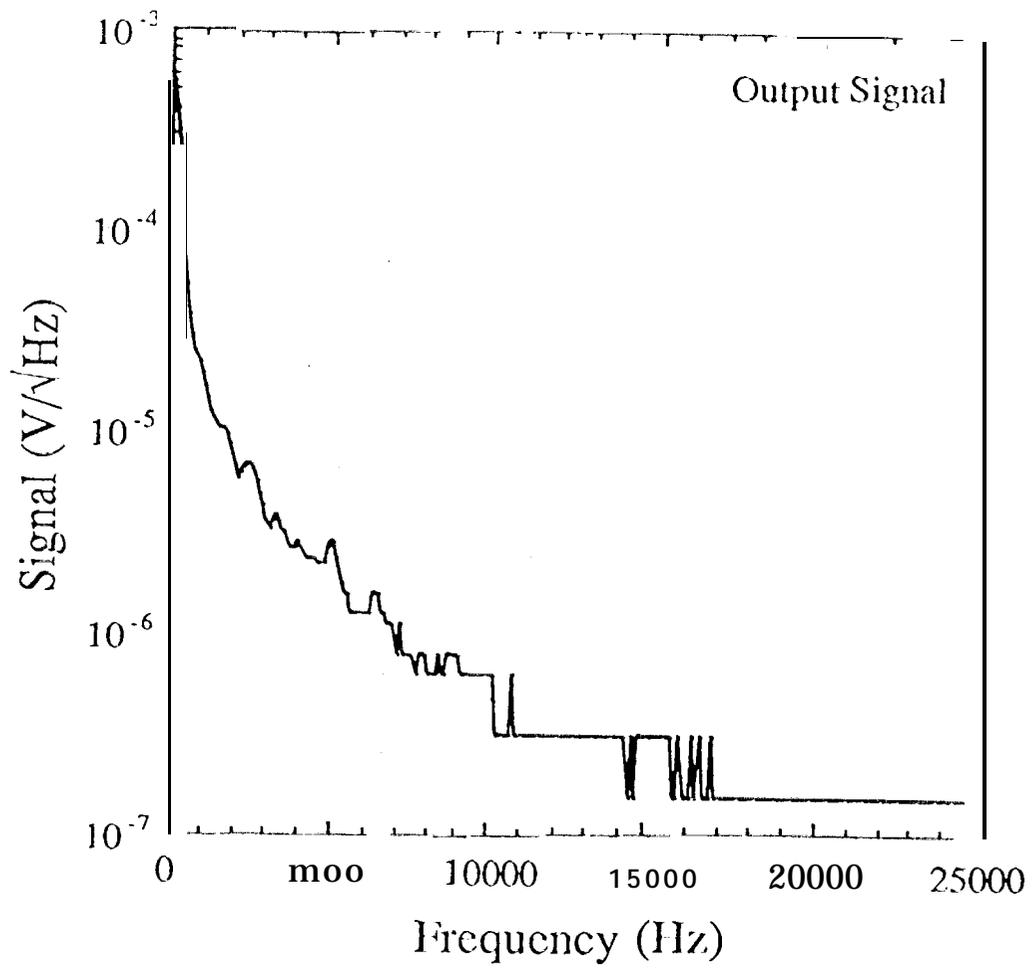


Figure 8. Noise spectrum for difference output signal of prototype capacitive edge sensor.

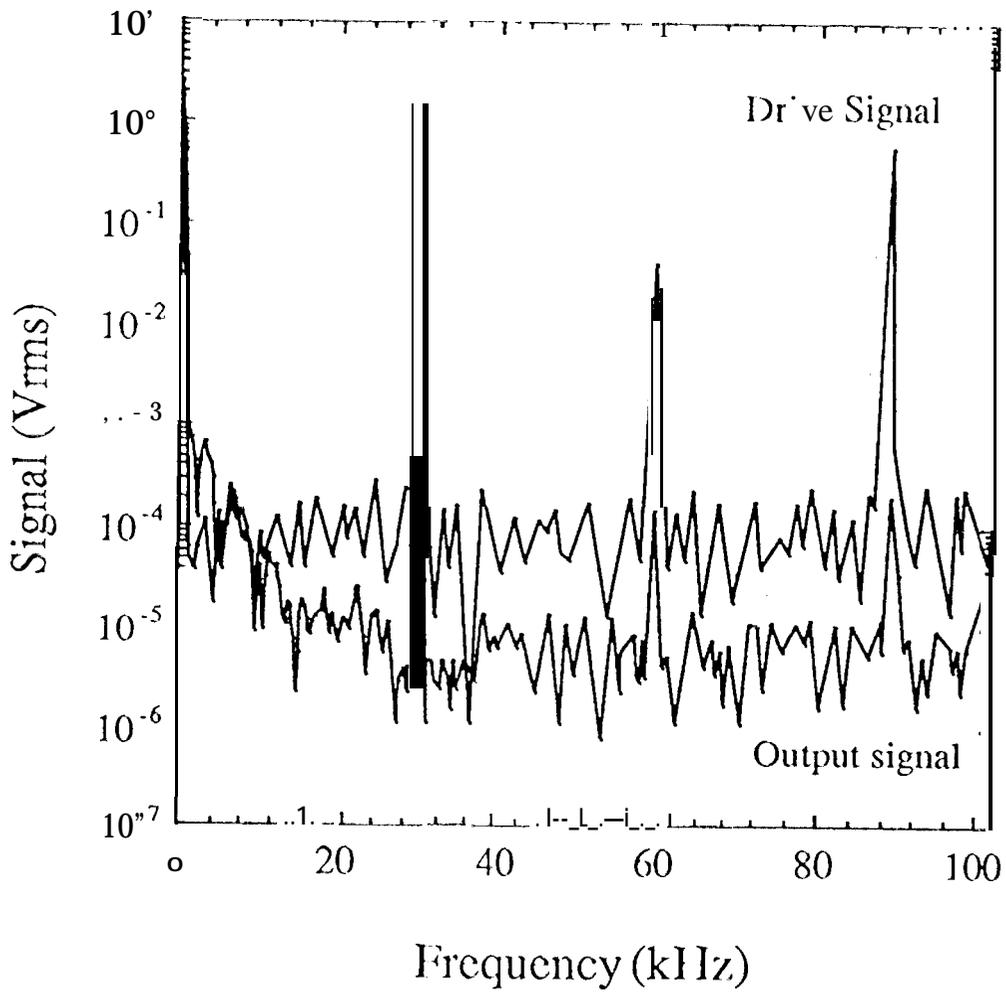


Figure 9. Drive and difference output signal for capacitive edge sensor prototype.

Sensor Fabrication

During this stage of the proof-of-concept demonstration, a silicon micromachined sensor was fabricated and assembled with a bimorph test fixture shown in the photograph of Fig. 10. The metric ruler in the foreground is included for size reference. The vertical dimension of the electrodes was exaggerated in this design for ease of alignment.

The sensor was fabricated using standard photolithography, metallization, and micromachining techniques. A thick silicon dioxide (SiO_2) layer, $\sim 1 \mu\text{m}$, was first grown on the bare silicon wafer for isolation of the electrodes. The electrodes were then formed by standard photolithography, metallization and lift-off techniques. Finally, the individual sensors were cut to size using bulk micromachining. The color difference between the two sensor halves shown in Fig. 10 is due to the fact that the sensor halves were fabricated on separate wafers with a slightly different oxide thickness.

The sensor is shown mounted on a bimorph test fixture in the photograph of Fig. 10. The cross-section of this configuration is shown in more detail in Fig. 11. One half of the sensor is mounted to a grounded aluminum block for shielding purposes, while the other half of the sensor is mounted on the end of a bimorph strip. When a bias is applied across the top and bottom surfaces of the bimorph, a translation in z occurs on the order of $0.65 \mu\text{m}/\text{V}$ for small translations. For larger applied voltages, a change in the gap spacing also occurs. For example, at 100 V applied bias, $\Delta d/d = -10\%$ where d is the gap spacing and Δd is the change in gap spacing at the upper or lower edge of the sensor. This variation is neglected in the following measurement since it is within the measurement error. The gap spacing was set at $\sim 100 \mu\text{m}$ by inserting thin filter paper between the sensor halves and then adjusting the separation of the two aluminum blocks.

The electrode dimensions are:

Center Electrode: 6 mm X 6 mm
Opposing Electrodes: 8 mm X 10 mm

The corresponding overlap capacitances are $C_{1,2} = 1.593 \text{ pF}$. For a resolution of $\Delta z = 10 \text{ nm}$, $\Delta C = 8.85 \times 10^{-7} \text{ pF}$ where

$$\frac{\Delta C}{C} = \frac{\Delta z}{z} \quad (5)$$

The connection to the C to V converter stage is similar to that of the last section and shown schematically in Fig. 12.

The difference output for this configuration was again monitored first on a digital voltmeter and then on a spectrum analyzer. Sign information was obtained successfully. However, the noise floor of the drive/sensing circuitry increased significantly with the bimorph test fixture connected. For a 100 V applied bias, the difference output voltage was measured at 550 mV, with a signal to noise ratio of ~ 5.5 . This corresponds roughly to a resolution of $\sim 12 \mu\text{m}$. This noise level is considerably higher than that measured with the air gap capacitors for several reasons. The primary cause of noise in this configuration is the coupling of environmental factors into the long bimorph cantilever arm. Most of the noise observed was at low frequencies which we interpret as contributions from air currents and other accelerations of the bimorph arm. The second major cause of noise in this experiment was the coupling of noise into the long wires of the test fixture. The wires connecting the sensor to the breadboard circuitry are composed of bare gold wires, painted silver traces and long unshielded solid wires over the edge of the chassis. All of these contributions could be eliminated with the proper (micro) technology.

CONCLUSIONS

In summary, the proof-of-concept demonstration of the capacitive edge sensor was successful. Excellent linearity and sign information was obtained by using air gap capacitors. The noise floor of the breadboard circuitry was sufficiently low enough to resolve a 10 nm relative z translations in a $40 \mu\text{m}$ full range application. Demonstration of the actual size silicon sensor was also successful. The silicon micromachined sensor produced sign information and reasonable linearity within the constraints of the test fixture limits. The noise floor, however, increased due to

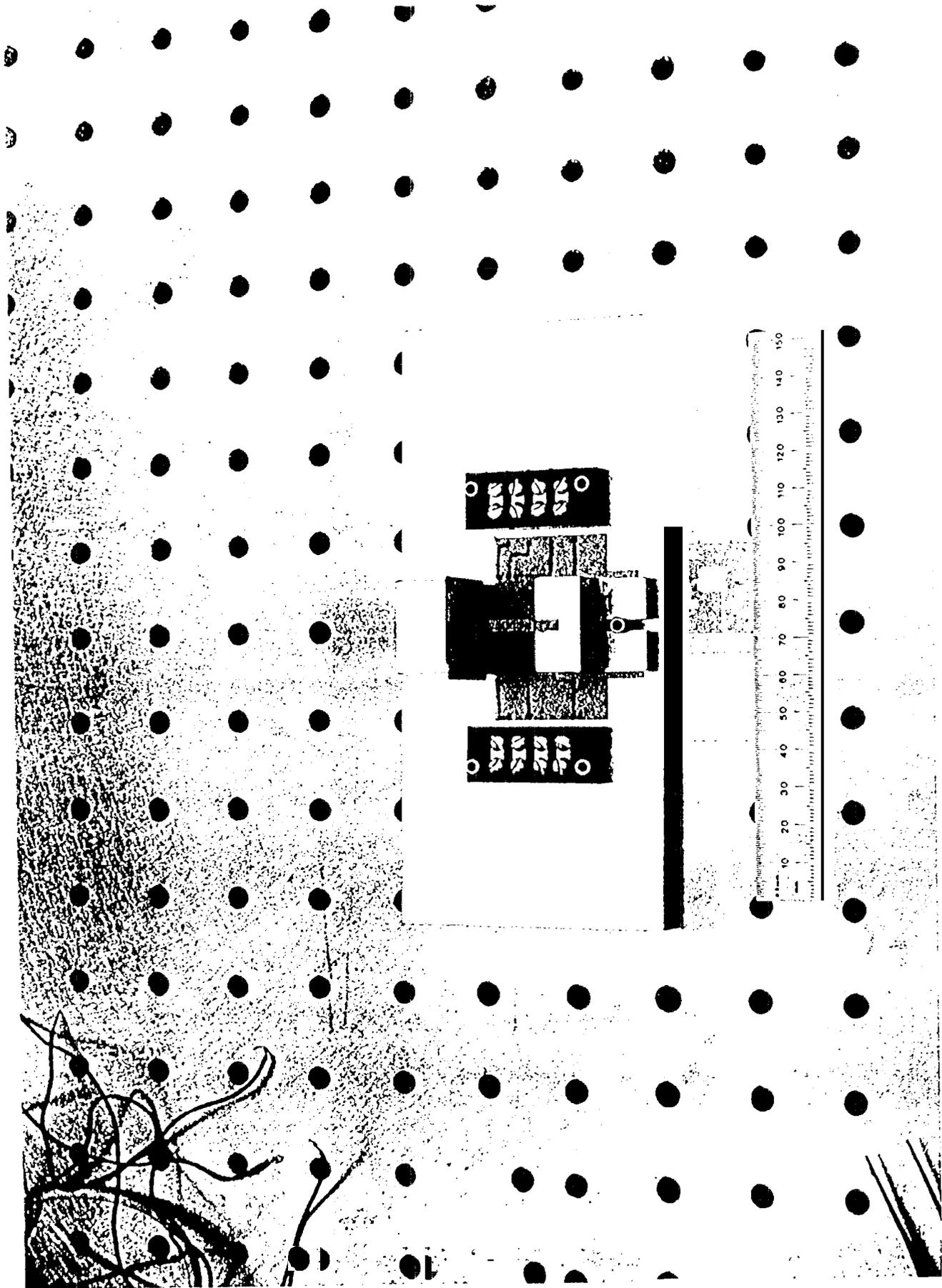


Figure 10. Photograph of silicon edge sensor and bimorph test fixture.

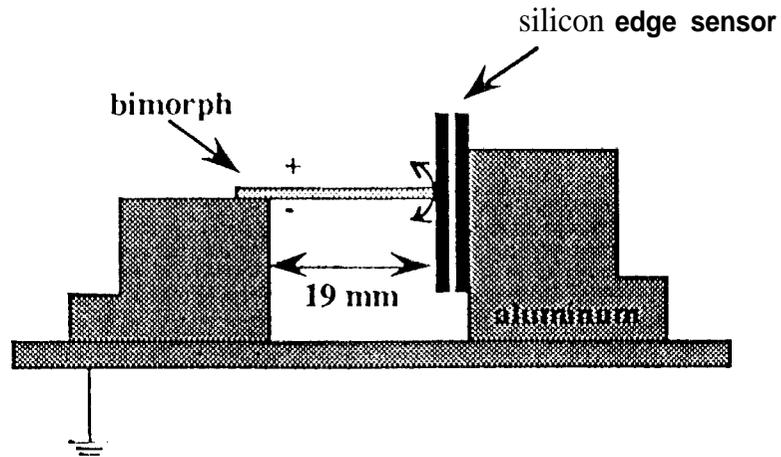
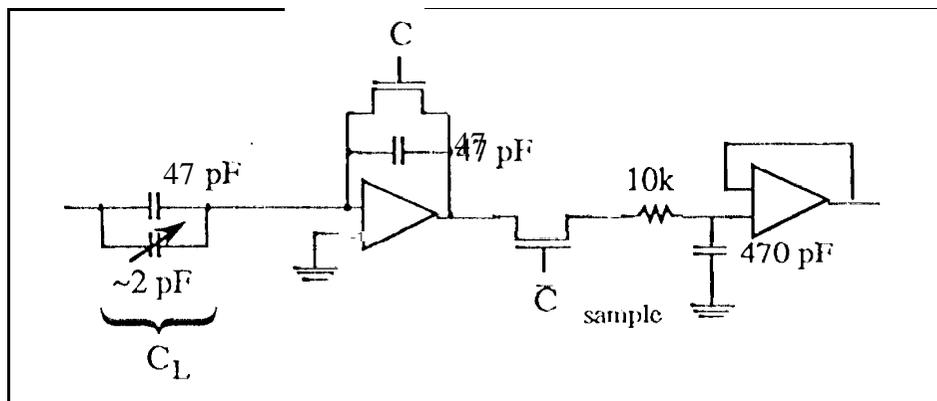


Figure 11. Cross-sectional schematic of a pair of silicon edge sensor electrode arrays mounted on a bimorph test fixture.

$C \rightarrow V$



$C \rightarrow V$

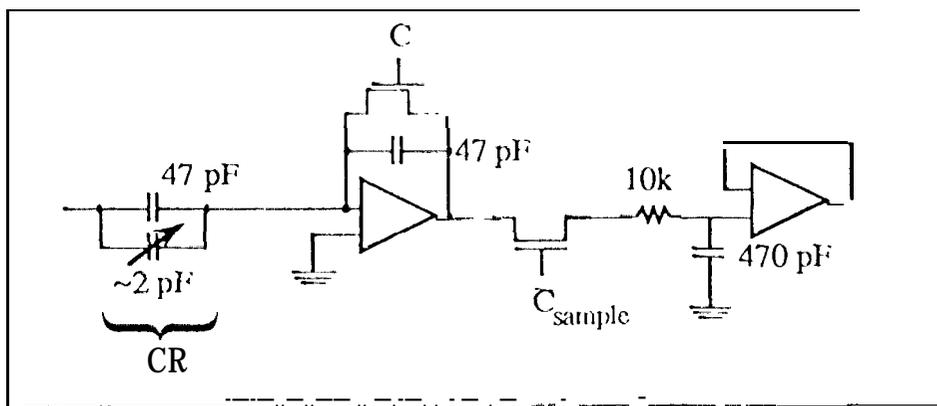


Figure 12. Schematic diagram of C to V converter stage including sample and hold circuitry and micromachined sensors,

extraneous coupling of environmental and **signal** noise through the mechanical and electrical extremities of the test **fixture**. Improvements in the test **fixture** design to eliminate these contributions include improved electrical shielding and vibration isolation. Ideally, the **circuitry** would best be tested by configuring an actual sensor into a **SELENE testbed**.

The next logical step in the development of the capacitive edge sensor is to modify the breadboard circuitry to improve the noise floor. This can be accomplished by optimizing the chip layout, replacing the breadboard with a printed circuit board, and by replacing the off-the-shelf op amps with low noise op amps. Ultimately, the C to V converter must be fabricated as close to the sensor electrodes as possible, possibly in a hybrid configuration. The feedback capacitor in this circuit stage must also be thermally matched to the sensor overlap capacitor. Finally, the next generation of the sensor must be fabricated to incorporate tip/tilt measurements and should ideally be tested on a primary mirror cluster testbed. This will provide the opportunity to test the sensor and circuitry using a wide bandwidth test fixture. We expect these next generation modifications to fully demonstrate the superior resolution and sensitivity capabilities of the capacitive edge sensor in the SELENE segmented primary mirror.

ACKNOWLEDGMENTS

The research described in this paper was performed by the Center for Space Microelectronics Technology, Jet Propulsion Laboratory, California Institute of Technology, and was sponsored by the National Aeronautics and Space Administration, Guidance and Controls RTOP.