

Solid State Memory Study Final Report

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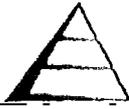
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EXECUTIVE SUMMARY

Existing and future solid state nonvolatile memory technologies are described and evaluated in this report. Solid state memory technologies can offer size, speed, power, weight, and ruggedness advantages over conventional moving media storage technologies such as disk or tape. The nonvolatile solid state technologies considered in this report are magnetic bubble, vertical Bloch line (VBL), magnetic core, plated wire, optical holographic, two photon three dimensional optical, spectral hole burning, magnetoresistive random access memory (MRAM), Josephson junction, single electron, flash electrically erasable programmable read only memory (FLASH), ferroelectric random access memory (FRAM), and chemical or molecular. This technology list is not all inclusive, but rather is a broad sampling of past, present, emerging, and future solid state memory technologies.

Magnetic bubble, plated wire, and magnetic core memory are mature and being used in niche applications at present. These technologies offer limited opportunities for improvement. VBL, optical holographic, and MRAM offer the promise of near term improvements in cost and storage density with low development investment. FLASH, battery backed up SRAM, and FRAM are technologies that appear to be controlled by large commercial investments and offer the government little opportunity for influence or small scale investment at this time. Josephson junction, single electron, two photon three dimensional optical, spectral hole burning, and chemical or molecular memories offer the long range hope of improved memory, but these will require significant effort and investments over long time periods to become technically feasible.

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1 INTRODUCTION

The purpose of this report is to summarize the results of an eighteen month research study at the National Media Laboratory (NML). The study was undertaken to identify, understand, and evaluate new and emerging nonvolatile solid state memory technologies. Solid memory in the context of this report means that there are no mechanical moving parts. An examination of the state of commercial data storage technology today reveals the emergence of new solid state memory technologies into the market place. Examples of such new technologies are battery backed up static random access memories (SRAM), flash electrically erasable read only memories (EEPROM), ferroelectric random access memories (FRAM), magnetoresistive random access memories (MRAM), and holographic optical memories. These and other technologies were and are being investigate] at the NML by a group of seven people. The study is organized by the physics of the device. Written reports describing the various types of storage technologies follow this introduction.

The purpose of the study is to identify the solid memory technologies that are under development or emerging in the world today. This was accomplished in two overlapping phases. First, in the search phase, literature searches as well as university visits and conference attendance were used to gather information. Second, in the evaluation phase, technologies and candidates from the first phase were listed in a matrix listing time to maturity, cost, risk, and benefit. The purpose of this matrix is to facilitate choosing evolving technologies for different programs of interest to the government.

This report is the combined work of Gary Ashton, Robert Lorentz, Joe Skorjanec, William Mitchell and Roy Callaby of 3M; Dan Dahlberg of the University of Minnesota as a consultant to NML.; and Romney Katti of the Jet Propulsion Laboratory (JPL).

This report is the second and final report generated as part of this study and is based on the first report titled "Solid State Memory Study Mid-Term Report." The optical holographic storage technology section in this report includes an addendum describing new developments. Other differences between the two reports include the addition of new references or insights into the technology gained during the last half of this study as well as two new sections on spectral hole burning and photon echo technologies. In addition, the new reference list at the end of this report includes articles comparing the technologies as well as articles of a more general nature which describe the specific technologies. This report also contains more analysis of the technologies.

Information about storage capacities presented in this report is expressed in Megabytes (MB) rather than Megabits (Mb). One Megabyte equals eight Megabits. This unit was used because commercial end users usually specify their requirements in Megabytes even though some technology areas such as integrated circuit technology use units of Megabits. For instance, a PC user will purchase so many Megabytes of disk, tape, or RAM storage. This makes it much easier for the end user to make a comparison to familiar items and relate to the results in this report. In addition, it allows a consistent comparison of technologies by using the same units in each technology discussion.

2 ELECTRICAL TECHNOLOGIES

2.1 Non-Volatile Semiconductor Memories

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2.1.1 Introduction

Semiconductor memory began displacing magnetic core memory in computers in the early 1970's. The inability of these memories (RAM) to retain data after power has been turned off initiated a quest for non-volatile memory. Designers dreamed of the ideal non-volatile memory which would offer high density and low cost, be infinitely and randomly rewritable at static-RAM speeds, and have dynamic-RAM capacity. All memory technologies demand some concessions from users and the many ROM and RAM solutions were implemented with increased cost and volume penalties.

A review of the types of semiconductor memories in use, their basic operation, and acronyms and definitions is useful in charting the progress and development of several memory types and to relate to the progress in achieving non-volatile memories (Cheng Ming Hu 1991). These are:

ROM: Read -Only Memory; content is determined by the masks of the chip making process. Typically used for video games, font cards, and other non-changeable information. Very low cost per bit.

PROM: Programmable Read-Only Memory; similar to ROM's, except that the user can electrically program the memory one time.

EPROM: Electrically Programmable Read Only Memory; a UV erasable hot-electron programming memory. Non-volatile, but long erase times and window necessary for UV erase pose difficulties. Fast read cycle, high density, few erase/read cycles.

EEPROM: Electrically Erasable/Programmable Read Only Memory; programmable by Fowler-Nordheim tunneling in which electrons tunnel through a thin dielectric to/from a floating gate and to/from a conducting channel. Erasable byte by byte so writing speed is relatively slow.

2.1.2 EEPROM or Flash Memories

The first paper discussing the concept of using a variation of the EEPROM technology and calling it a Flash EEPROM appeared in 1984 (Cheng Ming Hu 1991). This led to the evolution of megabit devices in only five years. The design of the FLASH memory incorporates the floating gate of the EPROM and hot electron injection for the write process; with Fowler-Nordheim tunneling for the erase process. The charge injection process removes or adds electrons from the floating gate. This floating gate provides a gate voltage similar to a single gate transistor, providing logic ones or zeros. The cell volume is about the size of an EPROM, and the chip layout involves the erase of a section on the chip (unlike the bit by bit erase of the EEPROM). This rapid erase results in the name FLASH. This design now approaches the read and write speeds of DRAM and SRAM with the additional feature of non-volatility.

FLASH appears to be the ideal non-volatile solid state memory, however, there is a concern about the number of read and write cycles possible. The very thin layers involved (especially the tunnel oxide) eventually lose their capability to retain a charge. As fabrication processes improve, better quality films are being produced and the cycle endurance appears to be increasing. Higher density products at 16Mbit have been introduced and are available now. New product designs feature 3.3 Volt operation for low power consumption.

2.1.3 Ferroelectric Random Access Memory or FRAM

Because of concerns about the longevity and stability of the thin, floating gate oxide, research continued on finding other approaches to non-volatile memory. One approach replaces the thin oxide used for charge storage in a RAM chip with a ferroelectric material.

The ferroelectric effect is the tendency of dipoles within certain crystals to spontaneously polarize (align in parallel) under the influence of an applied electric field and remain in a stable position after the electric field has been removed. Reversal of the field causes polarization of the dipoles in the opposite direction. These two stable polarization states can be considered a bistable capacitor capable of storing digital data. A substantial amount of research has produced quality films of a complex ferroelectric material and replaced the conventional capacitor in a standard DMM with this material. Reported endurance or cycle capability is substantially higher than that of FLASH or EEPROM (as much as a factor of ten thousand). Areal densities have not yet approached those of conventional RAM, but developments are promising (AMD, Hitachi, and Ramtrom vendor literature). Current products

are available at 16Kbit densities, with 1Mbit devices projected in about three years (Ramtrom 1993). FRAM technology appears to be about three generations behind FLASH, but the companies involved are optimistic that they can catch up (Ramtrom 1993).

2.1.4 Assessment

There continues to be rapid development of both FLASH and FRAM technology. Manufacturers of FLASH are now producing and designing second and third generation products. Much effort is centered on chip layout for various applications. Large driving forces in the market exist to produce chips which appear to a computer as a "magnetic hard disk." However, there are substantial other applications that could result in tremendous market size. Projected applications are:

1. Low density memories for TV, auto's, etc. Anyplace where a low cost non-volatile memory is used. Use will expand with availability.
2. Microprogram control is ranked by some estimates to have the greatest market potential. Examples of this are: BIOS and operating system on a chip, allowing instant boot up and updatability; fonts for printers; updatable control and storage in instrumentation, i.e. meters; and "Smart" instruments. The bulk of current FLASH products are sold as individual memory devices (Electronics 1993).
3. Radiation hardened applications.
4. Solid state "disks" (*Computer Design* 1992; *IEEE Spectrum* 1989, 1992) as a replacement for rotating magnetic hard disks. Potentially a large market, but very price sensitive and costs of solid state memory are projected to be always three to five times the price per megabyte of rotating magnetic memory. In some, or even many applications of small hand held computers, the small size, shock resistance, and non-volatility will be of primary importance and result in large markets.
5. New markets. Discussions with vendors have indicated that they are pursuing applications where traditional rotating memories have not been used. The feeling is that whole new market areas will open up with the greater availability of solid state memories, particularly in the PCMCIA format.

The shortages of 1993 (*Computer Design* 1993) have disappeared and production is dominated by Intel and AMD. There is room for new companies to enter the market, since projected demand is very high. A variety of FLASH memory products are available. Higher density chips (16 Mbit)

have been introduced, and density is expected to double to 32 Mbits soon (Electronic *Design* 1993). Lower power chips (3.3 V) for the mobile computing market are available and will probably dominate markets because of power considerations.

Growth in PCMCIA cards for disk replacement in mobile computing is accelerating. Two forms of FLASH architecture (block or serial) are being evaluated for the replacement of disks in the mobile computing market. Several organizations have tested various PCMCIA cards with mixed results (*PC Magazine* 1993, *Computer Reseller News* 1993). There are still some concerns over the write cycle time and endurance of FLASH memory; however, for most applications there does not seem to be a problem.

FRAM technology is lagging FLASH by several generations. Current leaders are Ramtron and Hitachi, but several large semiconductor houses are expressing more interest and application for memory chips.

It appears that the improvement in density, power consumption, endurance, and projected price, have made FLASH a formidable technology with wide applications and an installed user base. Other than FRAM, which partially build on FLASH technology, it will be difficult for other technologies to be competitive.

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2.2 Single Electron Transistors

By Professor Dan Dahlberg
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A fundamental building block for traditional memory systems is the transistor. Loosely defined, a transistor is a device with a transfer function between two terminals controlled by a third terminal. Recent experiments on extremely small semiconductor and metal particle devices have indicated three potential terminal devices with operation considerably different from conventional transistors. Recent literature (Likarev 1993, Kastner 1993, Reed 1993) refers to the devices as artificial atoms or coulomb blockade devices. The basic operation of both types of devices relies on the effect of a single electron in a particular region on the transfer function between two terminals. At the present time there has not been a proposed memory system based upon single-electron transistors; however, because of the potential for speed and density and the clear fundamental limits to traditional device operation, it was felt important to present a brief overview of single-electron devices. For possible applications information on this phenomena, see Averin and Likarev (1992).

The devices explored thus far consist of both semiconductor devices and metal devices. Their operation is explained by first considering that the energy stored in a capacitor is given by $Q^2/2C$, where Q is the charge and C is the capacitance. If C is small enough then charges as small as a single electron can have energies as large a millivolt. A device consists of two electrodes with a small metallic particle between the electrodes. The two electrodes are the drain and source, a third electrode in close proximity to the small metallic particle would be the gate. In the unbiased state, the only way charge can be transferred between the source and drain is to supply the energy necessary to charge the capacitor. In this "off" state, there would be no current flow until a voltage sufficient for this process to occur is applied. Because of the quantization of charge, this makes the lowest charging energy or voltage for current flow to be $e^2/2C$, where e is the charge on an electron. By applying a voltage between the gate and the source, V_g , one can provide a bias to charge the capacitor thus allowing for transfer of charge between the drain and source. In this "on" state, a current can flow between the drain and source at voltages less than the $e^2/2C$ potential.

For a more detailed description of the operation, one must use a model for the charging of the gate particle. In this more accurate model, the energy of the charge on the gate particle is given by $E = QV_g + (Q^2/2C)$. This parabolic energy expression is quantized in units of e , the electron charge. In this case, the parabolic energy minimum is given by $Q_0 = -CV_g$. One can imagine a V_g

which determines a Q_0 that would correspond to an integral number of electrons. One could also imagine a different V_g where the lowest energy was not an integral number of electrons and therefore the particle would not be in its lowest state but in a state with either an excess of one electron or a depletion of one electron, depending upon which charge state was the lower energy. For operation of the single-electron transistor, one selects a gate voltage, V_g , which provides two degenerate states, not the lowest energy in the parabola, for the particle. These two degenerate states, one on each side of the parabola minimum, must differ in electron number. With this bias voltage, the gate particle can freely transfer electrons between the drain and source without the need for an extra bias.

Although the devices are simple to contemplate and model at the elementary level, they are limited by the need for low temperature operation. One way to see this is to compare the thermal energy, kbT to the difference between the 0 and 1 state energies, e^2/C , where T is the temperature in Kelvin, and C is the capacitance. For stable operation, the energy difference must be several times the thermal energy. For energy differences on the order of 1 K, this corresponds to capacitances on the order of 10-15 For if one considers a parallel square plate capacitor with a separation of 1 nm, the plates would be 0.5 microns. For LN2 operation, the plates would have to be on the order of 0.05 microns or 50 nm. For stable operation, the sizes would have to be considerably smaller. For example, metal capacitors with dimensions on the on the order 50nm have stored charge for greater than 40 minutes at temperatures on the order of 0.1K (Likarev 1993). This example also points out why single electron devices constructed of metal hold more promise than semiconductor devices. For metal devices, such as small dots deposited on insulators, the parallel plate capacitor analogy is applicable. For semiconductor devices, the capacitance will be determined not only by the geometry of the opposing semiconductors, but also the stray coupling through the substrate.

On the positive side, switching times should be fast (100 psec write and 10's nsec write), have high storage densities (10¹¹ bits/cm²), and the devices robust. Also, room temperature effects have been observed using scanning tunneling microscopy (Schoenberg et al. 1992) and that some devices are predicted to be operational at room temperature (*Electronic Engineering Times* 1993, *Technology Japan* 1993). If limited to low temperature operation, some work has been done to consider superconductor aspects to the general phenomenon (Tuominen et al. 1993). A final note is that these are very much in the laboratory setting as physics devices and although transistors are not commercially available or even planned, there are transistor models (Amman et al. 1989) and transistors with voltage gain in the laboratory (Zimmerli et al. 1992). All in all, memory devices based on this phenomena are least a decade away if ever.

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3 MAGNETIC TECHNOLOGIES

3.1 Magnetic Core Memory Review

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3.1.1 Technology Overview

Magnetic Core (MC) memory is a random access, nonvolatile, radiation hard, magnetic memory technology. Binary information is stored in the magnetization states of discrete magnetic cores. Arrays and planes of arrays of magnetic cores are used to create two-dimensional and three-dimensional random access memories, respectively. Core diameters can range from 750 microns or less, corresponding to a volumetric storage density of 15 bytes/ems or greater, and practical storage capacities of 200 kbytes or more. Magnetic cores are typically made of ferrites including manganese/magnesium ferrites and lithium ferrites. Writing and readback are achieved with wires which are threaded through the magnetic cores. A common technique for writing a bit into a particular core within a two dimensional array of cores uses two sets of conductors. One set of conductors is arranged so that every core in a given row is threaded by one conductor. A second set of conductors is arranged so that every core in a given column is threaded by one conductor. Every core is threaded by one row and one column wire, and therefore has a unique row and column address position. If a current with amplitude I_w is needed to provide a local magnetic field that magnetizes a core to saturation in a particular direction, and if currents I_r and I_c are passed respectively into particular row and column lines, then if $I_r + I_c > I_w$ while $I_r < I_w$ and $I_c < I_w$, then only the bit for the core for which $I_r + I_c > I_w$ is rewritten, and the magnetization states of each of the other cores is not altered. The sense of I_r , I_c , and I_w are all the same, and the polarity is used to write binary information. In practice, I_r and I_c are approximately equal and typically equal $2I_w/3$. Write times typically range between 200 ns and 3 microseconds.

Readback occurs typically through inductive coupling and flux sensing between a drive line, a selected core, and the sense line. Architecturally, the lines used for readback can either be separable from or common to the writing lines. During readback, a given core is in a known magnetic state and a current is issued to the drive line. Cores already magnetized in the same direction as the magnetic field induced by the drive current produce a

negligible voltage in the sense line, since there is no significant irreversible change in magnetization. The albeit small noise can be attributed physically to the difference between remanent and saturated states. However, cores initially magnetized oppositely will have their magnetizations reversed. This reversal of magnetization produces a voltage signal in the sense line which differs from that induced in cores already magnetized in the direction of the field from the drive current. In this manner, binary information is recovered. It is noted that this readback method is destructive. Once the data are readback, electronic control is required to restore the data if needed.

3.1.2 Conclusion

MC memory is a mature technology, currently with niche applications. Core memories were at one time a dominant random access memory technology. Core memories were dominant when the cost per bit for cores was less than the cost of discrete semiconductors and prior to the introduction of integrated circuit memories with reduced costs per bit. MC memory technology currently exists and has been in existence for more than forty years. It is estimated that doubling storage density can be achieved at an investment of \$5 million. Issues to be addressed surround further miniaturizing discrete cores to achieve sufficient mass, volume, power consumption, and speed advantages; reducing peak current requirements; reducing line inductance to decrease cycle times; providing techniques that address nondestructive readback; obtaining good margins during half-select writing; and obtaining good read signal margins. The physical stability, handling characteristics, temperature stability, and reliability of miniaturized discrete cores needs to be addressed. Bit cost is estimated at approximately \$1 00/Megabyte.

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3.2 Thin Film Plated Wire Memory and Cross-Tie Storage Review

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3.2.1 Technology Overview

Plated Wire (PW) memory is a random access, nonvolatile, radiation hard, magnetic memory technology. Binary information is stored in the magnetization states of patterned magnetic elements. Arrays of these magnetic elements are used to create two-dimensional random access memories. In a PW memory, the magnetic elements are typically square, rectangular, or rhomboid in shape and are typically single-domain. The magnetic material is typically a plated or vacuum-deposited soft magnetic material, such as permalloy (NiFe), with a uniaxial anisotropy.

The architecture of a PW wire memory is somewhat like that of a magnetic core (MC) memory. Row-ordered and column-ordered metal lines cross each magnetic element to write to and to access each memory element, and a separate, inductively-coupled metal line is used to read data. Because of limitations in permalloy film uniformity, word addressed storage is typically used rather than coincident selection as is used typically in MC memories.

The basic principle for writing data involves the use of abrupt coherent switching in a uniaxial film. The classical switching astroid equation, which describes the energy density of a magnetic element that is governed by uniaxial anisotropy energy density and a magnetostatic energy density caused by the interaction of the magnetization with an applied field, describes the stable states and switching conditions for the magnetization. Each magnetic element has an easy axis of magnetization which is the axis along which the magnetization aligns in the absence of applied fields. The magnetization can point in either of two directions along this easy axis to provide binary data storage. Orthogonal to the easy axis is the hard axis. For stable magnetization directions which are along the easy axis, increasingly large fields applied along the hard axis cause easy axis-directed magnetizations to rotate reversibly toward the hard axis. For stable magnetization directions which are along the easy axis, fields applied parallel to the magnetization induce no change in state; while increasingly large fields applied antiparallel to the magnetization direction induce an abrupt magnetization reversal at a critical field value, as predicted by the switching astroid, which causes the magnetization to align parallel to the applied field.

Two currents are used to write data. A drive current is applied along with a digit current whose polarity defines a binary "1" or "0." The net magnetic field produced by these two currents induces the magnetization to reside on one or the other side of the hard axis. When the currents are removed, the magnetization aligns with the digit field to store a "1" or "0."

Readback is performed by applying the drive current and measuring the inductive signal pulse produced on the inductively-coupled read line. The polarity of the inductive signal indicates a "1" or a "0," since the rotation directions and hence induced flux are opposite in sign since the binary magnetization directions are oppositely directed and hence opposite in sign. If the drive current is sufficiently large, which is typically necessary to induce a large signal, destructive readback may occur. In this event, data restoration may be achieved by energizing the appropriate digit current line with the proper current polarity. This write after read may be performed within a single read cycle using electronic feedback. It is also noted that non-destructive readback maybe achieved simply by canting the drive lines with respect to the easy axis, as verified by the switching astroid.

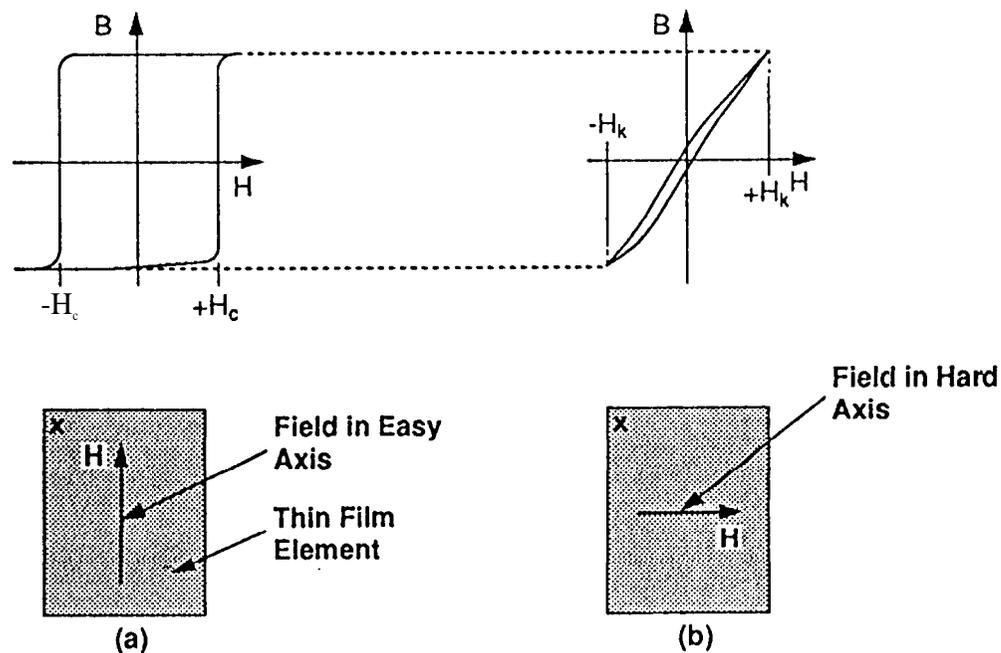


Figure 3.2.1 Thin Film Properties. BH loops: (a) BH loop in easy axis; (b) BH loop in hard axis. Source: Dakin & Cooke (1967)

In practical PW memories, the ratio of the drive current to the digit current ranges approximately from 5 to 7. Practical limitations which affect PW memories include density limits which result from signal, single-domain storage and switching characteristics, and element-to-element crosstalk

considerations. Power levels can be high because currents ranging from 0.1 to 1.5 A are typically needed to account for the magnetic characteristics and coupling **inefficiency**. Selection **circuitry** can be complex and architectural constraints are formed because of tradeoffs needed between noise margin, power, and data accessibility.

The Cross-Tie (CT) storage device is a solid-state storage device in which magnetic domain wall structure is used to store and access information. ACT storage device typically uses **permalloy** material as the storage medium. The presence or absence of magnetic cross-ties in a Neel-type magnetic domain wall is used to store binary data. The magnetization in the **permalloy** film lies in the plane of the film. A Neel wall, which can have two **chiralities** of in-plane magnetization, is the boundary between two oppositely magnetized domains. The magnetization throughout the Neel wall is in-plane, and the magnetization in the center of the Neel wall is perpendicular to the magnetizations of the two adjoining magnetic domains.

Data are stored by creating and/or annihilating magnetic cross-ties. Data are readback in magnetoresistive permalloy using a magnetoresistance bridge. Data access is achieved by propagating cross-ties along the Neel wall. While each of the necessary components have been developed and operated successfully, system implementations of the CT storage device have been limited.

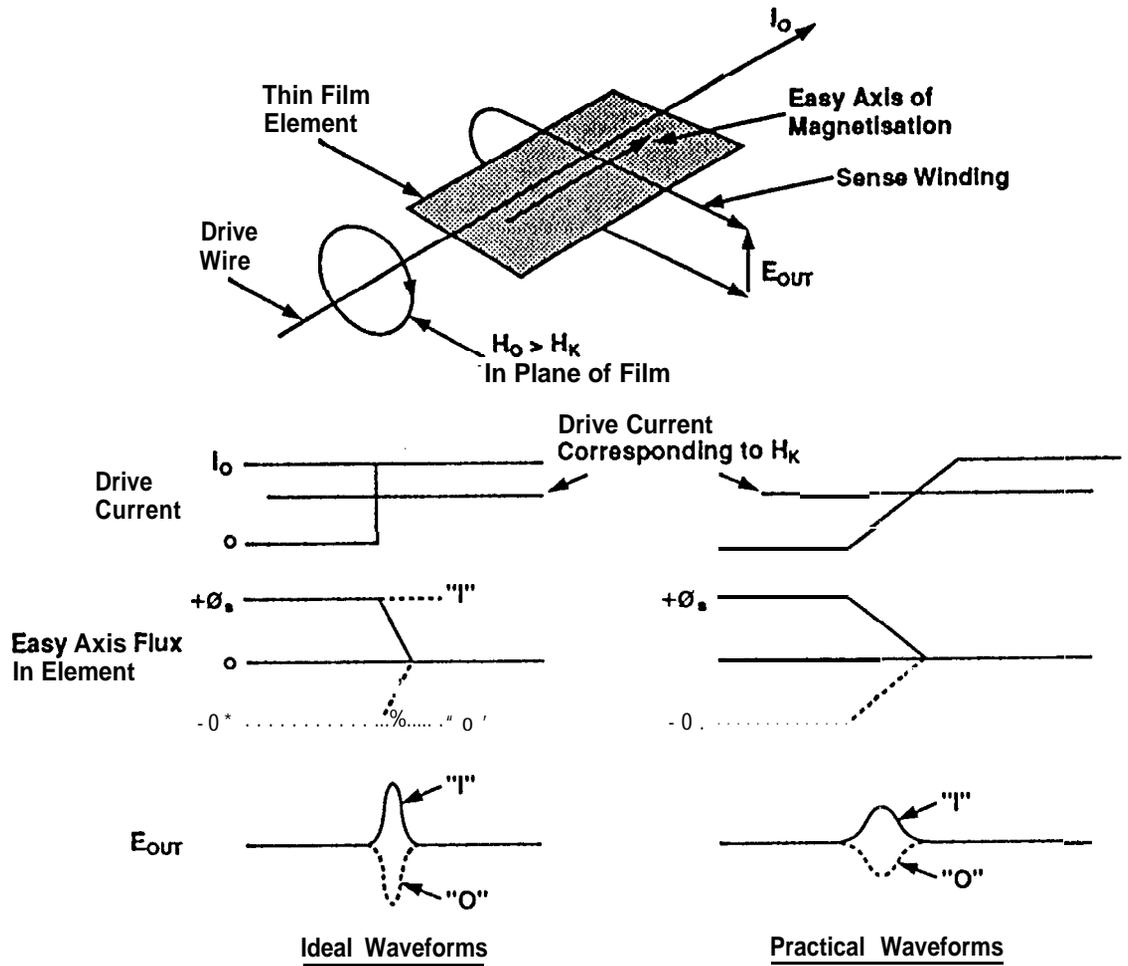


Figure 3.2.2 Sensing method for thin film elements. Source: Dakin & Cooke (1967)

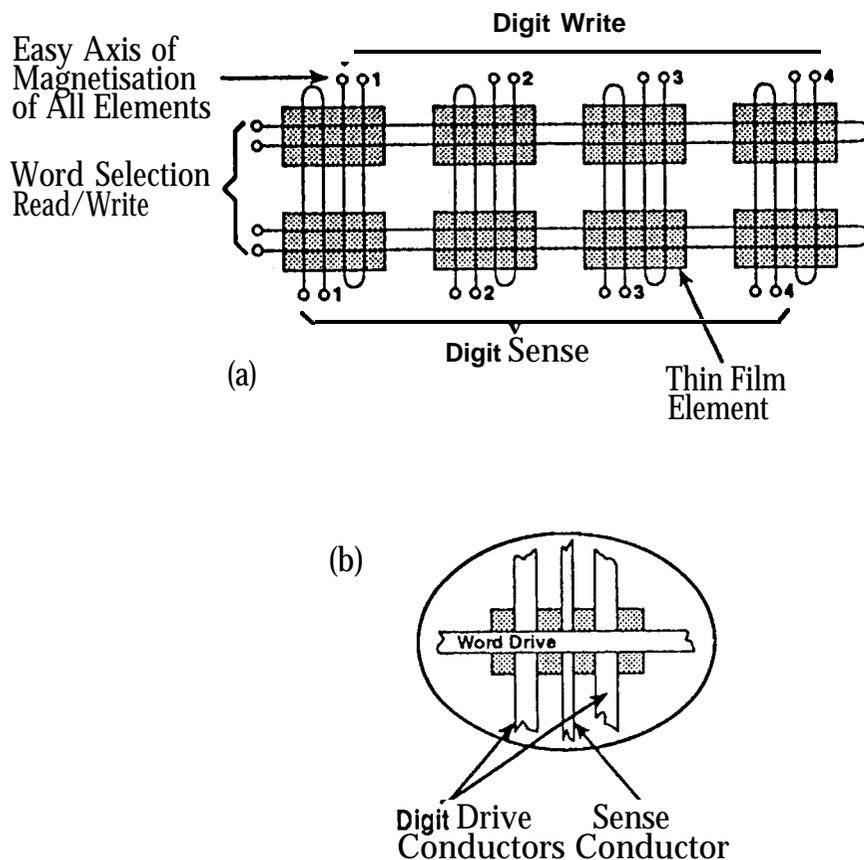


Figure 3.2.3 Two word, four bit per word thin film plane store: (a) wiring schematic arrangement; (b) practical winding detail of one element. Source: Dakin & Cooke (1967).

3.2.2 Conclusion

Plated wire memory is a mature and established technology with niche applications. As PW memory elements are reduced in size to achieve higher storage density, the switching characteristics of the domain structure in the storage material become more significant. Further integration of magnetic storage elements into active semiconducting circuitry can be performed for purposes of miniaturization, control, and signal enhancement, and cost, to lead to hybrid random access memories. PW memory technology currently exists, and has been in existence for more than forty years. It is estimated that doubling storage density can be achieved at an investment of \$5 million. Issues to be addressed surround further miniaturization to reduce mass and volume consumption; reducing current requirements to reduce power consumption; reducing line inductance to decrease write times while

increasing mutual inductance to increase read signals; providing techniques that address nondestructive readback; and obtaining good switching characteristics and margins during the writing process. Bit cost is estimated at approximately \$100/Megabyte.

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3.3 Magnetic Bubble Storage Review

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3.3.1 Technology Overview

Magnetic Bubble (MB) storage is a nonvolatile, radiation hard, solid-state magnetic storage technology. Cylindrical magnetic domains, called magnetic bubbles, are used to store and access data. MB storage chips typically use major loop/minor loop architectures to increase storage density and allow reasonable access to data. In a major loop/minor loop architecture, the major loop is physically a shift-register-like ring structure which allows data to be read from and written to the system. The minor loops are an array of shift-register-like ring structures which store data and allow data to be circulated and accessed. Transfer gates are used to move data between the major loop and the minor loops. The use of major loop/minor loop architectures in MB storage chips provides associative data storage and hence block access to data since the output data stream is composed of bits of data that are physically related when stored in the minor loops.

Magnetic bubbles are stable magnetic domains with perpendicular magnetization that range from 100 micrometers to less than 0.1 micrometers in diameter. Magnetic garnet materials are typically used because they support bubble diameters in the current range of interest which is between 0.5 micrometers and 5 micrometers. Orthoferrites can be used if larger bubble diameters are needed, while hexaferrites and amorphous rare earth transition metal films can be used if bubbles with smaller diameters are preferred. Magnetic bubbles are stabilized by a balance between a static bias field, demagnetizing fields, and domain wall energy pressure. The presence or absence of a magnetic bubble in a physical bit location represents binary information. Magnetic bubbles are typically accessed and propagated using a technique called field access which is implemented using a rotating in-plane magnetic field. Two windings, physically rotated by 90 degrees from each other, are driven sinusoidally or linearly at the same frequency or fundamental frequency but out-of-phase so that the magnetic field vector induced by the two windings rotates in-plane. A magnetic layer composed of a highly permeable, soft magnetic material such as permalloy (NiFe) is deposited and patterned on an insulator above the garnets top surface. Magnetic charges, induced by uncompensated magnetic dipoles at the patterns edges, systematically serve to repel or attract bubbles by creating magnetic field gradients. Patterns, such as T-I bars, C bars, chevrons,

asymmetric chevrons, asymmetric half-discs, and other patterns inducing **contiguous** disks, are used to control the propagation of bubbles synchronously around major loops and minor loops. Bit propagation rates typically range from 100 kHz to 1 MHz.

Bit operations other than magnetic bubble propagation are typically current driven. Magnetic bubbles are written into the major line using a bubble nucleator. In one type of bubble nucleator, a seed bubble is created and maintained. When the seed bubble is stretched, it can be split into two bubbles, in which one part is the remanent seed bubble, and the second part is a new bubble. A second type of bubble nucleator uses a hairpin-shaped conductor. When a bubble nucleating current is issued to the nucleator, a field is induced in the storage material in a direction that opposes the static bias field. This opposing field induces a reversed magnetic domain, i.e., a magnetic bubble, into the material. Erasing, or annihilating a magnetic bubble occurs through an analogous process. When a perpendicular field is applied using a hairpin conductor in the direction of the bias field, the magnetization in the bulk is reinforced so that the magnetization in a magnetic bubble is effectively reversed and hence removed.

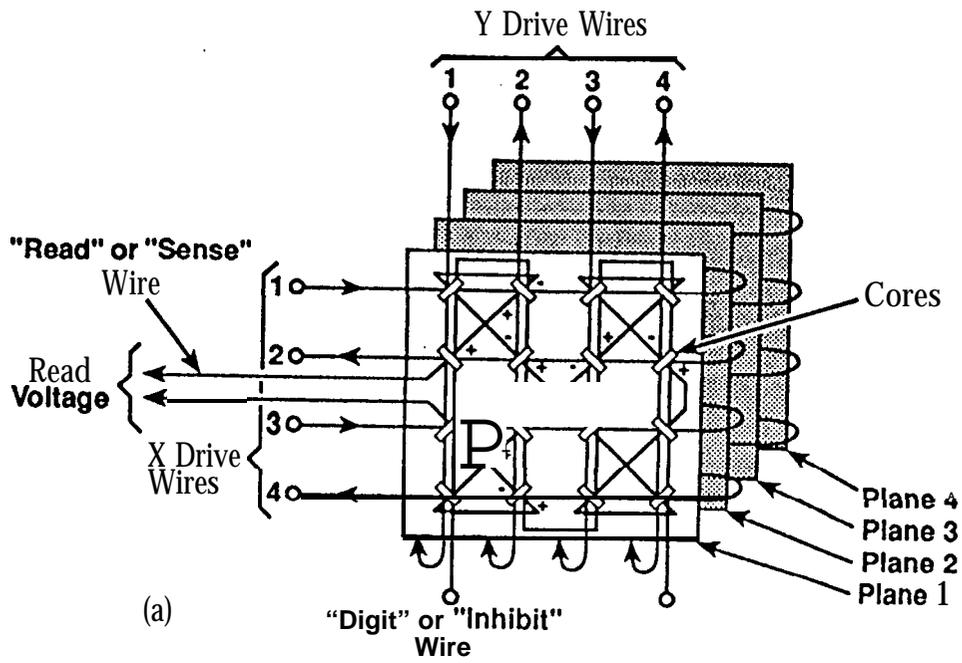
Bubbles are transferred between major loops and minor loops using transfer gates. Transfer gates can be designed to transfer bubbles between major loops and minor loops, to replicate bubbles and then transfer them, or to swap bubbles between major loops and minor loops without replication. Sequences of currents that are phased with the rotating in-plane field are used to operate the transfer gates.

Output sensing of magnetic bubble patterns into data typically occurs magnetoresistively. Permalloy is commonly used as the magnetoresistor. The fringing magnetic field from a magnetic bubble or a stretched magnetic bubble changes the resistance of the magnetoresistor. Given a reference sensing current, two voltage states are produced, depending upon whether or not a bubble is present in the magnetoresistive detector. Differential detection is typically employed since the common mode signal from the rotating in-plane field needs to be removed from the magnetoresistive signal induced by the data.

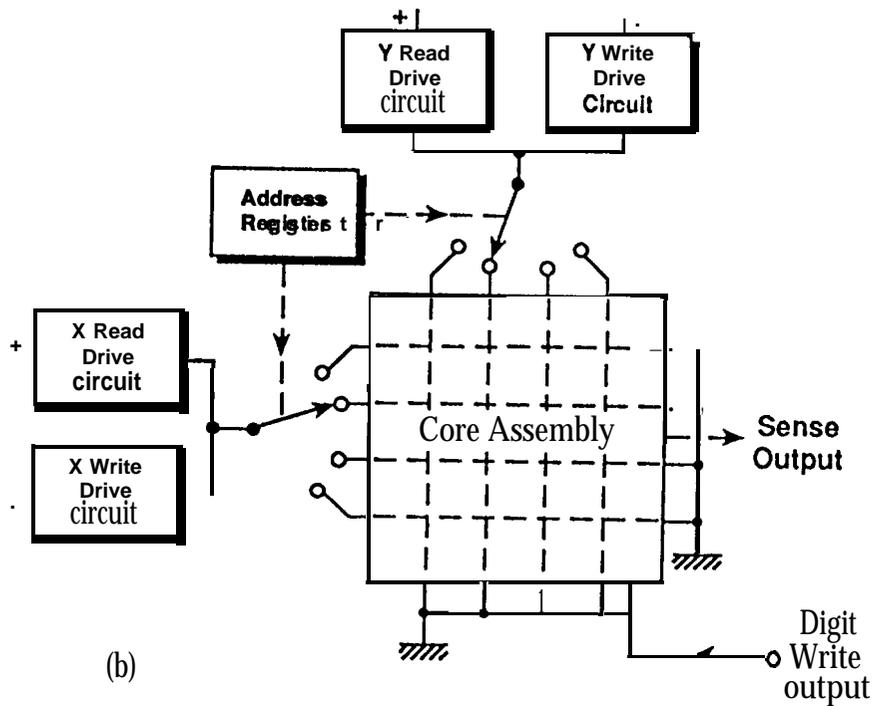
3.3.2 Conclusion

MB storage is a mature technology, with niche applications. Sagem Corporation, in Paris, France, is a leading manufacturer of MB devices. MB storage was a candidate technology with the potential to serve effectively as a data cache between memory and mechanical storage devices. However, as the cost and performance of mechanical storage devices improved, the opportunities for MB storage technology diminished significantly. Prototype

packages with 128 kbyte to 1 Mbyte capacities are available. Higher **density** devices could be developed in two to five years. Prototype packages with doubled or quadrupled densities could be made available at costs around \$5 million. Issues to be addressed in further technology development include obtaining satisfactory major loop/minor loop operating margins, and limiting power consumption from current-driven rotating field sources as data rates are increased. Cost is estimated as approximately \$50/Megabyte. Hundreds of papers have been written on the subject over the past thirty years, with reduced activity over the past ten years.



(a)



(b)

Figure 3.3.1. MIT Storage System: (a) 16 word store, 4 bits per word; (b) selection circuits arrangement. Source: Dakin & Cooke (1967).

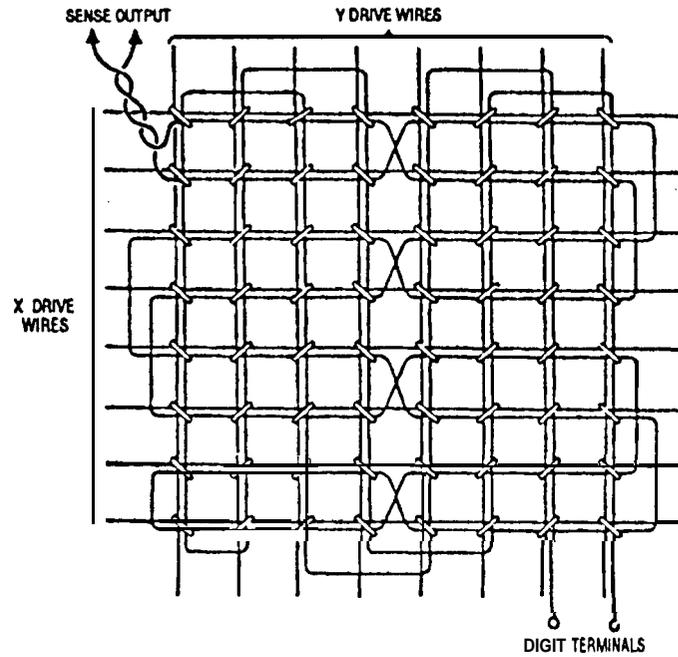


Figure 3.3.2. MIT store rectangular sense winding. Source: Dakin & Cooke (1967).

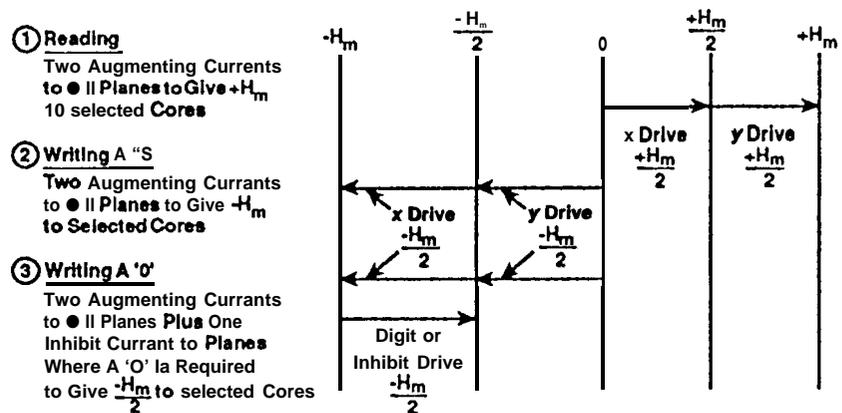


Figure 3.3.3. Reading and writing method in MIT store. Source: Dakin & Cooke (1967).

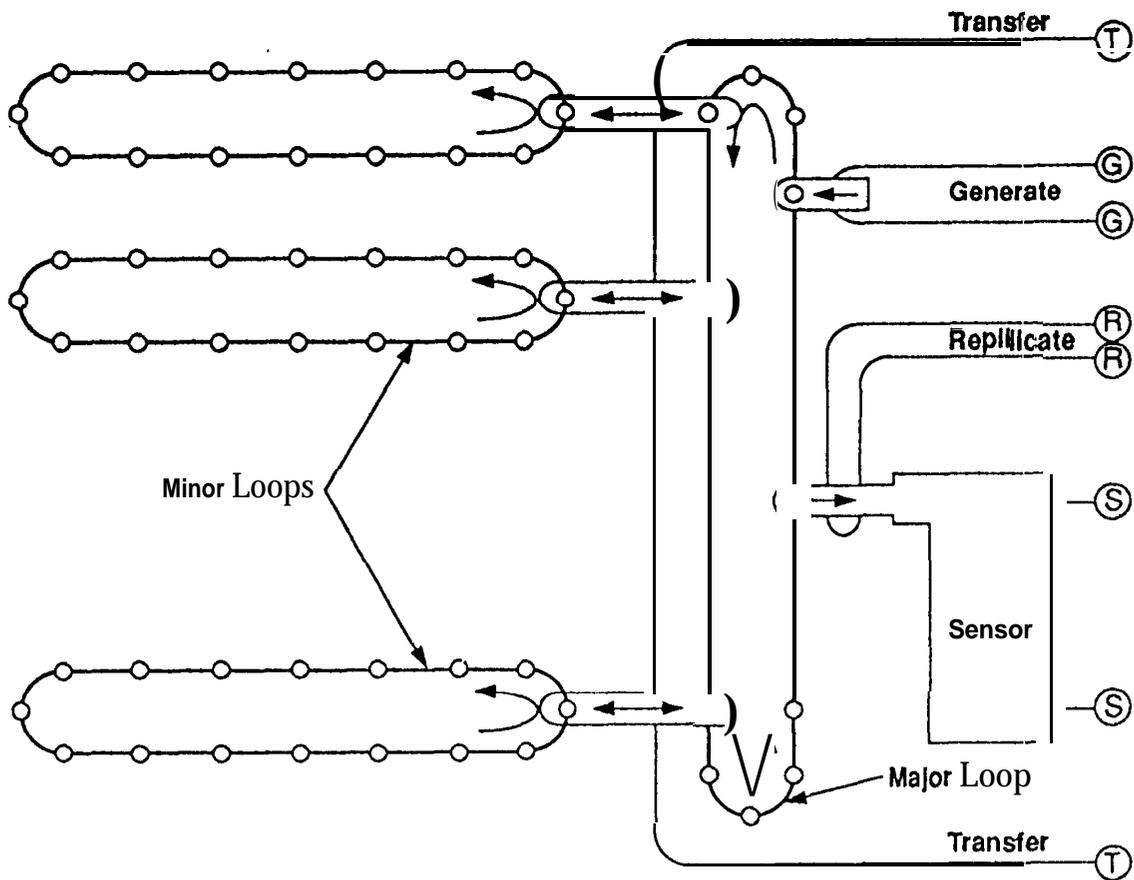


Figure 3.3.4. Source: Watson (1980).

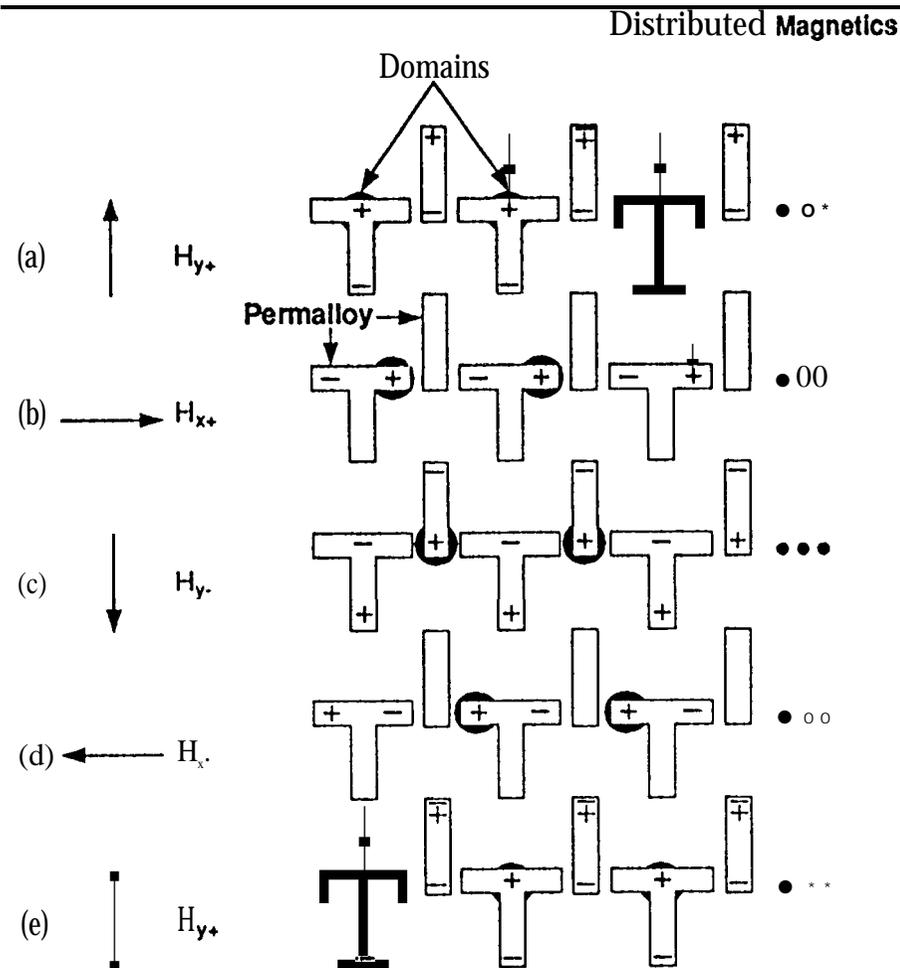


Figure 3.3.5. Propagation of bubbles with field-accessed T-bar overlay elements. The drive field rotates clockwise in the x-y plane, causing the bubble pattern to move to the right. Source: Watson (1980).

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3.4 Vertical Bloch Line (VBL) Storage Review

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3.4.1 Technology Overview

Vertical Bloch Line (VBL) storage is a nonvolatile, radiation hard, solid-state magnetic storage technology. In a VBL storage chip, data are stored and accessed using minor loops and major line architecture. VBL storage chips typically use major line/minor loop architectures to increase storage density and allow reasonable access to data. In a major line/minor loop architecture, the major line is physically a shift-register-like structure which allows data to be read from and written to the system. The minor loops are an array of shift-register-like ring structures which store data and allow data to be circulated and accessed. Write/read gates are used to move data between the major line and the minor loops. The use of major line/minor loop architectures in VBL storage chips provides associative data storage and hence block access to data since the output data stream is composed of bits of data that are physically related when stored in the minor loops.

An array of magnetic domains is used to create the minor loop storage area. Epitaxial rare-earth-doped yttrium-iron-garnet (YIG) films, grown on substrates such as $Gd_3Ga_5O_{12}$ (GGG), serve as the host material. The magnetic domains which constitute the minor loops can be formed by first saturating the minor loop area, nucleating magnetic bubbles in the presence of a perpendicular bias field and then reducing the bias field to realize an array of stripe domains. Magnetic domains can also be formed by saturating the minor loop area, creating a series of islands of reversed magnetization, and then magnetically chopping the ends of these domains to create an array of stripe domains. When the minor loops are initialized using the former technique, the stripe domains are typically stabilized magnetostatically using partially etched grooves or patterned magnetic films. When the minor loops are initialized using the latter technique, the stripe domains are typically stabilized by wrapping a magnetic domain around a completely etched groove. It is noted that the conductors which support the minor loop initialization process can also be used to erase the entire chip with a single current pulse if necessary.

Domain walls between these magnetic domains serve as the storage medium. Bits are defined by the presence or absence of micromagnetic structures in bit cells that are defined along the domain walls. These cells can be defined by

using modulations in the film's surface, patterned strips of magnetizable material, or stress-induced anisotropy variations to create a periodic sequence of magnetic potential wells which define stable positions for VBL pairs.

The presence or absence of pairs of VBLs in a storage cell is typically used to store binary data. VBLs are stable magnetic transitions in domain walls. A VBL is the separation between the two possible in-plane magnetization states, or chiralities, of a magnetic domain wall. VBL pairs consist of coupled VBLs which are held together through a balance between exchange and demagnetizing energies. VBL pairs are approximately 0.05 micrometers to 0.3 micrometers in length in current YIG materials. Areal storage density can range from 200 kbytes per square centimeter to greater than 1 Gbyte per square centimeter. Volumetric storage density can exceed 128 Gbytes (1 Tbit) per cubic centimeter. Magnetic garnet materials are transparent, birefringent, and provide Faraday rotation of transmitted polarized light. Thus, optical techniques can be used to investigate VBL chip operation. Further, VBL devices can be conceived which could support direct optical data storage and optical addressing.

Access to the data in VBL chips is performed using read and write gates and input and output major lines that use magnetic bubble technology. To prepare for the writing operation into the VBL storage area, data are loaded into the VBL chip serially to create a data block. A pattern of magnetic bubbles is created in which the absence or presence of a magnetic bubble represents binary information. A local conductor at the head of the major line is used to inject magnetic bubbles into the major line. A two-layer serpentine shaped pair of conductors is used to propagate the bubbles towards the VBL storage area. A sequence of four bipolar current pulses are used to create a series of field gradients which propagate bubbles along the major line. Propagation rates are typically between 200 kbytes/s and 2 Mbytes/s per major line, with four or more major lines per chip, depending on architectural implementation and pin count, leading to chip data rates typically between 5 and 20 Mbytes/s. The writing of data into the VBL storage area is performed in a parallel operation in one clock cycle. Each bit in the data block is written into each minor loop simultaneously in the VBL storage area.

Physically, data are written by taking advantage of the dynamic punch-through of Bloch loops in magnetic domain walls. When a magnetic domain segment, such as a stripe domain in the vicinity of the write gate, does not move, no change in wall state occurs. However, when a domain wall segment with a given in-plane magnetization chirality is driven with a magnetic field impulse, magnetization reversal is induced. This region of reversed magnetization is initiated at the surface of the material; propagates through the thickness of the film via the propagation of the resulting Bloch loop which serves as the dynamic boundary between the original and new wall segment chiralities; and reaches the other film surface, thereby allowing

the Bloch loop to punch through and form a stable pair of Bloch lines. By taking advantage of magnetostatic repulsion that occurs between a magnetic bubble and a stripe domain near its write gate, the wall segment near the write gate can either be immobilized or allowed to move, depending on whether a bubble is introduced from the major line into the write gate. In this manner, binary data can be written since VBL pair injection is controlled by the presence or absence of a magnetic bubble in a particular minor loop's write gate.

Data are manipulated around the storage area using a local pulsed magnetic field. VBL pairs are propagated gyrotropically around magnetic domain walls in a shift register format. Bits propagate around each minor loop simultaneously and synchronously. The readback of data occurs in a parallel operation that reads a block of data into the major line from the minor loop in a single clock cycle. The data block appears as a sequence of magnetic bubbles in which the presence or absence of a magnetic bubble in the major line constitutes the data. During a read cycle, data which are positioned at the ends of each minor loop are read in parallel and nondestructively by taking advantage of the difference in exchange energy in domain walls whether there either is or is not a VBL between the two domain wall segments. If a VBL pair is not present, the chiralities of the domain wall on opposite sides of a minor loop stripe are opposite, so that as the domain walls are brought together through the chopping process, it is difficult for the domain to be chopped. If a VBL pair is present, the VBL pair is first split, either dynamically or through the application of an in-plane field which is oriented parallel to the chirality of the domain wall that is between the two VBLs in the VBL pair. In this event, the chiralities of the domain wall on opposite sides of a minor loop stripe are now parallel, so that as the domain walls are brought together through the chopping process, it is easy for the domain to be chopped. Hence, the difference between the minimum currents needed to chop domains in these two cases forms the basis for nondestructive readback of binary data. It is noted that destructive readback, as well as data clearing, can be performed by bringing a stripe domain into a read gate and simply chopping both domains. The produced magnetic bubble will have either zero or one VBL pair. This difference can be used to identify the bubble's state, for example by noting the deflection angle of the bubble in a gradient field.

After a read operation, once the data are loaded into the major line, the data are transferred to and serially detected by a magnetoresistive sensor. This sensor provides a signal, typically on the order of 100 mV, which can be amplified and converted into a digital signal. Read rates are typically 200 kbytes/s to 2 Mbytes/s per major line. Each VBL chip is expected to support several major lines, in which the number of implemented major lines will depend upon application requirements.

3.4.2 VBL Technology Issues

While VBL technology is based on magnetic bubble technology, several **technological** differences lead to VBL architectural and performance improvements in terms of storage density, data rate, access rate, and power consumption. First, the use of VBLs along a domain wall in place of bubbles for storing data in the minor loops significantly increases areal and volumetric storage density. Second, the use of a current-access major line in place of a rotating in-plane field increases VBL chip data rate while also reducing power consumption. Third, the use of pulsed gyromagnetic bit propagation for shifting high-mobility VBLs around the minor loops in place of rotating in-plane field propagation of magnetic bubbles decreases data access times while also reducing power consumption.

Research and development into VBL technology and VBL storage chips has been conducted in the United States, Japan, and France. Positive prototype chip results in laboratory demonstrations have been obtained by corporations including Hitachi, NEC, Sony, and Sagem for chips ranging in density from 1 to 32 Mbytes/cm². Several technological approaches have been evaluated including a variety of techniques for stabilizing minor loops, defining bit positions along domain walls, and writing and reading bits into the storage area.

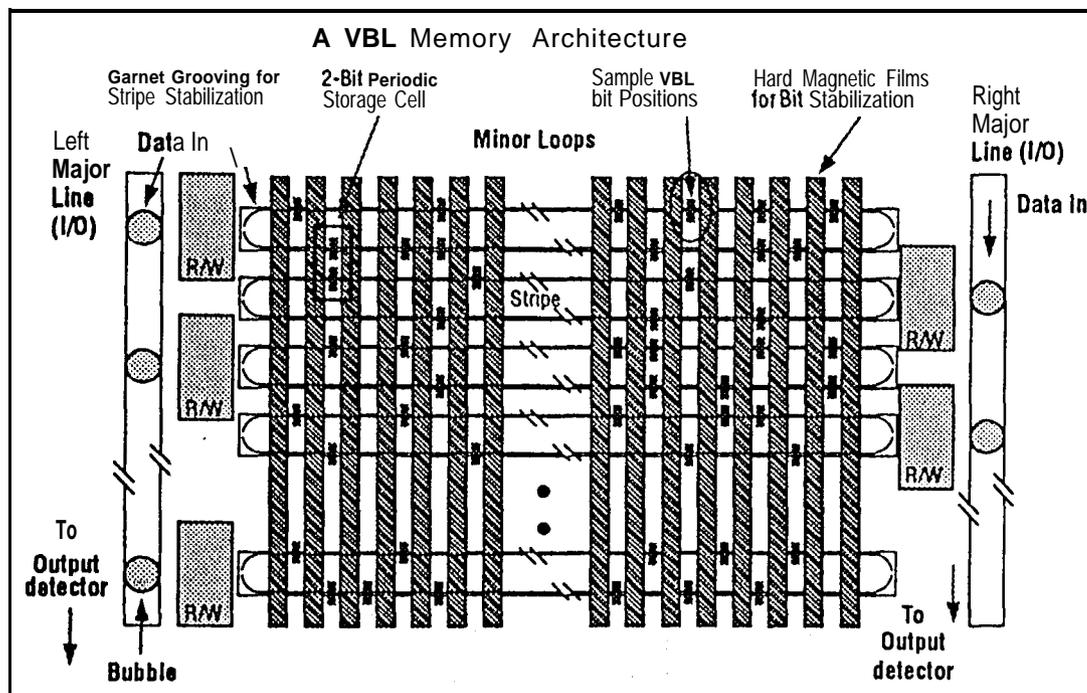


Figure 3.4.1 A schematic areal layout of a VBL chip.

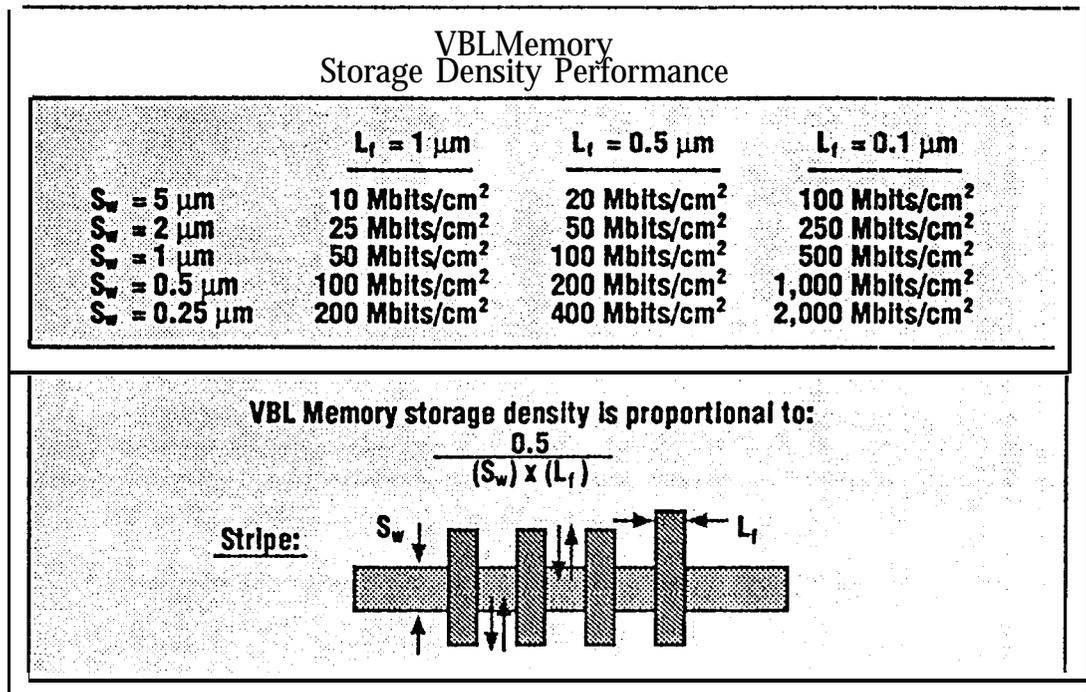


Figure 3.4.2 VBL technology storage density calculations.

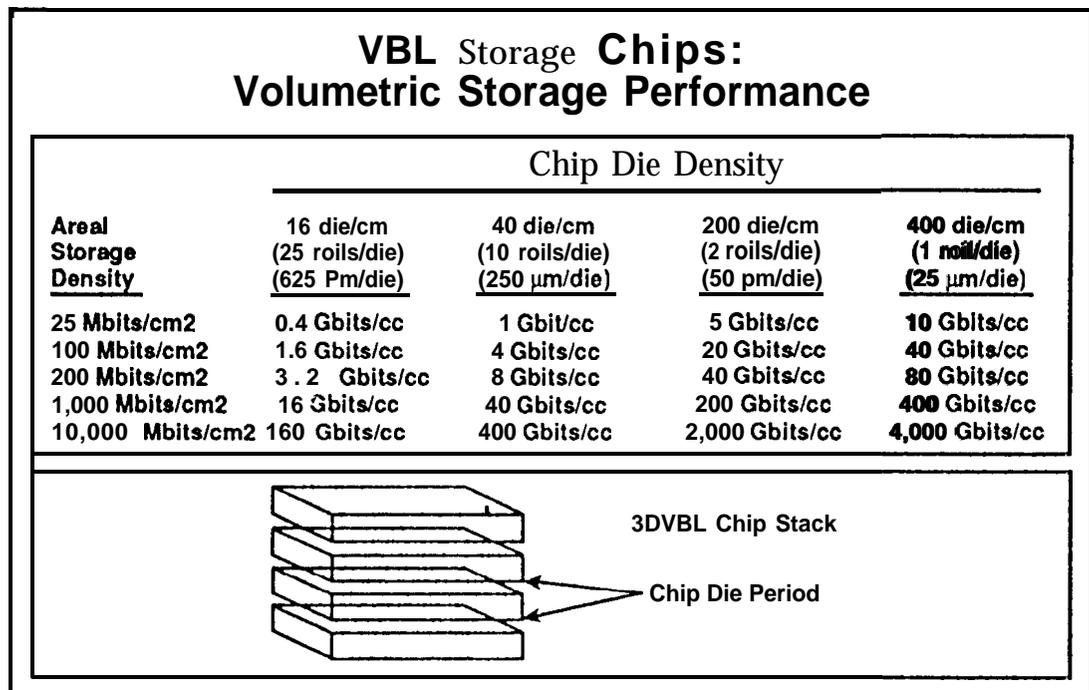


Figure 3.4.3 VBL volumetric storage performance.

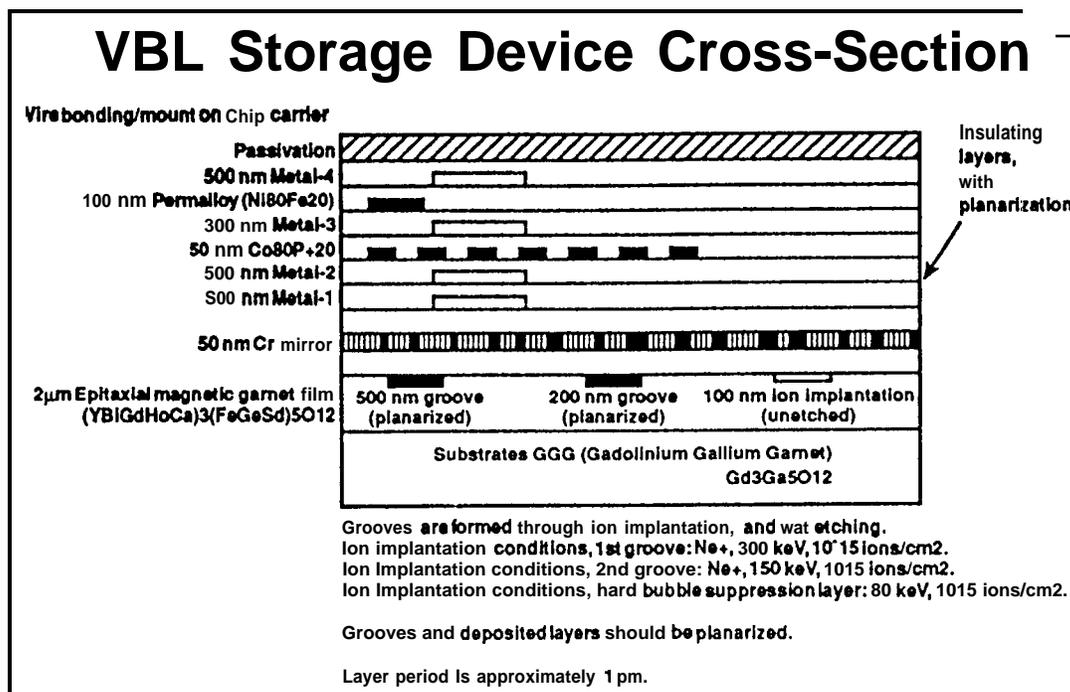


Figure 3.4.4. VBL device cross section.

3.4.3 Conclusion

VBL storage technology potentially offers very desirable solid-state data storage attributes within a single technology. VBL technology attributes, which include nonvolatility, high density, erasability, and cost-effectiveness, simply are not available in existing or alternative technologies. VBL technology is characterized as a new technology that is under research and development. VBL chips are based on materials which are magnetoelectronic and magneto-optic; indicating that VBL chips could support electronic as well as optical storage applications. It is conceivable for prototype VBL chips to be available at chip capacities between 2 Mbytes and 32 Mbytes in three to five years. This realization could be achieved at relatively modest investment costs when compared to the investment costs which have been made or which would need to be made to realize alternative technologies. Because of its architecture, VBL technology also potentially offers rapid evolutionary growth towards higher storage capacity solid-state storage chips. It is conceivable that prototype VBL chips can be available at densities between 2 Mbytes and 32 Mbytes for investment costs between \$3-10 million. Issues to be addressed include integrating all data storage device functions at high

density in a single chip, and demonstrating good margins, error-rate performance, manufacturability, reliability, and temperature-range operability. Raw cost is estimated around \$15/chip, or approximately \$0.5/Megabyte or less in high volume production.

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3.5 Magnetoresistive Random Access Memory

By Professor Dan Dahlberg
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Magnetoresistive (MR) memory devices rely on the anisotropic magnetoresistance (AMR) of ferromagnetic materials. Simply put, the resistance of a ferromagnet is a function of the angle the current makes with the magnetization. This phenomena is due to an asymmetry in the electron scattering cross section of ferromagnet materials and is not due to the modification of electron orbits by the presence of a magnetic field. For this later reason, it is not necessarily a fact that large AMR materials must also have large magnetizations. For example, the technological material of choice for AMR devices is a NiFeCo alloy, a relatively low moment ferromagnet. This alloy has a resistive difference on the order of 4% for the magnetization parallel (high resistance) and perpendicular (low resistance) to the current. This material has a magnetic moment considerably less than iron which has an AMR of only 0.4%. A number of advanced technological products utilizing the AMR are available. This includes read heads for magnetic data storage and a wide range of sensors.

MRAM devices have been developed by Honeywell Inc. and Nonvolatile Electronics, Inc., a spin off company (Daughton 1992). The following figure illustrates the geometry of the MRAM. The memory elements consist of two permalloy films (the NiFeCo alloy discussed earlier) separated by a high resistance interlayer. The energetic of the magnetization in the films (due to the crystalline anisotropy energy) is such that the magnetizations lie perpendicular to the length of the films. The purpose of the interlayer is to isolate the two films, break any exchange coupling, and allow the magnetizations to interact only magnetostatically. This magnetostatic coupling makes the 10 vest magnetic energy states to occur when the magnetizations in the wo films are

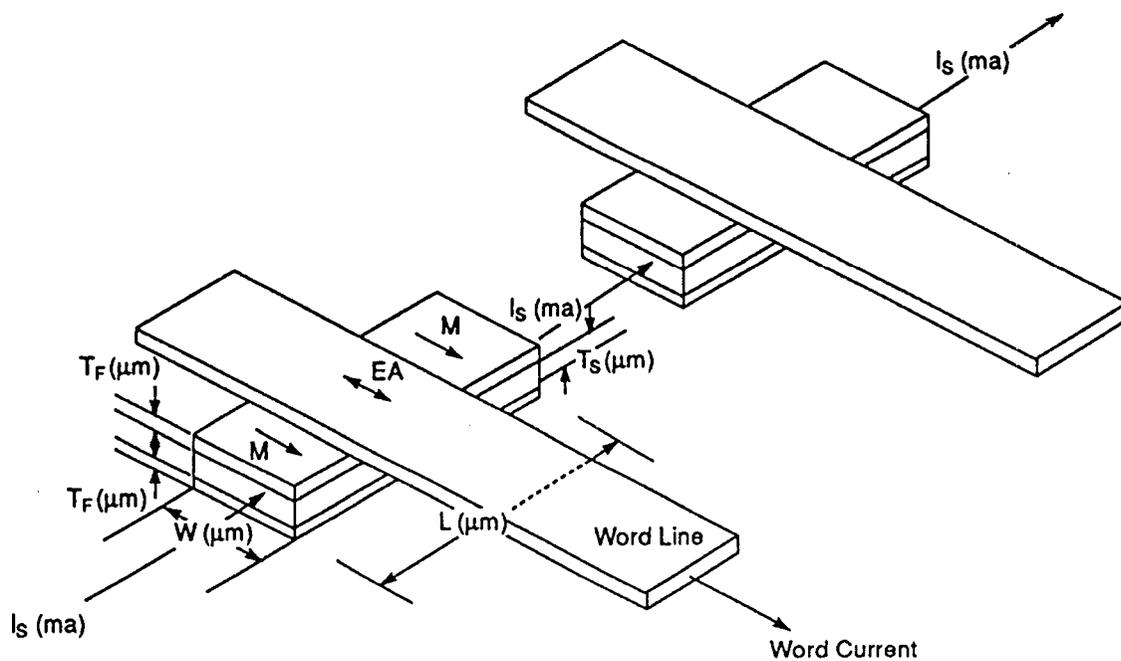


Figure 3.5.1. MRAM memory cell. Source: Daughton (1992).

antiparallel to each other. A “one” could correspond to the top magnetization going to the left as shown (the underlying film magnetization would go to the right) and a “zero” with the top magnetization going opposite to that shown, to the right (the underlying film would go the left for this state). The state of the cell can be altered by applying a current to the sense lines just described in combination with a word current in the word line. Neither the sense current by itself nor the word current by itself can switch the magnetization.

Reading can be accomplished by applying a sense current and word current below the switching threshold. If the sense current creates a magnetic field opposing the stored memory state, the magnetization will rotate to a large angle. If the current creates a magnetic field in the same direction as the stored state, then the angle of rotation is smaller. The difference in the angle of rotation between a stored “one” and “zero” gives different resistances (and thus voltages), and this difference is sensed.

At the present, limited production of 16K x 1 devices has been achieved. In general, access times can be on the order of 200 nsec with write times just a few nsec. A definite advantage of MRAM is the robustness of the devices. Devices cycled over 10¹⁵ cycles shown no signs of deterioration or wear out. Also, as with other magnetic memory devices, the MRAM devices offer excellent radiation hardness. The cost of the devices is also potentially low. The potential limitations of MRAM devices is the tradeoff between speed and density. Although the recently discovered giant magnetoresistance (GMR)

phenomena may provide a natural path for product development with both high speed and high density,

As mentioned, the limitation of MRAM devices arises from the tradeoff between speed and density (Ranmuth et al. 1992). As expected, the intrinsic speed of current devices is determined by the magnitude of the AMR of the ferromagnetic materials used. For the highest density, on the order of 4×10^8 bits/cm² with 0.2 micron feature size, the speed would be on the order of 2 microseconds (Pohm et al. 1989a, 1989b). For this density and a speed of 20 nsec, the magnetoresistance of the material would have to be increased from 2% to 20% (theoretically the sense time improves with the square of the improvement of magnetoresistance). Given the current understanding of the AMR phenomena and materials, this is unlikely to occur. There is an alternative, discovered by a French research group just a few years ago; the giant magnetoresistance (GMR) phenomena (Babich et al. 1988). Although a physics understanding of GMR is lacking, materials have been developed which provides magnetoresistance changes greater than 60% at room temperature. Clearly with the development of devices based upon the GMR phenomena, much faster devices and higher density devices can be considered. With the exception of the GMR discovery, all of the above mentioned work is US based. There is some literature which does indicate development of MR memories in the former Soviet Union (Vas'kovskii et al. 1993),

In addition to the MRAM, both older (Baugh et al. 1982, Lo et al. 1982) and newer (Lebedev et al. 1991) MR devices have been proposed included domain wall RAM devices. The magnetic phenomena for one type of memory is the ordinary Hall effect (OHE), a magnetotransport phenomena which occurs in both magnetic and nonmagnetic materials. In these memory elements, known as MHRAM for magnetic Hall random access memory, a permanent magnetic is used to induce an OHE voltage in a semiconductor element (Wu et al. 1989). This type of memory is also nonvolatile as the state of the device depends upon the magnetization direction of the ferromagnetic element. The state change occurs by flipping the magnetization of the ferromagnetic element. At the present time, these devices have read and write times on the order of 100 nsec, are nonvolatile, exhibit unlimited endurance, and are radiation hard. The difficulties, if any, are not well documented. It is clear that although the devices were first described in 1989, there are no researchers in this area other than the original developers. This may be because of the complexity of the devices, in particular, the materials used. In a recent NASA Tech Briefs (NASA 1993), some of the complexities were described in a discussion of the growth of a GaAs/InGaAs buffer and then InAs on Si to enhance the Hall signal.

In addition to the above, there are other potentially useful devices based upon magnetic phenomena other than AMR and GMR, A very recent creation

whose potential is undetermined is the recently created magnetic transistor (Johnson 1993). All three devices, the MRAM using GMR materials, the MHRAM memory cell, and the magnetic transistor provide the potential for nonvolatile memory with fast access times, radiation hardness, low cost, high density, and excellent endurance. Although at the present time the devices are serviceable, the ultimate times and densities of both the MRAM/GMR devices and the magnetic transistors require a higher degree of physics understanding of the underlying phenomena and development of the materials science of thin multilayer magnetic films.

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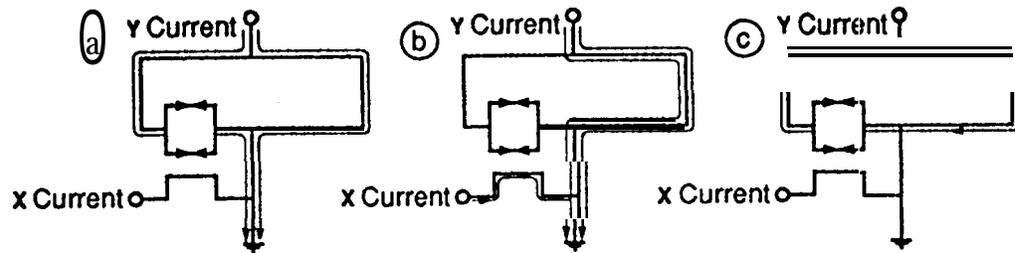
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3.6 Superconducting Josephson Junction Memory

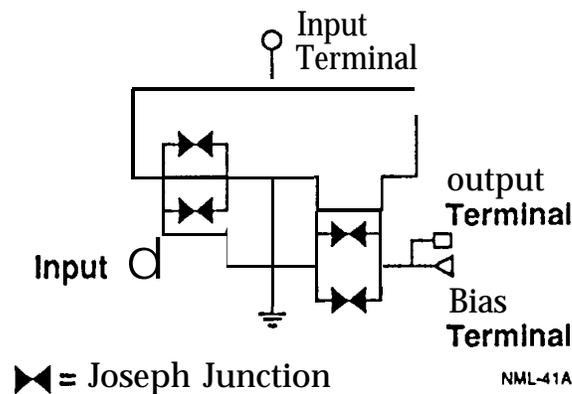
By Professor Dan Dahlberg
University of Minnesota

There has long been a recognized potential for superconducting elements for logic families and memory storage devices. In particular the high speed, zero resistance or low dissipation, and nonvolatility have been considered as very attractive features for memory systems. In the 70's and 80's, IBM pursued a development program for computers based on the superconducting Josephson effect for high speed computing and memory (Matisoo 1980). A similar, but smaller program was pursued by Sperry Univac Corporation. Probably for a variety of reasons neither company developed a superconducting computer and both abandoned their projects. In 1991, a Japanese venture funded by the Ministry of International Trade and Industry, also ended its efforts. Since that time, a few companies, mostly offshore, have continued in their efforts to develop superconducting computers. These projects have focused on the Josephson junction as the fundamental building block for the superconducting computer.

The Josephson junction consists of an oxide or very poor conductor separating two superconductors. The quantum mechanical nature of electrons and the superconducting state provide a coupling between the two superconductors which is not allowed classically. This coupling allows a weak zero resistance current to flow between the two superconductors. The other necessary ingredient for use of Josephson junctions as memory elements is the quantization of magnetic flux. Simply put, the maximum zero voltage current which can be carried by a superconducting wire and/or Josephson current is a function of the magnetic field enclosed by the current. This current field relationship is nonmonotonic and for a superconducting loop with a small inductance is given by the cosine of the flux contained in the loop. For one memory element, two Josephson junctions are used in a superconducting loop in a configuration commonly known as a SQUID (Superconducting QUantum Interference Device). The operation of superconducting memory is given by the following excerpts from *Physics Today* :



Operation of a memory cell consisting of a superconducting loop with an inserted SQUID. If flux is trapped in the loop it is interpreted as "1." and the absence of the trapped flux is a "0." Consider the writing of a 1 in a cell initially in the 0 state. The writing sequence begins with the application of a Y current as shown in part a. This current naturally divides itself between the two sides of the superconducting loop according to their relative inductances. The current in the SQUID in the left-hand branch of the main loop is arranged to be less than the SQUID critical current. Next an X current is applied. It is inductively coupled to the SQUID and reduces the SQUID's critical current below the level of the applied Y current. This causes the SQUID to switch temporarily to the voltage state, which diverts its current to the other side of the loop, as in b. if the X and Y currents are now turned off, a persistent current is established in the loop as shown in c. resulting in a 1 state. Reading of the 0 or 1 states is done with a nearby second SQUID on the right-hand side of the memory cell, which simply detects whether or not there is flux in the loop.



Memory compatible with high speed logic utilizes the quantized flux state of a superconductor. Two flux quanta are inserted for a 1 and no quanta for a 0. In present design work a one-bit memory cell is expected to have a current transfer time of about 35 ps (time to go from a to b in the above diagram), when fabricated with 2.5 micron minimum line widths. Overall memory access time for reading one bit is no more than about 500 ps on a 4K-bit chip having a 6 mW of dissipation per chip.

Figure 3.6.1. Superconducting memory operation. Source: McDonald (1981)

Switching speeds for single Josephson junctions have been recorded as fast as 1 ps. Because of the extreme sensitivity to magnetic fields, care must be taken in the layout of memory chips. This is the dominant consideration as power

dissipation is very low and self heating is not problematic. In part, this magnetic field sensitivity limits device integration. Another limitation to integration is that flux quantization imposes an inherent size limitation. A nondestructive read only memory of 16k has been proposed on a 1.5 in x 1.5 in substrate. Although not as dense as the MRAM described in the last section or silicon memory, it is comparable to gallium arsenide memory and, of course, is very fast. In this quest, there have been reports of superconducting memory chip devices with speeds on the order of 600 psec (4 kbit RAM) (Tahara et al. 1991, Ishida et al. 1991), 475 psec (16 kbit RAM with 392 micron sq area) (Kurosawa et al. 1993)], and proposed devices with times of 200 psec (4 kbit) (Chen et al. 1993). Single-Flux-Quantum (SFQ) (Fulton et al. 1973, Loe et al, 1988) and the related Rapid Single-Flux-Quantum (RSFQ) devices (Likharev et al. 1985, 1991; Mukhanov 1987) have exhibited considerably faster clocks speeds, faster than 100 GHz (10 psec). The RSFQ work, a SUNY Stony Brook- Hypres collaboration, shows that operation at 100 GHz with a power consumption of microwatts/gate is feasible. A second consortium, IBM, AT&T, Linclon Labs, and SUNY Stony Brook, are attempting to make smaller and therefore faster RSFQ devices (Taubes 1993).

Limitations of Josephson technology are the need for operation below room temperature, the lack of a suitable three terminal superconducting device for impedance matching, and the high demand made on materials processing. In the later case, the wave function of the superconducting electrons coupling across the two superconductors decays exponentially with the thickness of the oxide. This means a very small variation in the thickness across the junctions can result in a very large variation in the current carrying capacity of the device. The original IBM process which used Pb created more difficulties in this area than the later use of Nb Josephson junctions (Hasuo 1992). [There have also been efforts at using NbN for devices (Aoyagi 1992).] Attempts made at making useful three terminal devices include T* transistors using injection of normal electrons or quasiparticles to effectively create an artificial temperature, the quisitor, similar if not identical to the T* device, hybrid superconductor/semiconductor memories, vortex flux transistors, and the proximity effect FET. Of these, work on the hybrid super/semiconductor devices (Ghoshal et al. 1993), proximity effect FETs and the vortex flux transistors (Martens et al. 1993a, 1993b) continues to proceed. A recent news release (Comline News Service 1993) also purports a hybrid optical-Josephson junction device with speeds of 10 Gbps.

A question not addressed until now is: Does the discovery of high temperature superconductivity remove any of the technological impediments of superconducting computers? This question focuses on the lack of development of superconducting computers after roughly 30 years of research and development. Another way to state the question is: Does the discovery of superconductors with critical transition temperatures above 100

K compared to the 10 K critical temperature of the previously used superconducting computer elements help? Certainly the relaxation of the refrigeration requirements clearly aides the development of this technology. The temperature requirements are still well below room temperature but they do allow operation with liquid nitrogen refrigeration (77 K) instead of the previous liquid helium requirement (4 K). However the new materials have not proven themselves to be readily amenable to memory technology. For example, only one hysteretic junction has been reported to date.

The use of high temperature superconductors in memory technology is adversely affected by the coherence length of the newly discovered superconductors. This is because the memory element relies on the Josephson junction which requires a very thin nonsuperconductor between two good superconductors. In short coherence length superconductors reliable tunneling characteristics has always presented a challenge. The coherence length is the distance over which the superconductivity can disappear. In traditional superconductors this length is on the order of 10 nm whereas in the high temperature superconductors this length is closer to 0.1 nm. Thus any surface damage or destruction of superconductivity due to the interface is much more effective in destroying the superconductivity in the high temperature superconductors that in the longer coherence length devices. This short coherence length also negatively affects the potential uses of high temperature superconductors in proximity effect FETs for the same reason. On the positive side, Conductus Inc. is currently manufacturing SQUIDS based on the new materials but not memory elements at the present time, Fujitsu claims to have developed a high T_c superconductor transistor (*Electronic Times* 1993), there have been high T_c materials based vortex flow transistors (Satchell et al. 1992), TRW developed high T_c logic gates (*New Technology Week* 1992), both experiments (Xi 1992) and modeling studies (Masakuni 1992) of high T_c FETs. Both the materials science for reliable manufacture of complex structures and the physics of the high temperature conductors are necessary to aid the development of this technology.

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4 OPTICAL TECHNOLOGIES

4.1 Holographic Storage Review

By Dr. Robert Lorentz
3M/NML

4.1.1 Introduction

The primary area of exploration into non-moving optical data storage during this period has been the recently developing technique of holographic data storage. Although known in the literature for a number of years, this method of storage maybe finally approaching viability. Advances in a number of technologies, such as the materials science of photorefractive crystals and the control of light with spatial light modulators, have been required to enable this possibility. There are still a number of issues which must be resolved for this to be a practical system of data storage, but the promises of high capacity and very high data transfer rates warrant this further work.

4.1.2 Operation

The most advanced holographic storage system appears to be that of the Tamarack company, a spin-off from MCC in Austin, Texas. Therefore, their system will be described and taken as the model for the evaluation of this technology.

A beam from a laser (typically a doubled YAG laser operating at 532 nm) passes through a "stack deflection system". Although not discussed much in the Tamarack literature, this is presumably the way different parts of the crystals are accessed. The beam is then split into two. The reference beam portion passes through a "page deflection system" before impinging on the crystal recording media. The main beam is expanded and then is sent to a spatial light modulator, which constructs the "page" of data to be stored as a hologram. A lens then applies a Fourier transform to the data and the beam is directed to a small spot on the recording media. The interaction of this beam with the reference beam produces the hologram.

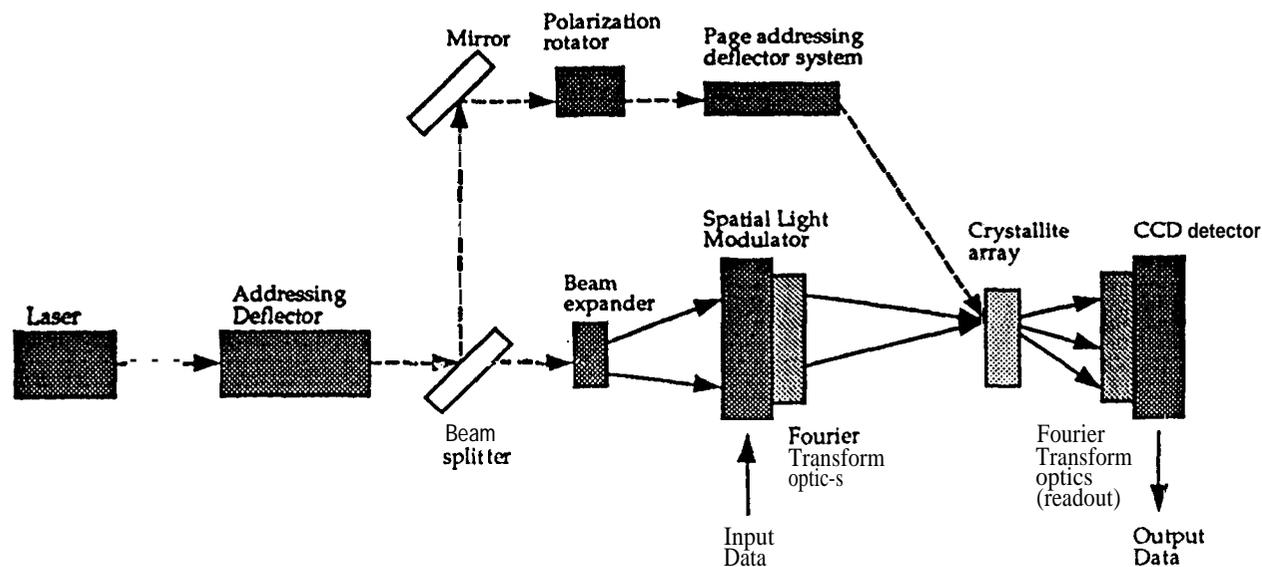


Figure 4.1.1 Holographic Storage Technology

Different holograms can be stored in the same physical space via either of two methods. The original angular multiplexing method used by Tamarack consisted of changing the angle of intersection of the reference beam with that of the object beam. Sufficiently different angles allow the Fourier Transform of the data to be stored in the same physical location. An improvement in the number and quality of the stored images ("pages") can be obtained by moving to a phase multiplexing, scheme. In this technique, the reference beam phase is shifted in a complex algorithm, with the result that more pages can be effectively stored in the same stack (of pages). One report from Tamarack indicates that the number of stored pages can go from 19 to 40 with this method. This method has the added benefit of shrinking the optical path and possibly reducing the number of optical components needed.

To store the page, one of two types of media are used. Photopolymer materials can be used as a write-once media. This is expected to be used in first generation products. To be used as an erasable /rewritable system, a photorefractive crystal, is used. Typically, this material is strontium barium niobate (SBN for short). A fiber form of the SBN media is currently being investigated. The fibers are arranged in a matrix, with each fiber separated from the others to reduce cross-talk. Each fiber can be separately written and addressed, and is responsible for storing a stack of pages. The object and reference beams must converge on the individual fibers, so they must be "addressed" by the optical system by moving the beams.

Once written, the page is not stable upon additional pages being written to the same stack, or upon readout. There is a limit to the number of times a given page can be read before the S/N drops too low. In addition, when

pages are written to the same stack, the available S/N of a previous page decreases. To avoid this problem, the pages are "fixed" by the application of a high voltage. During the writing process, a field of 6000 Volts/cm is applied. The amount of time the voltage is applied is not stated. Due to the isolated nature of the fiber crystals, an individual unit can be fixed separately.

To read the stored pages, only the reference beam is needed. In the preferred technique, the phase of the reference beam is selected for the desired page. Alternatively, the angle of the reference beam can be adjusted if the other method is used. Another lens is used to reconstruct the image since it was stored as a Fourier Transform of the data, and this image is projected on a CCD detector array for readout. Since the readout process is eventually destructive, another "fixing" voltage must be used. A field of about 1000 Volts/cm is applied and the polarization of the reference beam is shifted by 90°. This appears to produce an essentially stable readout.

4.1.3 Findings and Analysis - Holographic Storage

Advantages of the Technology/Product Development

- Tamarack is receiving about \$10.3 million from the NIST/ATP program. This is less than half the total funding for the project. The project includes technology development on the SBN crystals (Stanford and Deltronic Crystal Industries) and write-once photopolymers (DuPont), small laser source development (AMOCO Laser Company), and display and detector technologies (Displaytech, Inc. and Hughes).
- The storage of the Fourier Transform of the data should make the process more robust.
- This system has the potential for an extremely high data transfer rate, which may be of use in a number of applications (supercomputers, image storage and manipulation, etc.)
- This system has the potential to store large amounts of data, especially if multiple tiles are used.
- Claims have been made that this product will be useful to PC's, however, the performance of the system appears to be way in excess of what current PC's need.
- Use of SBN fibers may simplify the media fabrication process. In addition, the fibers of SBN are well isolated, reducing crosstalk relative to a monolithic SBN crystal. The fibers can be fixed on a fiber-by-fiber basis.

- The fact that pages can be written and retrieved as one unit may be advantageous for video and image processing applications.
- The system can be configured to meet a wide variety of applications. Three configurations discussed by Tamarack are for general, high capacity, and high bandwidth applications. Listed below are representative parameters of such systems. Note that within each class, a wide variety of parameters are possible.

	Capacity (Gbytes)	Transfer rate (Mbytes/s)	Read cycle (ms)
General use	0.7-2.3	80-327	0.1
High capacity	350	11	3.1
High bandwidth	2.3	327	0.1

Limitations of the Technology

- The first prototype (expected Q1 '94) of the "Holostore" product from Tamarack will not be rewritable; rather, it will use photopolymer media. Thus, it will be a WORM system. It will hold 50 "tiles" in a jukebox compatible cartridge. A "tile" is a component of the medium, and consists of an array of the photosensitive material, each element of which can store a "stack" of pages. This configuration of the device will require movement of the tiles from the cartridge to the optical area for I/O, and therefore is not a non-moving system. The storage capacity of a non-moving system may therefore be limited to some fraction of that of the larger, moving, system.
- The holographs must be fixed during writing and during reading by the application of a high field (6000 and 1000 Volts/cm, respectively). This requires additional electronics in the system. How fast the fields can be applied, and if this is a limitation to the data transfer rates, size, cost, etc. in any way is not yet determined by this review.
- A low-cost fabrication process for the SBN crystals is needed.
- There is some practical size limit to the media. Beyond some point, the optics and beam deflection system get expensive and complex. This limits the storage capacity of one tile. To use multiple tiles would require some mechanical system to move tiles into the beams.

- The 1/0 rate maybe limited by the spatial light modulator frame rate.

Unresolved Issues

- The suitability of this recording method for archival purposes is not yet known (to this researcher).
- **Bellcore** is pursuing multiple lasers on a chip. To date, they have developed prototypes with 1024 semiconductor lasers on one chip. This may be of use to the holostore technology by replacing the current laser, whose beam must be moved by the beam deflection system in order to reach different areas on the medium. Use of this technology may simplify the optics.
- The first incarnation of the Holostore technology will use write-once media. It is not apparent when a rewritable version will be available.
- Cost. No information has been determined yet.

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4.1.5 Addendum to Holographic Storage Review

By Dr. Gary R. Ashton
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In the second half of this study, additional information was collected about optical holographic storage systems. The purpose of this addendum is to summarize the new information.

The first commercial system produced by Tamarack Storage Devices, Incorporated is expected to be a write once (WORM) system which uses DuPont photo polymer as the recording media. References to DuPont photo polymers were collected as part of the second half of this study (Rhee et al. 1993). Additional information about the strontium barium niobate (SBN) work at Stanford was also collected as this is the media expected to be used in the second generation rewritable device (Hesselink et al. 1991). In fact, the SBN device is talked about by Tamarack Storage Devices, Incorporated much more than the WORM system.

An additional media development was noted. IBM has announced a new organic polymer for use in holographic memories (Anderson 1993). This is not the first such announcement from IBM as is evidenced by a 1991 reference to holographic material developments at IBM (Buderl 1991). Conference attendance, press announcements, and private conversations over the last few months indicate that IBM Almaden Research Center in San Jose, CA is expending significant effort on holographic storage even though there is little evidence of this from a survey of the published technical literature.

Two organizational announcements of interest also took place in recent months. First, a new company called Holoplex was formed to "exploit optical memories" (Bains 1993). This event is notable because of its timing and the fact that researchers at Caltech who have been very active in the technology founded the company. Second, the National Storage Industry Consortium (NSIC) recently announced a new division which will pursue research in the optical holographic storage area (NSIC 1993).

The optical holographic storage field was one of the more active areas of research studied in this report. There are several reasons for this level of activity. The idea of holographic information storage is an old one; several decades old (Zech 1992, Chen & Zook 1975). Progress in optical computing, optical communications, laser, and optical disk storage technologies are all contributing to the knowledge base and components needed to make optical holographic storage viable (Weber 1992, Psaltis 1992, Islam 1992, Ansari et al.

1992, Guilfoyle 1993, Stuart & Handschy 1993, Arnold 1993). In fact, the government is funding optical storage and computing research in a number of locations. Some of this work in optical storage is available in the form of government reports (Verber et al. 1992, Dornash & Ryan 1993, Callen & Gaylord 1993).

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4.2 Persistent Spectral Hole Burning

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4.2.1 Introduction

Persistent spectral hole burning was originally developed for the investigation of the physical properties of dopants or impurities in solids at low (liquid helium) temperatures using high resolution spectroscopy. At the present time, however, a new application is being investigated and research is being carried out in the U. S., Europe (including Estonia), Switzerland, Russia, Japan, and China into the possibility of using this technique for very high density optical memories (Moerner 1988).

4.2.2 Operation

The system is at the laboratory research stage at this time but it holds promise of being able to store data with a density of up to 10^{12} bits/cm². This would give 10 terabytes of information or about 5 billion pages of text in 100 square centimeters. As a comparison, one square foot would be more than that required to store the total information in the Library of Congress. Some authors have estimated that 10^{14} bits/cm² maybe possible which would enable the whole Library of Congress to be stored on one square inch of the media (DeCaro et al. 1991, Ollikainen 1993, Wild & Renn 1993).

The storage material is typically a host polymer or glass transparent in the visible wavelength which contains a dopant (guest) which has an absorption band in the visible wavelength region. Because the polymer is inhomogeneous, each molecule of the dopant does not see exactly the same surroundings as another and the result is a relatively broad absorption band. If a narrow beam of light from a tuned laser is made incident onto a small region of the polymer, a resulting change in the electronic states of those molecules absorbing at that wavelength modifies the absorptivity at the laser wavelength producing a hole in the absorption band (Figure 4.2.1).

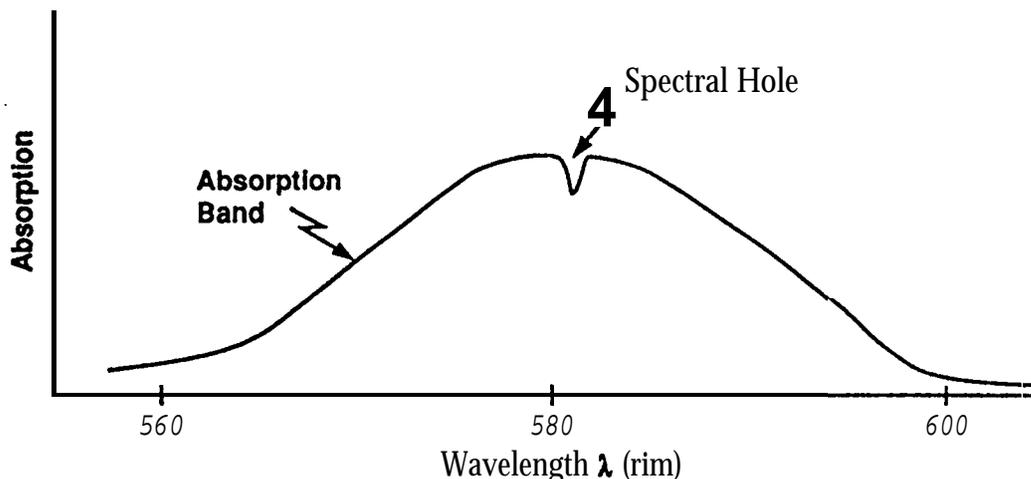


Figure 4.2.1

Because the information is stored at each (1@ point on the media by means of a series of laser beams at different frequencies in the absorption band, this system is often called Frequency Domain Optical Storage. In practice, the spot illuminated can be less than one micron and the laser wavelength can be set to a relatively large number of values, each one corresponding to one bit stored in the same one micron area of the media. For a $1\ \mu$ size spot, the density of spots is 10^8 bits/cm² and if one can select 100 different wavelengths within the absorption band, it follows that the bit density will now be 10^{10} bits/cm². Yoshimura et al. (1989) have shown that it is possible to have more than 600 different wavelengths within the absorption band and *this* would give 6×10^{10} bits/cm².

4.2.3 Photon Gated Materials

The main problem with the system described above is the fact that even though the information can be retained for a long time especially at low temperatures, each time the information is read back by measuring the absorption with a tuned laser, there will be some molecules that revert back to their original state. The result is a decrease in the signal for each read out resulting finally in a loss of the information. In order to stabilize the memory, photon gated materials must be used. The principle is shown in Figure 2.

In Figure 4.2.2, the incident laser beam will raise the energy level of the guest absorber from the ground singlet state S_0 to singlet state S_1 . This state can transfer to the triplet state T_1 which, without any additional illumination, would return to S_0 . However, when a second laser beam of the correct wavelength falls onto the sample on a continuous basis, the triplet state T_1 is

elevated to a higher level triplet state T_2 and from there, an electron transfer produces a stable acceptor state as shown. This will ensure stability of the spectral hole and will also produce an absorption band caused by the acceptor at a wavelength outside the "storage" absorption band being swept by the first laser. An example of a photon gated process via donor-acceptor electron transfer is shown in Moerner et al. (1987, p.153).

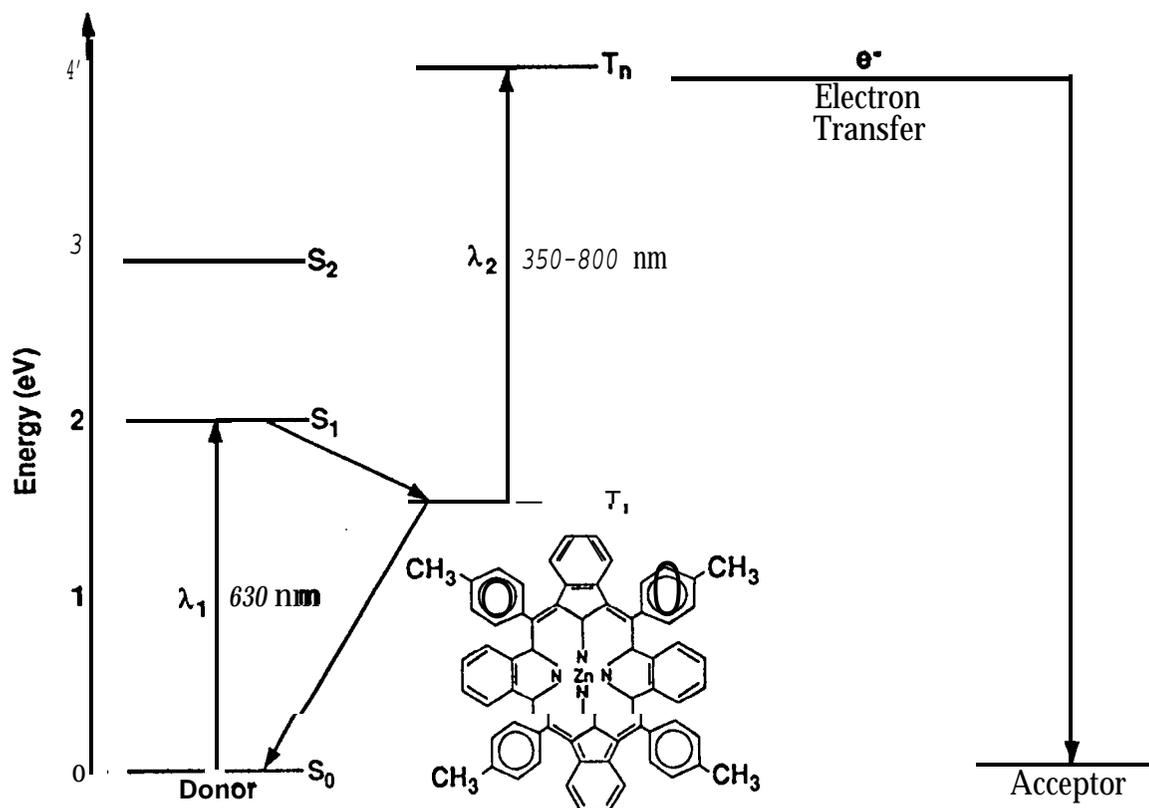


Figure 4.2.2. A photon gated process. Source: Moerner et al. (1987).

4.2.4 Electric Field Domain

An alternative method of storage has been to use the applied electric field domain instead of the (laser) frequency domain (Bogner et al. 1985). Applying an incident laser beam of fixed frequency, holes can be burned in the electric field domain by applying fields of up to 28 kV/cm at the same time as a laser pulse is applied. While the electric field strength is relatively high, the voltage required is in the range of 50 V because of the relatively thin storage medium. It has been proposed (DeCaro et al. 1989, Wild et al. 1989) that the frequency domain and the electric field domain can be combined to give a potential storage of 103×103 bits /micron of storage area.

4.2.5 Room Temperature Operation

One of the major drawbacks of these techniques is that the samples are best used at very low temperatures around 2K. i.e. at liquid helium temperatures. More recently, Arnold et al. (1991) have proposed using an ensemble of dyed microsphere at room temperatures and the results they obtained look interesting but need more investigation. On an alternate track, Hirao et al. (1993) have demonstrated room temperature hole burning in Sm^{2+} doped fluorohafnate glasses. At room temperature, the width of the stored holes are much wider than that at very low temperatures but data storage of between 10 and 100 bits/square micron are still possible. A further increase of 10-100 times can be achieved by using the applied electric field domain in addition to the frequency domain.

More recently, Hirao (1993) has shown that boric acid glass ($\text{Na}_2\text{O}-\text{B}_2\text{O}_3$) doped with samarium ions can also be used. With both of these room temperature systems, the read /write time using the current red laser is very slow (about one second) but this speed can be increased to give read/write times of a few microseconds by using a green laser as a gate.

4.2.6 Future Needs

The possibility of data densities of 10^{14} bits/cm² is very attractive. In order to achieve this, fine tuned lasers, preferably solid state lasers, will be needed that can, in the read mode, be made to sweep through the absorption band of the dopant or guest material in a very short time measured in nanoseconds or even picosecond so that a large data rate can be used. Similarly, the write speed also needs to be increased so that the large amount of information can be stored in an acceptably short time. In addition, a means of rapidly scanning the optical beam of the laser across a one to two cm sweep of the data storage media must be devised.

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403 Two Photon Three Dimensional Optical Storage

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4.3.1 Introduction

At this time, gigabytes of information are usually stored on hard magnetic disks, magneto-optic disks or on magnetic or optical tape. Disks offer rapid access to the stored information while tape offers greater volume density of the data but with much slower access times. One possibility of combining high volume density with rapid access is to store the information in a relatively transparent solid which can be addressed optically bit by bit by the intersection of two laser beams. Such systems are in the research stage at this time and are commonly referred to as two photon 3D optical storage systems.

4.3.2 Operation

Work in this area is currently being carried out by P. M. Rentzepis and colleagues (1989, 1990, 1991, 1992a, 1992b, 1993a, 1993b) at the University of California at Irvine and San Diego at La Jolla. One of the materials used in their investigation is a photochromic molecule of spirobenzopyran in a polymer matrix (Malkin et al. 1993). This absorbs in the UV but not in the visible wavelength region. When excited simultaneously by two intersecting beams (usually at right angles) using photons of 1064nm and 532nm wavelength, the two photons will correspond to a higher energy at a wavelength of 355 nm which is in the absorption band of the spirobenzopyran. The molecule changes to the merocyanine form which now absorbs in the green-red region of the visible spectrum. As a result, there will be a stored data bit at the intersection of the two beams in the form of a colored spot.

The data bits can be read out by the same process as the write cycle using two intersecting laser beams at a higher wavelength (lower energy). At the points where the data bits have been stored, there will be some fluorescence in the red (600 nm) and this could be detected as the presence of a data bit. The principle of operation is shown in the figure below:

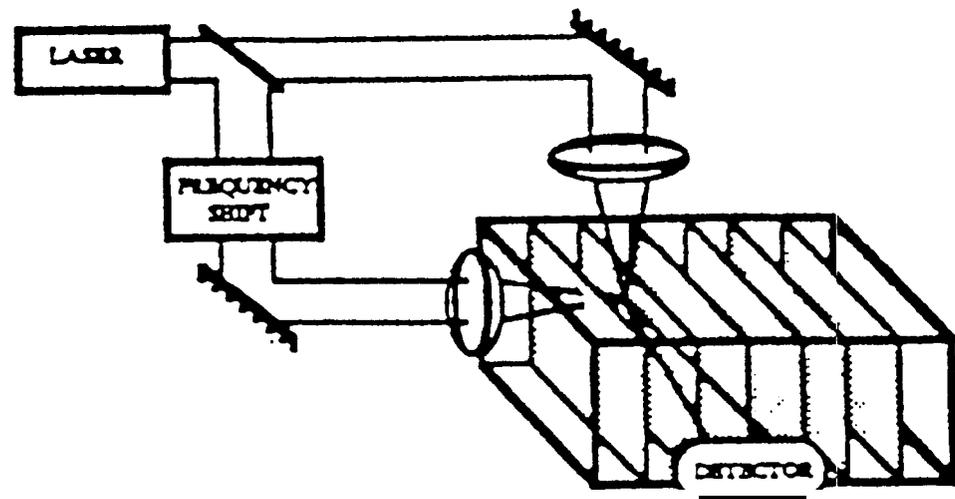


Figure 4.3.1 Schematic diagram of a 3D-memory device
Source: Dvornikov & Rentzepis (1992)

Light from a Nd/YAG laser is split into two beams and one beam is frequency doubled to give two beams of wavelengths 1064nm and 532nm which are then incident on a point in the solid at the same time producing the data bit. Alternatively, both beams can be frequency doubled to give the equivalent of a 266nm excitation at the point where the two beams intersect in the solid. It has been estimated (Parthenopoulos & Rentzepis 1989, Stein 1992) that the density of information storage is at least 6.5×10^{12} bits/cm³, which means that approximately one terabyte of information can be stored in a solid of one cubic centimeter in size.

It has been proposed (Hunter et al. 1990) that one of the beams be used to address a whole layer in the solid instead of one point. The second beam then quickly moves from point to point in that layer to write (or read) the data. In fact, with the future development of spatial light modulator arrays, data for the whole layer could be written or read at the same time in parallel to produce a very high rate of data handling. This possibility requires that the two-photon materials perform at lower light levels. It should be noted that M. E. Marhic (1991) has pointed out that this parallel method of data input/output could give rise to a significant loss of storage density because of diffraction effects.

4.3.3 Future Needs

The idea of using a solid to store information is very attractive because it enables data to be stored at a high volume density with rapid access to the information. However, one of the problems is the low sensitivity of the photochromic materials used which requires a high powered laser for the writing process.

A potential advantage of the solid store is the possibility of parallel writing or read out. This has been examined in detail by Esener et al. (1992) and they propose that with the rapid increase of computer power and speed, present memories (tape and disk) will become too slow. They make the point that using extremely short high intensity pulses from a Ti:Sapphire laser, one could address a whole sequence of planes in a short time to give data rates of one Terabit/second. This would require the development of new spatial light modulators and dynamic focusing lenses.

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5 MOLECULAR, CHEMICAL, BIOLOGICAL TECHNOLOGIES

5.1 Assessment of Molecular Electronic Memory Technology

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5.1.1 Summary of Molecular Electronics

The basic idea in molecular electronics is to reduce switching and memory elements to molecular dimensions. This could conceivably increase bit density to 10^{12} bits/cm² (Hopfield 1992), decrease cycle time to 10-11 sec (Hameroff et al., ClarkSon 1989), and reduce energy per bit cycle to 1 ev (Hopfield 1992, Rambidi 1993; Carter 1983a, 1983b, 1984). These values represent the potential for several orders of magnitude improvement in key parameters over conventional semiconductor or magnetic recording technology and would by themselves justify interest in molecular electronics.

However, there is also a second basic idea implicit in discussions of molecular electronics. This is to shift the paradigm for device assembly from lithography with masks and thin films to some form of molecular self assembly with organic synthesis, Langmuir Blodgett films, or biologic techniques (Carter 1983a, 1983b; Aviram 1988). Ultimately, molecular self assembly would reduce the cost per bit, and permit true three dimensional systems with bit densities as high as 10^{18} bits per cc (Carter 1983b).

Molecular electronics is a broad category which has been receiving considerable attention recently. In fact, interest has grown to the point where there are symposia dedicated to molecular electronics as well as a new society called The International Society For Molecular Electronics and **BioComputing**. Typical examples of molecular memory related research are efforts to model the potential performance of bimolecular switches based on enzyme **specificity in** tasks such as pattern recognition (Capstick et al. 1992, Aoki et al. 1992, Gretsenco et al. 1991), a scheme for computing with protein configurations (Hameroff et al.), or demonstration of rectification and transistor effects in organic thin films (Martinet al. 1993, Fichou et al. 1992). Also, some broad general principles for molecular memory systems have been set forth (Hopfield 1992, Rambidi et al., Kahn et al, Kahn 1988).

But this level of related research does not mean that commercialization of molecular electronic based memories is imminent. Molecular electronic memory systems are still in the concept stage without laboratory demonstration systems for bench marking. Biological systems certainly

constitute an existence proof for molecular self assembly, and clever chemical synthesis techniques have been used to synthesize structures analogous to wires and switches but without demonstrating functionality. Some molecular electronic materials such as bacteriorhodopsin may be used earlier as components in memories, but it appears that commercial application of complete molecular electronic memory systems is fifteen years away (Clarkson 1989, Armitage 1988).

5.1.2 Findings and Analysis - Molecular Shift Register Memory

It is necessary to focus on a specific molecular electronic memory system concept rather than on the extensive related research on potentially useful materials and components in order to fit the format of this study. The molecular shift register proposed by Hopfield et al. (1989, IEEE, Science) is arguably the most complete system concept. For example, this was the only system described in the 1988 Symposium on Molecular Electronics - Biosensors and Biocomputers (Hong 1988). It has consequently been selected as the straw man system for evaluating the state of the art in molecular electronic memories.

5.1.3 Operation

A shift register memory is a device which stores data bits in memory elements along a chain. At some time interval determined by an external clock, the whole string of data is shifted one unit down the chain in lock step. The head of the chain has some mechanism to input data bits in sequence with the clock, and the tail of the chain has a mechanism to read the data bits as they are shifted out of the end of the chain. Examples of shift register memories are bubble memories and conventional electronic shift register CCD's.

Hopfield et al. (1989, IEEE, Science) proposed using organic polymers of precisely defined length as the chain with the oxidation state of repeating components of the polymer serving as memory elements. Electrons correspond to data bits; they are shifted down the chain one unit every time an external light source is pulsed. The external light source thus serves as both clock and power source, providing an optical excitation energy on the order of 1 eV to each storage element in each clock cycle. The head of the polymer chain is attached to an electrode which controls the injection of electrons into the polymer chain shift register. The tail of the polymer chain is connected to an electrode which detects the arrival of electrons. Hopfield et al point out that if the polymer chains are 600 repeat units long, then the length of the chains would be about 1.2 μm which is compatible with conventional lithography for electrode fabrication on silicon wafers. If about 5000 oriented chains were hooked up in parallel between the two electrodes, then sufficient

electrons would arrive in each clock cycle to be detected by a conventional silicon detector. A conventional silicon wafer circuit thus could provide the interconnection between the ultra small molecular domain and ordinary silicon based electronics.

5.1.4 Advantages of the Technology/Product Development

A molecular shift register device proposed by Hopfield et al could increase memory density by two orders of magnitude relative to silicon semiconductor technology. This memory would also be non-volatile, unlike present DRAM or SRAM. Non-volatile single chip memories of 1 GByte are conceivable with this technique.

5.1.5 Limitations of the Technology

The major limitation in the present concept is that low light adsorption in the thin polymer film would require excessive power to ensure photo excitation of each element during each cycle. This would restrict data rates to well below 1 MHz.

5.1.6 Unresolved Issues

The quantum efficiency of the uni directional charge transport must be demonstrated.

The capability for precise synthesis of the specific polymer chains suggested must be developed.

The data rate must be dramatically increased.

The potential for low cost per bit must be demonstrated.

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6 FINDINGS AND ANALYSIS

Many people will read this report with many different applications in mind. A preference for one technology over another is only possible on a rational basis by comparing the facts about the technologies along with the application. In preparing this report we did not have any prior knowledge of the reader's intended application for the technologies presented. Without this application knowledge, this report can not show that one technology is better than another or that one technology is preferred over another. This leaves the decision makers with the task and responsibility of reading this report and gathering application information in order to make their own technology choices.

Analysis of the data in this report then means to present the benefits and limitations of the technology and the risks associated with its development or use. Analysis should be strictly based on verifiable facts and be independently verifiable by other researchers. In new embryonic technologies there are often few technical references and few verifiable, well documented facts.

Judgment or opinion should be used for decisions only if absolutely necessary to fill in the space where there are missing facts. Please be careful to separate analysis from opinion and from suitability for a particular application. Opinion represents the judgment and biases of the individual expressing the opinion and is not based completely on verifiable facts. The people responsible for the judgments or opinions expressed in this report are identified for each technology section as the author of the section.

6.1 Research Activity Levels

In order to judge the activity in each of the technology areas presented in this report, an on-line library search of several databases was carried out for technology areas of interest. The search results were reported as the number of citations per year for the years 1988 through 1993. Because of lags in indexing and abstracting, the 1993 results cover from about 10.5 to 11 months of 1993. The databases searched are detailed below.

AEROSPACE DATABASE (1962 to the present) contains over 1.3 million references to the international literature of aerospace research and applied technology. This source regularly scans over 1600 journals, plus books, theses, conference papers, and technical reports, and corresponds to the printed publications, International Aerospace Abstracts and Scientific and Technical Aerospace Reports.

COMPENDEX (1970 to the present) is a computerized version of Engineering Index. It covers international journal literature, conference proceedings, technical reports, and books on all aspects of engineering.

ENERGY SCIENCE & TECH. (1974 to the present) is a multi-disciplinary file containing worldwide references to basic and applied scientific and technical research literature. Energy conservation, fossil fuel, solar, geothermal and advanced energy systems, environment and safety, nuclear energy, and national security are among the topics covered.

INSPEC (1969 to the present) provides international coverage of literature published in electronics, computers and computing, physics, electrical engineering control engineering, and information technology. Sources abstracted: journal articles, conference literature, books, technical reports, and dissertations.

NTIS (1964 to the present) is a database of government sponsored research, development, and engineering reports and studies done by government agencies, their contractors or grantees. Subjects covered include: physical sciences, technology, engineering, biological sciences, medicine, agriculture and social sciences.

	1988	1989	1990	1991	1992	1993	Totals
DRAM or SRAM	403	459	477	572	477	237	2625
Holographic	63	107	108	110	129	102	619
EEPROM	92	93	70	92	79	68	494
VBL	70	45	40	65	19	9	248
Flash	29	20	33	38	31	23	174
Magnetic Bubble	53	30	29	43	13	1	169
FRAM	16	15	28	33	41	9	142
Josephson Junction	14	30	15	33	16	19	127
Magnetic Core	12	18	13	26	20	3	92
Spectral Hole Burning	8	7	16	18	24	11	84
Biological or Molecular	9	8	6	12	6	7	48
MRAM	5	4	8	11	12	2	42
Two Photon Three Dimensional	0	2	13	7	4	14	40
Single Electron Transistor	1	1	0	5	12	9	28
Hall Effect	1	3	5	6	0	5	20
Magnetic Cross Tie	3	3	2	2	4	4	18
Plated Wire	3	1	1	0	0	0	5

Table 6.1.1. Technical Publication Activity for 1988 to 1993 by year
This table shows the number of references located in the library databases for each year from 1988 to 1993, The total number of references found for the search period are indicated in the right most column.

Total Number of Citations over 5 years

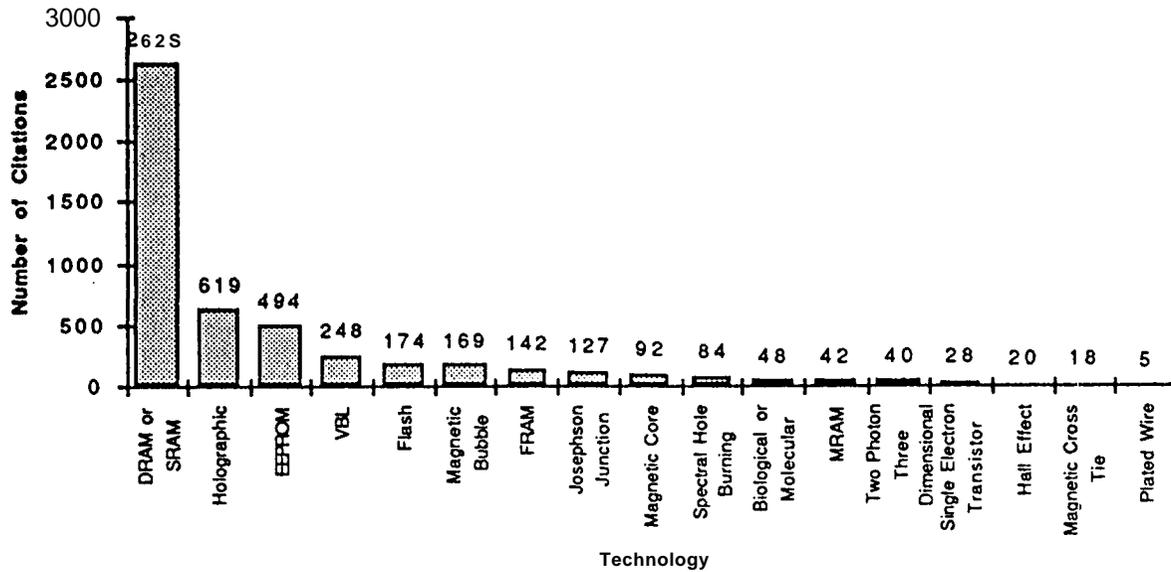


Figure 6.1.2. Total Technical Publication Activity for 1988 to 1993

This graph shows the total number of references found for the period from 1988 to 1993. The total number of references located in each technology area are printed above the bars. The data has been sorted from the largest number of references to the smallest.

Industrial Commercial	Government Commercial	Functioning Prototype	Research and Development
EEPROM	Magnetic Core	MRAM	Single Electron
FLASH	Plated Wire	FRAM	Josephson Junction
ROM	Cross-Tie	VBL	Photon Echo
SRAM	Magnetic Bubble	Holographic	Spectral Hole Burning
DRAM	NVSRAM		Molecular or Chemical
			2 Photon 3D

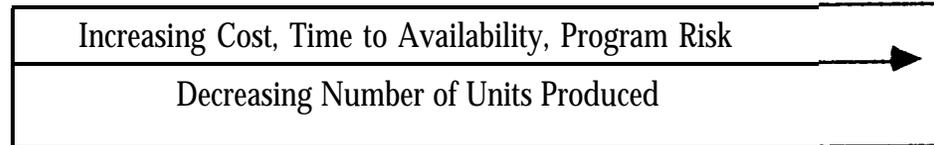


Figure 6.1.3. Technology Classifications

The figure indicates four classifications for the technologies presented in this report as well as ranking for cost, time to availability, risk, and number of units produced.

The numbers of technical publications for each area shown in the table and graph above can be understood by considering the location of the technology in its usable product life cycle. For instance the largest activity is expected to occur in technologies that are Industrial Commercial and mature or middle aged. This is because these types of technologies have the largest commercial economic use, are proven to be low risk, and have the largest research and development investments. These relationships are detailed in the table below.

For future technology investment purposes, technologies are represented in order of increasing risk as, young Industrial Commercial technologies, young Government Commercial technologies, young prototype technologies, and new technologies. Older technologies seldom represent areas of acceptable investment risk due to projected technological obsolescence. Established technologies of high commercial interest usually require unacceptable and large capital investments to influence.

Technology	Category	Location in Product Life Cycle	Anticipated Activity Level
Magnetic Core, Plated Wire, Cross-Tie, Magnetic Bubble	Government Commercial	Old	Small and Decreasing
EEPROM, ROM, SRAM, DRAM,	Industrial Commercial	Middle Aged	Large and Steady
Flash	Industrial Commercial	Young	Moderate and Increasing
NVSRAM	Government Commercial	Young	Small
MRAM, FRAM, VBL, Holographic	Prototype	Young	Small and Increasing
Single Electron, Josephson Junction, Photon Echo, Spectral Hole Burning, Molecular or Chemical, Two Photon Three Dimensional	Research and Development	Never a product	small

Table 6.1.4. Reasons for Technical Activity Levels

This table explains the general level of activity measured by number of technical publications for the technologies examined in this report. It uses the category together with the location in the product life cycle to predict the activity level and rate of change of the activity level.

6.2 Technology Comparison Matrix

The following matrix lists the estimates of cost per megabyte, time to maturity, development funding, risks and benefits of each of the technologies presented in this report. The matrix is not a substitute for a full analysis of the specific application needs and the technology, but does allow a general overview and comparison of the technologies. Magnetic disk and tape technologies are included in the matrix as familiar points of reference for comparison purposes.

Table 6.2.1. Technology Comparison Matrix

Type of Memory	Cost per MByte (\$)	Years to Maturity	Development COST (\$)	Risk (minuses)	Benefit (pluses)	Density (MByte/cc)	Power
Magnetic Bubble	100	Zero	Zero	Power use, speed, limited density	Known technology, radiation hard	0.008 to 0.005	1-100 W/Mbit/see
VBL	0.01 to 5	5 to 10	5 to 15M	Losing bubble technology base	Dense, radiation hard, few fabrication steps	1 to 100	0.01 to 1 W/Mbit/sec
Magnetic Core	100 to 1000	Zero	Zero	Size, power, cost, speed	Robust, reliable, radiation hard	0.0002 to 0.001	1 to 60 W/Mbit/sec
Optical Holographic	0.06 to 0.10	5 to 10	>25M	Media, optics, lasers	High speed, parallel read	16.5	Less than 15 watts
MRAM	10.00	5 to 10	100M	Speed/density tradeoff, Materials development	Few fabrication steps, radiation hard, NDRO , nonvolatile, fast write, infinite durability, high density	1x10 ⁹ bytes/cc (10 ⁸ /cm ²)	0.025 W/Mbit/see read or write
GMRAM	10.00	5 to 10	100M	Materials development	Few fabrication steps, radiation hard, NDRO , nonvolatile, fast write, infinite durability, high density	1 x 10 ⁹ bytes/cc (10 ⁸ /cm ²)	0.025 W/Mbit/sec read or write
Josephson Junction	10.00	10	1B	Low temperature operation	Extremely high speed (picosec)	1x10 ⁹ bytes/cc (10 ⁸ /cm ²)	0.001 W/Mbit/sec
Single Electron Transistors	10.00	15	10B	Low temperature operation, extreme lithographic needs, some volatility	Extremely high density/high speed (picosec)	1x10 ¹² bytes/cc (10 ¹¹ /cm ²)	0.0001 W/Mbit/sec
Flash EEPROM	30-55 Now Follows Semiconductor Trends	2	Enormous (industry dominated)	Slow write cycle, Number of read/write cycles	Known technology, commercially driven	1.7-2.6 PCMCIA Card, Follows Semiconductor Trends	125-350 mW operating; 2 mW sleep
FRAM	2000 Now Follows Semiconductor	3 to 5	Large, industry driven	Low density, Number of read/write cycles, Ferroelectric materials	Low power, individually addressable bits	340 KByte/cc in chip package, Follows Semiconductor Trends	0.5 mW operating, 0.12 mW sleep

(continued)

Table 6.2.1 Technology Comparison Matrix - *Continued*

Type of Memory	Cost per MByte (\$)	Years to Maturity	Development cost (\$)	Risk (minuses)	Benefit (pluses)	Density (MByte/cc)	Power
Magnetic Disk (2 GByte)	1	Zero	Zero	Head crash	Well known, random access	3.1	12.7 watts
Magnetic Tape	0.4 (drive & 1 tape) 0.03 per Tape)	Zero	Zero	Media wear and archivability	Low cost, well defined growth paths	1.8	15watts running or 3.1 watts idle
2 Photon 3D	Low	10-20	Unknown	High power laser	Parallel Processing	10^5	Laser Dependent
Spectral Hole Burning	Very Low	10-20	Unknown	Slow speed, Low Temperature	Very high density	108	Unknown
Plated Wire	100to 1000	Zero	Zero	Power use, speed, limited density	Known technology, radiation hard	0.00004 to 0.001	1 to 40 W/Mbits/sec
Chemical and Molecular	Very Low	>20	Very High	Materials, electrical interface	Dense, possible simple fabrication	10^{11}	10^{-13} W/Mbit/sec (theoretical)

6.2.1 Descriptions of Entries in Table 621

Magnetic Bubble Memory

Magnetic bubble technology is a mature technology. Sagem Corporation and Hitachi Corporation are the known suppliers of bubble memories. The current magnetic bubble technology base is relatively small. Magnetic bubble memories costs are approximately \$100/MByte. Magnetic bubble memories offer nonvolatile data storage and radiation hardness. However, magnetic bubble memory performance in terms of data rate, power dissipation, and volumetric storage capability is limited. Based on Sagem Corporation's 32 Megabyte EBS 2801 magnetic bubble mass memory system, volumetric storage density is 0.00079 MBytes/cc, based on 32 Mbyte storage capacity in a unit that is 34.2 cm high, 38.7 cm long, and 30.6 cm wide. Of this volume, 54% of the volume is tied to the memory pages, and the remaining volume is used by the controllers, power supply, chassis, and cabling. System mass is determined by the number of memory pages, number of controllers, the mass of the power supply, and the remaining mass of the chassis and cabling. a 32 Byte system has a mass of 40 kg, of which 60% of the mass is tied to the memory. System power consumption ranges from 62 W (typical) to 77 W (worst case) for an 800 kbyte/sec maximum data transfer rate which is produced by eight active chips.

Vertical Bloch Line (VBL) Memory

Vertical Bloch Line (VBL) storage technology is a new/emerging technology. Research and development of VBL technology and VBL prototype chips has been performed by Hitachi, NEC, and Sony Corporation in Japan and Sagem Corporation in France. An activity is underway to produce VBL prototypes of 16 Mbit to 256 Mbit chips in the U.S. VBL storage chip costs in volume are projected to range from \$0.01 to \$5 per MByte, depending on fabrication costs, yield, and chip capacity. For example, a wafer yielding one hundred 32-Mbyte chips at a wafer processing cost of \$1000 yields a cost of \$0.3/Mbyte. VBL memories potentially offer nonvolatile data storage, radiation hardness, and data erasability at reasonable data rate, power dissipation, and high areal and volumetric storage capacity. For example, a chip using 2 micron magnetic domains with 1 micron lithography produces an areal storage density of 3 Mbytes/cm² (i.e., 25Mbits/cm²) which can be used to form 2 Mbyte (i.e., 16 Mbit) or 8 Mbyte (i.e., 64 Mbit) chips. If 1 micron magnetic domains using 0.25 micron lithography are used, an areal storage density of 25 Mbytes/cm² (i.e., 200 Mbits/cm²) is generated for use in making 32 Mbyte (i.e., 256 Mbit) chips. If 625 micron (i.e., 25 roil) or 250 micron (i.e., 10 roil) device pitches can be realized for 25 Mbyte/cm² VBL technology, VBL volumetric storage density in a multi-chip module becomes 400 and 1000 Mbytes/cc, respectively. VBL chip power consumption is expected to range approximate y from 10 mW to 1 W per Mbit/s, depending on whether the

device is used primarily as a data input/output device or as a block-search/data retrieval device.

Magnetic Core Memory

Magnetic core memory technology is a mature technology. Ampex Corporation is a known suppliers of core memories. The current magnetic core technology base is relatively small. Magnetic core memory costs are approximately \$100 to \$1,000 per MB yte. Magnetic core memories offer nonvolatile data storage, random access, and radiation hardness. However, magnetic core memory performance is limited, relative to existing technologies, in terms of data rate, power dissipation, and volumetric storage capability. Based on Ampex Corporation's 256 kbyte (128 Kwords with 18-bit words which include 2 parity bits) MESA-128 magnetic core memory system product, volumetric storage density is 0.00019Mbytes/cc, based on 256 kbyte storage capacity in a unit that is 16.3 cm long, 22.9 cm wide, and 3.6 cm high. System mass is 2.1 kg. Maximum system power consumption is 53.6 W based on a system with a 900 ns maximum full cycle time (including read/restore and clear/write cycles), 1000 ns minimum split cycle time (including read /modify/ write), and a 350 ns access time.

Optical Holographic Memory

Information on costs of the Tamarack Systems Inc. RAT-Pack storage unit which uses fifty \$1 tiles in a 50 gigabyte storage unit can be found in; "MCC's Tamarack Storage Devices Spinoff, Government Computer News, March 29, 1993 as well as in "Tamarack Storage Devices Inc./Holography for Data Storage", Industry Week, December 20,1993.

The cost of the 50 gigabyte RAT-Pack is expected to be \$3000 to \$5000. The RAT-Pack is expected to be in a 5.25 inch form factor so that the dimensions are approximate y 83.8 mm high by 147.3 mm wide and 216 mm deep. This gives a data storage density of 16.5 megabytes per cubic centimeter. As the RAT-Pack is designed to replace current tape and disk drives it is expected to use less than 15 watts of power. The first generation write once and read many times (WORM) system is due out in the second quarter of 1994. The second generation rewritable system is due out in 1996 according to the Industry Week article. The funding expended by Tamarack Systems inc. already exceed \$25 million.

Magneto Resistive Random Access Memory (MRAM)

Cost per MByte (\$): \$10 (Cell size and number of layers less than or equal to FLASH, EEPROMS, or DRAM.

Sources for other table entries: *Defense Electronics*, October 1991, p. 82; G.

Granley (Honeywell); J. Daughton (NonVolatile Electronics).

Giant Magneto Resistive Random Access Memory (GMRAM):

Cost per MByte (\$): \$10 (with cell size and number of layers less than or equal to FLASH, EEPROMS or DRAM)

Sources for other table entries: *Defense Electronics*, October 1991, p. 82; G. Granley (Honeywell); J. Daughton (Nonvolatile Electronics).

Josephson Junction Memory

Sources for table entries: *Defense Electronics*, October 1991, p.82; K. Lihkarev (SUNY - Stony Brook), A. Goldman (University of Minnesota).

Single Electron Transistors

Sources for table entries: *Defense Electronics*, October 1991, p.82; K. Lihkarev (SUNY - Stony Brook), A. Goldman (University of Minnesota).

Flash Electrically Erasable Programmable Read Only Memory (EEPROM)

The price of FLASH memory has been published in reference articles and also ads from the various manufacturers. All of the prices seem to be in the range published in the table. This price is the same whether in chip form or in PCMCIA memory cards. The published dimensions of the PCMCIA Type I and II cards were used to calculate volume to arrive at the density number. These numbers are certainly subject to change due to the competitive and ever changing nature of the industry. References 10, 12 in the section on FLASH were used for the power, price and density data.

Ferroelectric Random Access Memory (FRAM)

Data was gathered from a phone conversation and discussion Ramtron tech service. Their current product is at 16 Kbit an available in a 0.635X 0.53 X 0.17 cm chip package priced at \$4 ea./1 000 lot. This data was used to calculate cost/MB and density. The power requirements were supplied by Ramtron. The data used to fill in the matrix was gathered from published papers and from the conversation with Ramtron.

Two GigaByte Magnetic Disk

The industry wide average cost per megabyte for rigid magnetic disk storage is approximately one dollar at present. The technology is already mature with no development cost as it is available from IBM now. The following

information is available from the specification sheet for two gigabyte IBM Disk drive Models 0664-M1H and NIH. The 2 gigabyte drive is 153.2 mm long by 41.3 mm high and 101.6 mm wide. This results in a density of 3.1 megabytes per cubic centimeter. The power consumption of the drive is listed as 12.7 watts.

Quarter Inch Cartridge (QIC) Magnetic Tape

Tandberg Data's model TDC 42202.5 gigabyte quarter inch cartridge (QIC) tape drive is used for this example. 3M announced the introduction of the Magnus 2.5 GB data cartridge for use in this drive in November of 1993. The 3M suggested list price of the cartridge was stated as \$78 at that time. The OEM or distributor cost of the drive is somewhere between \$600 to \$800 based on calls to Tandberg's list of distributors. Thus the end user price of the drive with one 2.5 GB data cartridge is estimated to be about \$1000. This makes the cost per megabyte of storage \$0.40 for one drive with one unit of media installed. The cost of storage considering the cost of the tape cartridge alone is \$0.03 per megabyte. The technology is already mature with no development cost as it is available now. The drive uses 3.1 watts when idle and 15 watts when running. The dimensions of the unit are 43 mm high by 149 mm wide and 216 mm deep. This is a 5.25 inch half height form factor. The cartridge dimensions are 1.6 cm thick by 10.1 cm wide and 15 cm long. This yields a cartridge data density of 10.3 megabytes per cubic centimeter.

Spectral Hole Burning Memory

The cost per megabyte is expected to be very low because of the relatively low cost of the materials and the very high data density which can be stored using this technique. Work is being carried out at many locations throughout the world and competition is high. For this reason, it is estimated that the time to a working prototype is in the range of 5-10 years. The development costs are unknown at this time.

On the negative or risk side is the relatively low sensitivity of present materials

The main attraction of this system is the very high data storage density that can be reached by storing up to one million bits on the same micron sized spot that is used at present to store only one bit. As a result, it is estimated that up to 10^8 megabytes per cc can be stored using a combination of the frequency domain and the electric field domain assuming that 10 layers of the material can be stacked in one cm.

The power required for operation of the system will depend on improvements to be made in the sensitivity of the material and this has been shown to depend not only on the dopant or guest but also on the host material.

2-Photon 3D Memory

The cost per megabyte will be low because of the low cost of the materials being used. The main work on this system is located at the University of California and, while there have been signs of interest in the literature, no publications of active work at other locations have been found. For this reason, it is expected that it will take between 10 and 20 years for a working prototype to be produced. The development costs are unknown at this time.

On the negative or risk side is the fact that relatively high powered lasers are required to operate the system with the materials available at this time.

On the positive or benefit side is the fact that the system can be used for parallel input/output to give very high data rates to match the expected requirements of future computers.

The potential density of data storage is 10^5 MByte/cc but this will be significantly lower for parallel input/output operation.

The power requirements needed for an operating prototype are difficult to estimate at this early stage.

Plated Wire Memory

Plated wire technology is a mature technology. Honeywell Corporation is a supplier of plated wire memory, while companies such as Burroughs and ICT have produced plated wire memories in the past. The current plated wire technology base is relatively small. Plated wire memories costs are approximately \$1,000/MByte. Plated wire memories offer nonvolatile data storage and radiation hardness, but, relative to existing technologies, offer limitations in performance in terms of data rate, power dissipation, and volumetric storage capability. Plated wire memories are available in 13 cm by 15 cm boards with 64 Kbits capacities, leading to a volumetric storage density of approximately 0.00004 MByte/cm³ assuming a board spacing of 1 cm. Typical currents range from 50 mA to 500 mA into 50 ohms, so that power consumption ranges approximately from 2 to 20 W for a 1 Mbit/see rate.

Chemical and Molecular

Cost per MByte: Very low, assuming some form of self-assembly is achieved

as contemplated in references [5-8].

Years to Maturity: Estimates are about 15 years until products appear commercially (3,12). Another five years would be a minimum to maturity.

Development Cost: Very high. This judgment is based on the tremendous number of unknowns.

Risk: Several authors, e.g., Hopfield (1992).

Benefit: Several authors, e.g., Carter (1983a, 1983b, 1984).

Density Carter (1983a, 1983b, 1984).

Power: Theoretical limit, based on 1 ev per bit cycle Carter (1983a, 1983b, 1984).

6.2.3 Technology Comparison Bibliography

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7 CONCLUSIONS

Several solid state memory technologies have been presented and evaluated in this report. Broadly speaking, the technologies are in the areas of electrical, magnetic, optical, and molecular memory. Of these only integrated circuit technology in the form of ROM, DRAM, SRAM, PRAM, EEPROM, or flash EEPROM enjoys wide commercial acceptance. The remaining technologies must compete with integrated circuit memory technology as well as the traditional moving media technologies of magnetic disk, optical disk and magnetic tape to become commercially successful. This is not easily accomplished because the traditional storage technologies show no clear limit to density and cost improvements and at the same time enjoy a tremendous research and development budget in comparison to the non-commercial solid state memory technologies presented here. An example of the power of commercial markets to set the pace for technology development is the recent use of integrated circuit flash memory in PCMCIA cards for the personal, mobile, computing market. Many solid state memory technologies will be used only in niche markets for specialized applications in the next five to ten years. The only technologies which have presently emerged for use in high volume, low cost markets are listed in the above table as industrial commercial technologies.

GLOSSARY

DRAM Dynamic Random Access Memory. A memory chip which stores bits of information in charged capacitors. In DRAM the data will disappear in less than a second unless refreshed. This type of memory is cheaper and allows more storage per chip than SRAM.

EEPROM: Electrically Erasable and Programmable Read-Only Memory. EEPROMS can be programmed and erased electrically while connected in the circuit.

ETOM: Electron Trapping Optical Memory. An optical recording method where phosphor materials with rare-earth dopants are used to store information. The material is illuminated with a blue laser to transfer energy to electrons in the phosphor which then store the energy in electron traps. Information retrieval is triggered by the absorption of infrared photons which release the stored energy as visible light that is detected. The amplitude of light emitted is used to indicate the stored information.

The transfer of data is based on a quantum effect which involves exciting a luminescent ion and passing its excited electron to a nearby trapping ion. Once bound to the new ion, the electron falls to the ground state of the ion; this traps the electron. This is the stored state and is a stable configuration for the electron. It will remain trapped until a photon of the read light source excites it from the ground state to the excited state. From here it can migrate back to luminescent ion and fall to the ground state. The transfer back to the ground state is accompanied by the emission of a photon which is detected by the disk drive and indicates stored data. Data can be stored at four levels per data location, but needs to be refreshed after a few reads.

FLASH Memory: This type of memory is also called FLASH EEPROM. An EEPROM that cannot be erased by bytes but can be erased as an entire chip or in large sections of the chip. This is a semiconductor memory in the category of programmable ROM devices. The unique features are that it is non volatile and can be electronically erased via programmed instructions. Feature size and capacity continue to increase. A plus for this device type is its circuit density while the negative is its limited rewrite capability 10,000 to 100,000 cycles and the necessity to erase the device a block at a time rather than one byte at a time.

FRAM: Ferroelectric Random Access Memory. A FRAM memory is built by replacing the conventional capacitor in a standard DRAM circuit with a thin film ferroelectric capacitor. The ferroelectric capacitor retains the capacitor's voltage after an externally applied electric field is removed.

Holographic Memory Information storage by recording the interference patterns of waves. This term usually refers to optical waves although sound or other waves can be used. Data is stored by intersecting two separately focused laser beams within the storage media. The first beam contains the image. The second beam, called a reference beam, when intersected with the first beam, produces an interference pattern, which is rerecorded by the media. Data is retrieved by shining the reference beam alone through the media. Positive features of this technology are the ability to store images directly, the potential for high density storage, and fast access.

MRAM: Magnetoresistive Random Access Memory. A memory chip that stores information magnetically and reads the information by the magneto resistance effect. The magneto resistance effect is the change in resistance of a conductor due to the presence of a magnetic field.

Magnetic Bubble Memory: Information storage by the creation and manipulation of cylindrical domains of reversed magnetization (magnetic bubbles) in a thin film of magnetic material.

Near Field Scanning: This recording method uses a flying head technology in combination with laser recording technology. The laser light source is focused through a fiber optic device and mounted on the flying head to position the read/write optics as close to the media as possible without touching the media. The advantage of this technique is a recorded bit smaller than the diffraction limited spot expected in traditional optical storage techniques.

Photo-Chemical Memory Information storage by inducing chemical changes in a media due to exposure to light.

Photon-Echo: A technique in which information is stored in the form of optical pulse trains in a media and retrieved as a stimulated emission of an "echo" pulse train by a single read laser pulse. The data is stored in the media as a modulation of the distribution of populations in the energy levels of the ions in the media.

SERODS: Surface-Enhanced Raman Optical Data Storage. Optical data storage based on optical Raman scattering. This technique was invented at The Oak Ridge National Laboratory by Tuan Vo-Dinh.

SRAM: Static Random Access Memory. A memory chip which stores bits of data in an array of flip-flops. A bit once written to SRAM stays there until rewritten unless the power is turned off.

Scanning Tunneling Microscopy This recording method uses a very sharp pointed cathode probe in close proximity to a conducting media. This technology was originally demonstrated in a vacuum chamber, but **has** recently been demonstrated in an air environment. Writing is accomplished by pulsing an electrical current **sufficient** to "pit" the media. Reading is accomplished by passing the probe over the previously pitted area and reading out low level current flow changes through the probe. Pit spacing is measured on the atomic scale, resulting in high density recording. Pit sizes are on the order of 3-6 nm.

Spectral Hole Burning Memory Information storage by optically producing features in the absorption or fluorescence spectra of the media. The features in the spectra are called "spectral holes". The spectral holes are written by a narrow wavelength laser and read by measuring the spectra of the media.

Two-Photon 3D Optical Memory An optical method of data storage and retrieval in which two light beams spatially and temporally overlap in the media volume to produce reversible and detectable changes in the media.

VBL Memory Vertical Bloch Line Memory. A nonvolatile memory chip using magnetic garnets to store information in Vertical Bloch Line (VBL) pairs. A twist of magnetization in the magnetic domain wall is a Vertical Bloch Line, and two such twists form a VBL Pair.