

Paul M. Stella  
M/S 303-308  
4800 Oak Grove Dr.  
Jet Propulsion laboratory  
Pasadena, CA 91109  
(81 8) 354-6308  
Fax: (818) 393-4272  
category 7B (or 6A)  
oral presentation preferred

## PV TECHNOLOGY FOR LOW INTENSITY, LOW TEMPERATURE (LILT) APPLICATIONS

Paul M. Stella, Frederick S. Pool, Peter A. Iles\*, and Marc A. Nicolet†

Jet Propulsion laboratory, 4800 Oak Grove Dr., Pasadena, CA 91109

\*Applied Solar Energy Corporation, 15251 East Don Julian Rd., City of industry, CA, 91749

†California Institute of Technology, Pasadena, CA, 91125

As a result of the recent NASA emphasis on smaller and lower cost space missions, PV is now being considered for a wide range of missions that involve operation at solar distances of 3 AU or greater. In the past, these missions would most likely be larger and utilize an RTG (radioisotope thermal-electric generator) as the preferred power source. Historically, silicon solar cell behavior at these distances has been compromised by a number of degradation mechanisms including shunting, non-ohmic back contacts, and the "broken knee" (or "flat spot") curve shape. The former two can usually be neglected for modern silicon cells with back surface fields, but the latter has not been eliminated and can be highly degrading. This problem has been identified with random and localized diffusion at the top surface contact metallization/silicon interface which leads to structural changes in the local junction. This is believed to create a resistive metal-semiconductor-like (MSL) interface in parallel with the junction which leads to the characteristic forms of the LILT "broken knee"<sup>1,2</sup>.

This paper discusses the development of a TaSiN contact barrier that can be applied to conventional solar cells, with minimum process changes, that will prevent the localized occurrence of the MSL structure in the junction. The behavior of the barrier was evaluated by the fabrication of large area diodes with full top surface metallization in order to maximize the formation of any localized junction defect regions. Dark forward I-V tests were obtained at room temperature and at 75K to evaluate the resultant cell characteristics. The cells were also subjected to long term high temperature thermal soaks (600C for 20 minutes) in order to provide an accelerated stress test for evaluating the barrier stability. Test results showed that the barrier samples were quite stable whereas the controls (without the TaSiN barrier) exhibited a large increase in the dark forward current (Figures 1 and 2). These results indicate that the contact barrier can prevent occurrence of the "broken knee" cell degradation. The barrier materials and

formation methods will be discussed in the complete paper, along with implications for implementation in high efficiency cell production.

As part of the investigation into silicon cell development for LLT conditions, an analysis was made for a typical mission application. Array performance was calculated for 5 AU operating conditions assuming a 50 w peak power requirement at that distance. Alternative approaches were examined, including cell selection for conventional devices with reduced LLT degradation and GaAs/Ge substitutes. It was concluded that the implementation of silicon cell processing to avoid the LLT degradations, although not always cost effective for any single mission, would provide significant economical benefits when examined in terms of multiple missions.

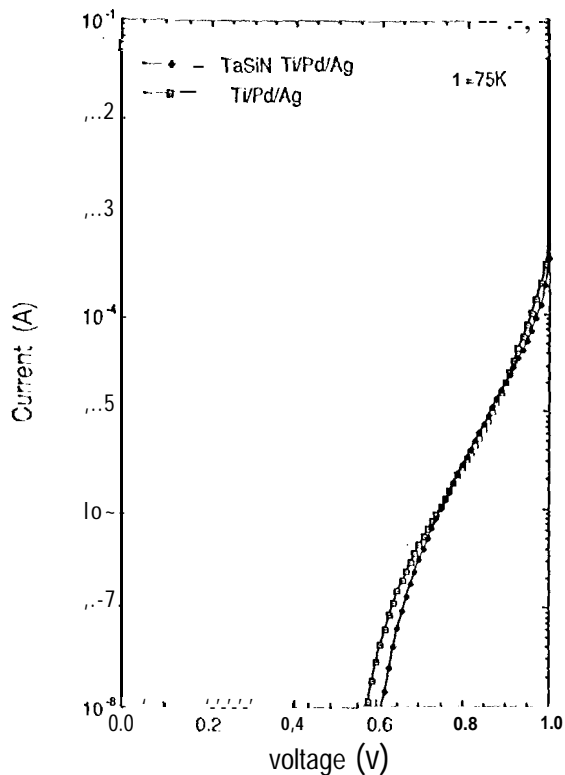


Figure 1. Dark I-V before 600C soak

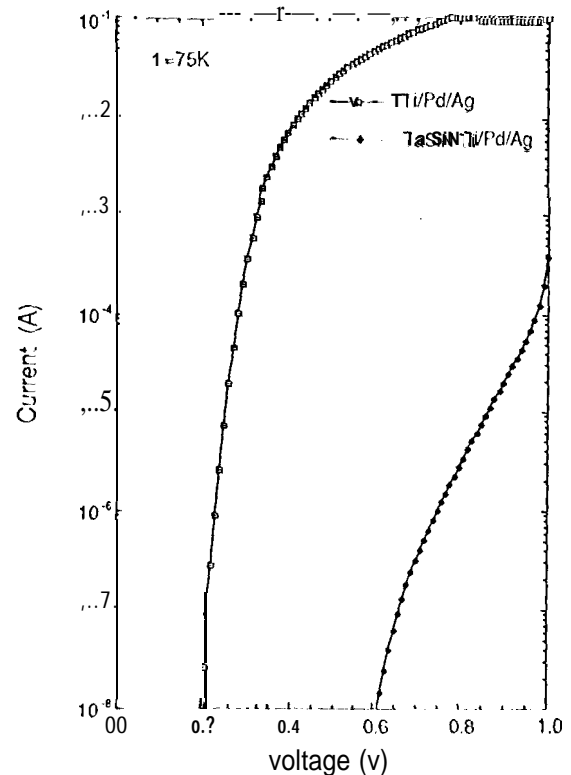


Figure 2. Dark I-V after 600C soak

1. Weizer, V.A. and Broder, J. D., "On the Cause of the Flat Spot Phenomenon Observed in Silicon Cells at Low Temperatures and Low Intensities", presented at the 15th IEEE Photovoltaic Specialists Conference, May, 1981
2. Payne, P.A. and Ralph, E.L., "Low Temperature and Low Intensity Characteristics of Silicon Solar Cells", Conference Proceedings of the 8th Photovoltaic Specialists Conference, 1970, p.135