DESIGNING FOR SMALL VOLUME ASSEMBLY OF ADVANCED ELECTRONIC PACKAGES

by

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ABSTRACT

We describe a general methodology to Design for Producibility and Reliability (DFPAR) for very small volume production runs, In cases where the entire volume for fabrication is less than five products, traditional Statistical Process Control (WC) is inadequate due to reliance on statistics of much larger volumes and the Central Limit Theorem. Data acquisition for process parameter estimation from such a small sample size is difficult; however, it is critical to producing high reliability product,

INTRODUCTION

Small volume fabrication is often as expensive or more expensive than high volume production to achieve acceptable performance levels. Cost factors such as material, assembly time, and safety remain important parameters for small volumes. Manufacture of circuit card assemblies and system units at the Jet Propulsion Laboratory, a NASA Center, is such an example. The need for very high functionality, safety, and reliability drives design and fabrication costs up, while the small total volume and individual component expense leave little latitude for error.

TAGUCHI METHODS

Traditional approaches fail to address the needs of small volume high reliability electronics manufacturing for several reasons:

1, The traditional methods invoke the Central Limit Theorem, implying an assumption of a normal distribution with greater than 30 data points.

2. The traditional methods assume that repair is a reasonable possibility, even after the unit is in the field. There is an extremely high price for NASA to retrieve a satellite when it fails, Medical electronics also cannot depend on going in after the failed component.

3. Traditional methods do not adequately address high reliability requirements which stress safety.

4. Traditional methods do not accommodate the very long expected lifetimes of NASA products.

The DFPAR method is based on the Taguchi Loss Function [1, 2]. The Taguchi loss function involves a different philosophical approach to quality: the further the product features arc from the target value, the greater the defined loss. Traditionally, in the US, when products arc within tolerance specifications, products are passed, then shipped. Genichi Taguchi defines loss as functional variation plus cost caused by the product being defective. The

Taguchi Loss Function is defined as the mean square deviation of specific features of a product from the target values of these features or:

$$L(y) = k(y - m)^2 \qquad (1)$$

where y = specified feat urc characteristic
m = target value
k = proportionality constant,
$k = \frac{\text{cost of a defective product}}{(\text{tolerance})^2} = \frac{A}{A^2}$

As the deviation from the target increases, an increase in loss of performance is seen. This cost maybe a decrease in expected product lifespan or a decrease in the expected Mean Time Between Failures (MTBF). The Taguchi loss function remains valid with very small sample sizes.

The mean square deviation of a specific feature from its target value maybe used to estimate the mean performance loss of Equation (l), where the Mean Square Error (MSE) or mean square deviation from the target value is defined as:

$$MSE = \text{mean value of } (y - m)^2$$

The Taguchi loss function may then be simplified to:

$$L = k(MSE).$$

Economic safety factors: account for the cost implications of variations in the product feature of interest. The economic safet y factor = ø, where

ø = [(mean cost when specific product feature exceeds product functional limits) +
(mean cost when same product feature exceeds design tolerance specification)]'

The numerator is designated to be A. and the denominator to be A. The economic safety factor is then:

$$ø = (A_0/A)^{1/2}$$

If the defective part is reworked during assembly, then A = cost of rework or scrapping the product.

Taguchi advocates putting more time up front, in the design of the product, while also trying to continually improve the assembly process itself. His recommendation is to maximize the signal to noise ratio (S/N) to improve processes. Signal factors are the intended inputs to the process. Noise factors arc uncontrollable error factors. The process is said to be "functionally robust" if the design intent is satisfied for a wide range of part features. Rather than attempting to eliminate or minimize noise factors, the design can be adapted to be less sensitive to these factors.

PWA EXAMPLE

PWA signal factors include voltage, current, component dimensions, solder viscosity at a given time, vapor phase sump temperature, etc. Ranges of the signal factors to test for process improvement may be selected from the chosen design levels. PWA noise factors include dirt, solder voids and bridges, chip movement during reflow, humidity, etc. Noise ranges may be ascertained by observation. An example experiment to determine the most important signal factors for best DFPAR is de-scribed below.

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Signal (Experiment Output or Response)	Influencing Factor
* Solderability	* Tinning
* Solder fillet formation	* Lead forming
* Coplanarity	* Lead forming
* Solder Joint Failure	* Thermal mismatch, assuming board design OK
* Cleanliness	* A = Minimum spacing between devices (15 mil/leaded, 25 mil/leadless)
	* B = Minimum device standoff from board (3 or 10 roils)
	* C = Maximum distance to neutral point
	* D = Minimum lead pitch

Noise
* Chip movement during reflow
* Minor flux residue

ANALYSIS OF EXISTING SMT DATA

The table below summarizes the basic data gleaned from a fcw existing SMT laboratory qualification boards (five total) and a board being assembled now for experiments. The data refers (o individual designs rather than boards. NA = not available. NYA = not yet available. Placement misalignment refers to the number of devices tiled for misalignment after reflow causing the device to be closer to its nearest neighbor than the PWA overall designed minimum spacing between devices. Misalignment is counted for any number of leads overhanging a solder pad.

	Board 1	Boards 2-6
Total Number of Devices	84	99
Of Devices		
Area (in^2)	41,65	54.44
Mean Device Density ($parts/in^2$)	2.02	1.79
Minimum Spacing Between Devices	1.5	1.5
Maximum Distance to Neutral Point	37.5	3
Minimum Lead Pitch	20	20
Placement Misalignment	NYA	10
Misalignment	NYA	10

Process procedures are in control and well documented. At this time, it appears that the DFA policies encourage optimizing the process so that the process will be insensitive to design flaws. While this should be the general policy for continuous process improvement, a more cost-effective approach would be to attempt to optimize the design for DFPAR and for insensitivity to process flaws. We typically have much more control over design than over processes.

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Some process challenges could be significantly reduced or eliminated by encouraging better communication (as part of concurrent engineering) during the PWA design phase. process tolerances arc based on Mil Spec requirements, such as some of those in MS 2000A, which include many non-value-adding requirements and lack some important checks, such as evaluation of thermal mismatches.

DESIGN OF EXPERIMENT (DOE) FOR SMT DFPAR

The example experiment design is a partial factorial design, as described below.

Basic Design: 2^k = n = number of runs, k = number of factors,
2 = number of levels, 2^3=8 runs
+ = high level and - = low level for a factor

Determine whether these factors do indeed influence the signal as hypothesized. Run an Analysis of Variance (ANOVA) first to determine the significance of these factors at their chosen levels. Check ANOVA assumptions for validity in your assembly situation. Major ANOVA assumptions arc:

1, process is in control
2. Population distribution is normal
3. Errors arc homogeneous

Assumption 1 can reasonably be said to be true. Assumption 2 can be said to bc true if the substitution of the t-distribution is made for the normal distribution, to account for the low volume of samples, Assumption 3 is made initially and will be rechecked as ANOVA residual values and the Sum of Squares (SS) are made available.

Ultra low volume production data acquisition was studied to maximize the information 10 bc gained from the data and minimize the total volume required and cost of acquisition. in order of preference these methods are:

1, Examine existing historical data
2. Rc-analyze and possibly partially reprocess rejected product
3. Run and analyze test coupons
4, Run and analyze product produced for these experiments.

Using the cleaning signal as an example with the influencing factors as defined above, an example DOE is:

Run Number	A	B	C	D
1				
2	+			+
3		+	-	+
4	+	+	-	
5			+	+
6	+		i-	
7		+	+	
8	+	+	+	+

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This DOE is a partial factorial design with confounded interactions. It was determined that interactions among influencing factors could be considered negligible or of questionable interpretation. Compute the S/N ratios, η, from the experiment results.

$$\eta = 10 \log(1/r) [(S_\beta - V_e)/V_N]$$

where r = magnitude of input signals,

S_β = sum of squares for each signal factor

V_e = mean square error of nonlinearity where

$V_e = S_e/(2k - 2)$,

2k -2 = number of degrees of freedom

k = proportionality constant defined above

S_e = sum of squares of the error term $= SS_{error} = S_T - S_\beta - S_{N*\beta}$

V_N = error term of nonlinearity and linearity

Having computed the S/N ratios, the next step is to improve the process, First, estimate the proportionality constant between component and PWB parameters. Tune controllable process factors to increase the S/N ratio. Process tuning may involve improving factors such as cleanliness, ESD, component values, solder paste curing time, etc. The next step is to adjust design features to be less sensitive to noise factors and closer to target values, for example, choose a different type of IC (any component) which has a better seal or dissipates heat more successfully. To summarize the five steps:

1, Identify signal and noise factors and their ranges,
2. Using fractional replication in a design of experiment, assign the design signal factors to experiments.
3. Compute S/N ratios from the experiment results.
4. Improve process conditions and estimate the proportionality constant between component and PWB assembl y parameters.
5. Adjust design features to be less sensitive to noise factors and closer to target values.

There is a need for high reliability PWB assembly processes for aerospace, military and medical applications. This approach to improving design for producibility and reliabilit y of circuit and electronic system assembly processes can be utilized as a beginning framework,

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