

PV TECHNOLOGY FOR LOW INTENSITY, LOW TEMPERATURE (LILT) APPLICATIONS

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ABSTRACT

As a result of the recent NASA emphasis on smaller, lower cost space missions, PV is now being considered for a number of missions operating at solar distances of 3 AU or greater. In the past, many of these missions would utilize an RTG (radioisotope thermo-electric generator). Historically, silicon solar cell behavior at these distances has been compromised by a number of mechanisms including shunting, non-ohmic back contacts, and the "broken knee" curve shape. The former two can usually be neglected for modern silicon cells, but the latter has not been eliminated. This problem has been identified with localized diffusion at the top contact/silicon interface which leads to structural changes in the local junction. This is believed to create a resistive metal-semiconductor-like (MSL) interface in parallel with the junction which results in the characteristic forms of the LILT (low intensity, low temperature) "broken knee". This paper discusses a TaSiN contact barrier that will prevent the MSL structure in the junction.

INTRODUCTION

The interest in using photovoltaic solar cells to power spacecraft for interplanetary missions began over three decades ago, fairly soon after the first Earth satellites were successfully launched. Initial choices included the nearby planets of Venus and Mars, although more ambitious efforts were also under evaluation. Early solar cell researchers quickly discovered a number of problems for solar cells operating at 1. LILT conditions.

Obviously, operation at increasing solar distances reduces the available light available to the cell in accordance with the inverse square law ($1/R^2$ - where R is the spacecraft distance to the Sun). As the solar intensity decreases the cell operating temperature decreases. The actual cell temperature is related to the solar incidence, the array absorptivity and emissivity, and thermal interactions with the spacecraft. A typical relationship is shown in Fig. 1 [1], although minor differences may occur for specific situations.

Initial cell LILT degradations included excessive cell shunting (current leakage), rear contact Schottky barrier formation, and the "broken knee" or "flat spot" curve shape degradation characterized by reductions in fill factor,

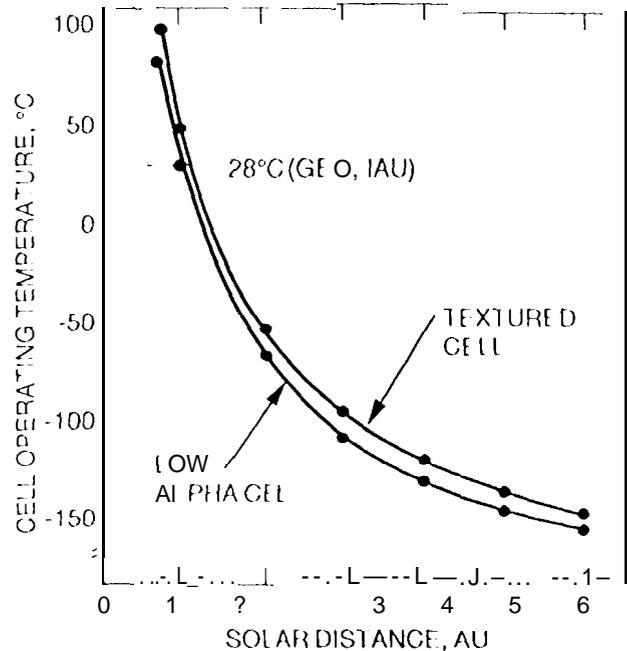


Fig. 1. Solar Cell Operating Temperature vs. Solar Distance

Examples are shown in Fig. 2 [2]. Shunting became a problem related to the low cell output currents. Although not necessarily significant at Air Mass Zero intensities, modest shunt losses could become a very significant fraction of the cell current output at low intensities. This problem was corrected by modifying cell fabrication processes to obtain increased shunt resistances, particularly at the cell edges. The Schottky barrier, which reduced the cell voltage, was corrected by increasing the dopant level in the silicon at the rear surface either by means of lower resistivity silicon or highly doped local regions as in p+ or back surface fields. The remaining degradation, the "broken knee", eluded an easy repair.

Studies reported in 1970 [3] showed a strong correlation between the "broken knee" and the region of the cell at or near the top contact/grid metallization. This was effectively demonstrated by breaking cells into small pieces and identifying the LILT loss phenomenon with the contacted pieces only. However, a workable correction for this problem was not found at this time. This was directly due to

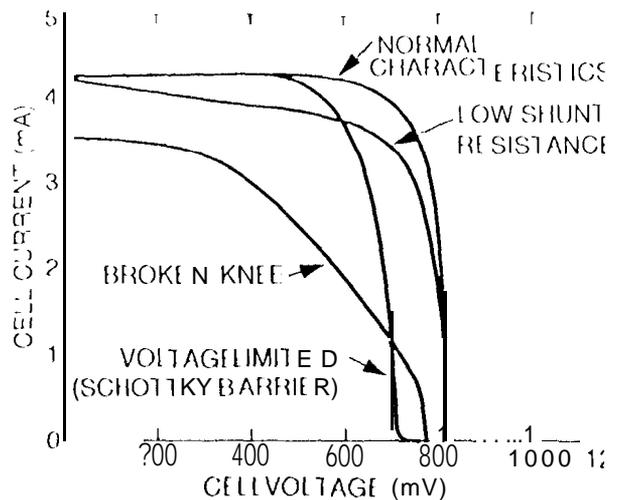


Figure 2. Examples of LILT Degradations

the success of reliable, albeit expensive, RTGs. As a result, little change occurred in cell performance under LILT conditions (outside of improvements due to general advances in solar cell technology) throughout the remainder of the 1960s, 1970s and early 1980s. Fig. 3 summarizes much of the published data on cells under LILT conditions [4]. These data represent both R&D cells and production cell devices utilizing a wide range of cell processing with the exception of front surface texturing. The later was not included since that data was similar to that shown in Fig. 3 but with even greater variations. The range of efficiencies shows increasing variability as LILT conditions become more severe. It is important to note that the individual cell performance at 1 AU, 28°C does not reliably indicate the cell performance at increasing AU distances.

In 1981, a major step was achieved with the identification of a degradation mechanism [5]. The proposed mechanism was the formation of a resistive metal-semiconductor-like (MSL) interface in parallel with the cell junction. The MSL formed as a result of thermally activated dissolution of silicon into the cell front surface metallization allowing the formation of a metal silicide-semiconductor interface. The variable properties of this interface were able to qualitatively describe the variations in the "broken knee" phenomenon. The temperature range where the MSL was observed to form was in the range 450-560°C, a region that was noted as the low temperature range for solid state metallurgical reactions in most metal-silicon systems. The authors attempted to suppress MSL formation by means of a Al_2O_3 overlayer, which would impede the formation of vacancies at the free metal surface and eliminate MSL formation. This approach was not fully effective.

Work was performed at JPL in the 1980s to provide a barrier between the front contact metals and the n-silicon surface using silicon oxide [6]. This was not a true barrier since small holes were required in the oxide to allow for ohmic contact to the silicon since the oxide was a non conductor. This was developed out of the DOE terrestrial high efficiency cell program. Although MSL structures could still form in the

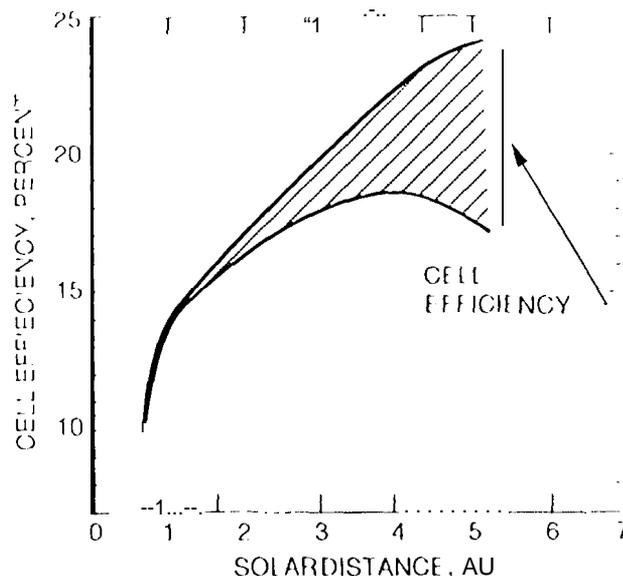


Fig. 3. Silicon Cell Efficiencies as a Function of Solar Distance

region of the oxide holes, the total area available was significantly reduced compared to conventional cells. These results showed a reduction in the occurrence and magnitude of LILT degradation, but the cell process was difficult to reproduce consistently. A new approach to barrier work was initiated in the early 1990s in response to continued interest in the use of non isotope power systems and the development of lightweight array technology [7]. The later would allow PV to compete, for some missions, on a mass basis with RTGs, as far from the sun as 5 AU. This time, a conductive barrier was selected as the focus of the work. An attractive feature of this approach is the possibility of implementing it on conventional cell production lines with a minimum of modifications, minimizing costs and qualification concerns. The barrier layer is of relatively low complexity and does not require any major changes in cell processing. The observed stability after high temperature sintering indicates high stability of the contacts. These factors are felt to enhance the probability for acceptance by the space cell manufacturers for what is presently a small volume item.

BARRIER FORMATION

The diffusion barrier adopted for this study consists of an amorphous metallic ternary alloy, TaSiN (or more accurately, $\text{Ta}_{30}\text{Si}_{14}\text{N}_{50}$). It is obtained by reactive sputtering of a 7.5 cm diameter Ta_5Si_3 target. The deposition pressure was 10 mTorr with a base pressure of 3×10^{-7} Torr. The gas flow consisted of 56 cc/min argon with 30 cc/min nitrogen. In terms of device stability achieved, thin-film barriers of this material - and others similar to it where Ti, Mo, or W is substituted for the Ta - outperform all other diffusion barriers known to date. They do so for both Si and GaAs devices and in combination with either Al, Au, or Cu as the metallization layer.

The unusual effectiveness of these thin-film barriers is partly due to their high crystallization temperature (approaching 1000 °C for hours of annealing) and their inertness to common semiconductors and metals used for device metallization. Their high atomic density ($\sim 8 \times 10^{22}/\text{cm}^3$) and amorphous structure is believed to impart the low atomic diffusivity required for an effective barrier. The combination of three elements of different sizes that can form both metallic and nonmetallic bonds is at the root of their very high metastability.

Evaluation

A number of silicon devices were fabricated using standard space solar cell processing. They utilized a shallow n⁺ phosphorous diffused region on a p-doped substrate. Devices were metallized with an approximately 1000 Angstrom thick TaSiN diffusion barrier contact on the n⁺ surface. This was followed with the standard TiPdAg contact metallization (Fig. 4). Controls were fabricated with a TiPdAg contact only. The entire n⁺ surface was covered by the barrier and metallization (or metallization only for the controls) to provide a greater opportunity for any local MSL formation. For these evaluations only dark I-V characteristics were measured. This was sufficient since the curve shape was the principal feature of interest. The cells were measured at 75K, then annealed in a quartz tube furnace at 600° C for twenty minutes. The minimum temperature required to produce noticeable damage in the controls was later found to be 450° C. The lower temperature was used in evaluating solar cell structures (see following discussion). The annealing environment consisted of 1000 sccm N₂ and 100 sccm H₂.

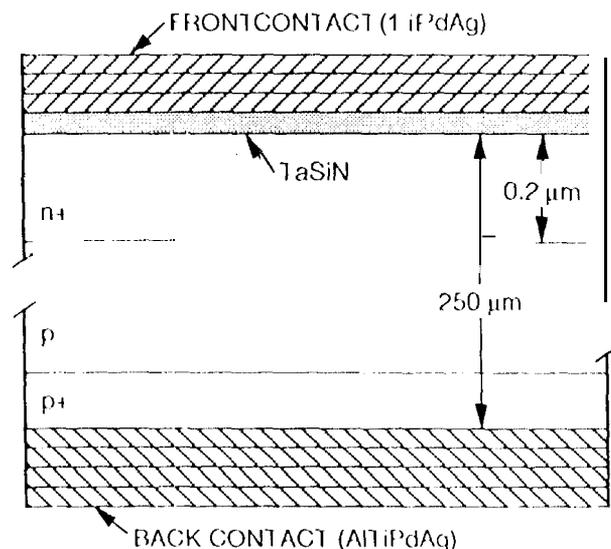


Fig. 4. Cross-section of Solar Cell With Barrier

The control devices showed an appreciable increase in the dark forward current, whereas devices with a diffusion barrier displayed relative stability in their I-V characteristics (Fig. 5 and 6). Some variation in the characteristics of cells with the barriers was observed, but further examination identified these effects with edge leakage of the devices.

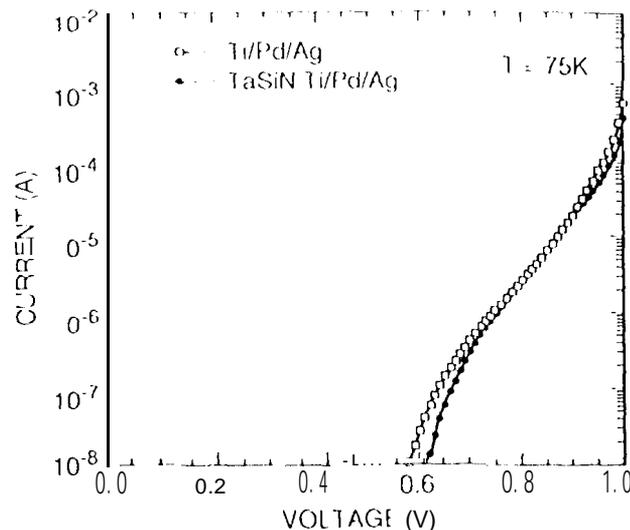


Fig. 5. Test Sample Dark Forward Characteristic - Before Annealing

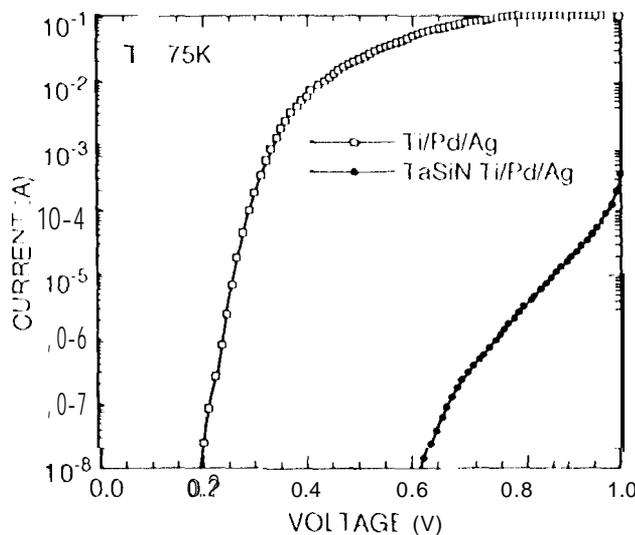


Fig. 6. Test Sample Dark Forward Characteristic - After Annealing

The initial evaluation provided a strong indication that the barrier could effectively eliminate or control the power loss typified by the "broken knee" in solar cells under severe LILT conditions. Consequently, further evaluations were extended to solar cell configurations. The cells were fabricated essentially identical to the above diodes with a top grid contact structure rather than full coverage. Existing cell masking tooling was utilized for the barrier and contacts. Although not optimized for accurate indexing, this was felt to be sufficient for test purposes. The cell I-V characteristics were measured at 5mW/cm² intensity at a temperature of approximately 115 K. As with the diodes above, the test cells were annealed in a quartz furnace at 450° C for ten minutes in a similar ambient. Controls were fabricated without the barrier. The diffusion barrier contact cells were found to show, on the average, an improvement in fill factor, while control cells all degraded noticeably (Fig.

in maximum power compared to an average loss of 7% for the controls. The fill factors of the test samples, after annealing, were on the order of 0.89.

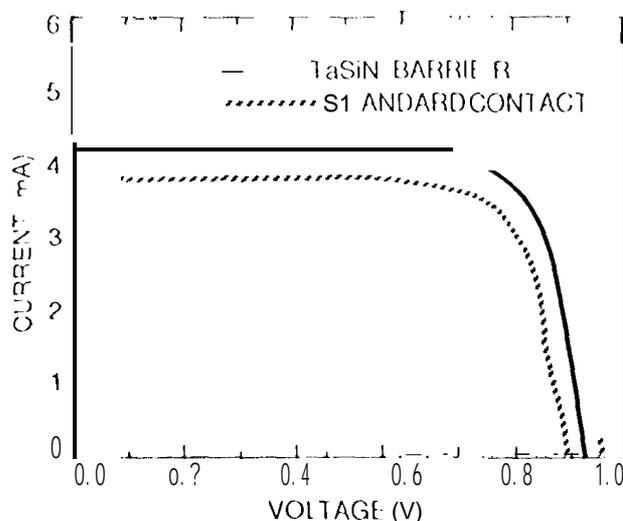


Fig. 7. Solar Cell I-V Characteristic - Before Annealing

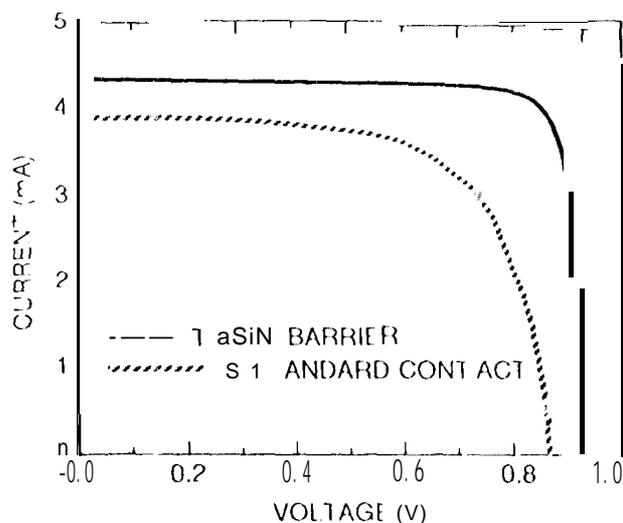


Fig. 8. Solar Cell I-V Characteristic - After Annealing

It was noted that some cells with the diffusion barrier did show a small loss in fill factor. Examination of the contact metallization by SEM (scanning electron microscope) revealed some flawed areas of the grid structure. These flaws appeared to be misalignments between the TaSiN layer and the subsequent contact metallization. In these regions it is believed that the contact metal may have directly contacted the silicon surface. The improvement for the barrier cells after annealing most likely reflects changes in the barrier material leading to improved contact resistance. For these studies little optimization of the barrier layer, in terms of thickness or composition, was undertaken. Parameters developed under other programs were used. In addition, the transfer of cells between CalTech, where the barrier material was deposited, and ASE C, where the

contacts were applied, may have introduced surface contaminants. In a production process all depositions and processing would be performed under controlled conditions leading to substantial improvement in material quality.

CELL IMPACT AT THE ARRAY LEVEL

In order to fully understand the impact of new cell technology, it is necessary to perform analyses at the mission/array level. Experience has shown that the optimum cell for a particular mission can only be determined by a knowledge of the mission requirements, including any power system constraints such as stowage volume or array mass. For this analysis design requirements were selected that were felt to be challenging and also potentially applicable to a variety of future missions. The selected requirements will push the limits of present day cell technology. It was assumed that the PV array system provides 100W to the spacecraft at 5 AU. This approximately equals the position of Jupiter. This would apply not only to a mission to that planet, but also to missions that would employ a Jupiter gravitational assist in order to achieve a higher orbital velocity than could be achieved from a practicable chemical propulsion system. An example of the later might be a comet or main belt asteroid rendezvous. For a small, lightly instrumented mission, the 100W power value can be taken as a modest science and engineering load or as a "keep alive" level for a spacecraft not actively undertaking science measurements.

Conventional array assembly and integration loss factors (UV cover losses, cell packing factor, current mismatch etc.) were included in lieu of any mission particular values. These were used to determine the effective array area conversion efficiency based on the initial cell efficiency under 5 AU operating conditions. In addition, a modest radiation power loss of 10% was assumed for silicon and 5% for GaAs to account for possible flare degradation during the direct Earth-5 AU transit. It should be noted that this does not account for additional radiation degradation that would occur during a Jupiter close approach. Some array design factors were ignored to simplify the analysis. However, the intent here was to determine differences, rather than absolute masses and area values. Initial cell efficiencies at 5 AU were assumed to be 20% for GaAs/Ge and 21% for silicon without LILT degradation and 16/0 for silicon cells with severe LILT degradation. These values correspond to efficiencies that have been measured in the laboratory. The 21% value for cells without LILT degradation is lower by about two or three efficiency points than the best cells reported. However, experience indicates that the typical cell in high volume production will fall short of the best R&D cells. This is particularly true in this situation where the data extends over three decades and comes from many sources. Consequently there is a concern for data accuracy due to less accurate measurement facilities and equipment that were available in the past. For the conventional silicon cells, the 16% efficiency was considered to be the average cell output even though it might correspond to the low range of the power distribution. This is because cell circuit string performance will tend to be dominated by the output power

performance will tend to be dominated by the output power of the lowest cells. This is particularly so where there is a wide variation in individual cell fill factor.

As a result the 100W requirement requires 1.7 m² of GaAs/Ge cells with the assumption of a 0.9 cell packing factor. For silicon a slightly lower cell packing factor of 0.85 was assumed to allow for area lost to bypass diodes and associated wiring. Ongoing studies show that bypass diode protection for cell cracking and/or shadowing is required for silicon although not necessarily for GaAs. For LILT silicon cells the required array area is approximately 11 m² and for conventional silicon cells 15 m². At Earth these arrays would produce 1350W for the LILT cell array, 1950W for conventional silicon, and 2300W for GaAs/Ge.

The mass impact will reflect the array areas and also the specific array technology, such as rigid, flexible, conventional or lightweight. Two basic design ranges were examined here. One is based on low mass technology (70-80 W/kg at Earth) and the second on more conventional technology of 40-50 W/kg. The details of the designs were not considered other than to determine the effective kg/m² for the cell circuit and the structural elements. However, thin cell technology was assumed (65-75 microns for silicon and 85-100 microns for GaAs). For the more conservative conventional array approach the GaAs, LILT silicon and conventional silicon array masses were 47, 40, and 54 kg respectively. For the low mass designs the values fell to 29, 23, and 31 kg. Consequently, silicon has the potential for the smallest and lowest mass array and also the largest and most massive array. These differences might be even greater if the larger array size required additional panels and the associated hinges and deployment mechanisms.

The final aspect of cell impact examined was array cost. Cost is always a difficult parameter since space arrays are built to specifications and requirements which are generally different for each array. This is particularly true for interplanetary spacecraft. The cost of the array is impacted by factors extending well beyond the activities of procurement and assembly. For example, array geometries can be simple rectangles or complex shapes with numerous "keep out" zones. Shadowing can be nonexistent or extensive. Array procurements may include fabrication and test of extensive qualification hardware and required qualification and acceptance tests can vary widely. In spite of the lack of "standard" array costs, estimates were made based on the review of a number of past and present JPL missions. The data was adjusted to project potential array costs for an array system having moderate design complexity and limited qualification and acceptance testing. The overall array procurement was assumed to have a duration of two years from contract initiation to final delivery. Obviously it is understood that actual array costs might be increased or decreased by changing the listed assumptions. However, the cost differentials for the different cell types used is felt to be relatively accurate even if overall costs are of greater uncertainty. A ten percent cost premium (at the array level) was assumed for the LILT silicon cell compared to the conventional silicon cell. This allows for an approximately 50% cell cost premium. In addition, thin cells are assumed for all configurations in line with the previously

mentioned thicknesses in the belief that low mass will be a prime design concern. The substrate costs are not included and although not insignificant, those costs would be similar for all cell choices. It is important to note that since silicon array costs were excluded in order to simplify the analysis, actual flight array costs will most likely be higher. However, the cost differentials between the three options would not be expected to change greatly. Study findings are summarized below in Table 1.

CELL TYPE	ARRAY AREA (m ²)	MASS (kg) Conventional/ Lightweight	COST (\$M)
silicon	16	54/31	2.4
LILT silicon	11.5	40/23	1.8
GaAs/Ge	12	47/29	2.9

Table 1. Cell Cost/Area/Mass Impact

The results for conventional silicon and GaAs/Ge are relatively similar - small mass and cost differences. The latter is somewhat closer if substrate and deployment mechanism costs are included. The GaAs option would be even more attractive due to the more predictable LILT array performance at 5 AU. Selection of conventional silicon solar cells for minimum LILT degradation, even assuming that the cell LILT characteristics don't change after array assembly operations, is probably not viable. The added test costs and reduced cell yields may not provide an array efficiency enhancement large enough to offset the additional costs.

In comparison, the use of LILT silicon cells will provide a wide range of benefits including significant mass and cost reductions. In fact, the cost savings of approximately \$0.6M-1.1 M compared to either conventional silicon or GaAs is on the order of what might be required to establish a production capability for LILT cells. In the past, individual missions have not provided the funds nor the time for developments such as this. Further, in the new era of "faster, better, cheaper" missions, it is unlikely that the situation would change. Possibly an approach similar to that of the Europeans, i.e., a committed government sponsored program, would be required. This could then establish a capability that could be used on many future missions, essentially "paying for itself" after only one or two flights.

CONCLUSIONS

A solar cell contact barrier consisting of TaSiN has been developed and evaluated as a method of preventing the occurrence of the "broken knee" phenomenon under LILT conditions. The barrier was shown to be stable under extended high temperature anneals, performed to reproduce and extend stressing typical of contact sintering, AF coating, and cell interconnection processes. The barrier was shown to significantly reduce the occurrence of "broken knee" effects. Cells were fabricated that regularly exhibited high fill factors (0.89) under LILT conditions corresponding to photovoltaic operation at approximately 5 AU.

An analysis of the impact of cell technology on array performance indicates that the use of silicon cells free from LILT degradations can provide substantial mass and cost advantages when compared to conventional silicon and GaAs/Ge cells. The actual magnitude of the gains can only be determined with knowledge of production cell LILT performance and from a detailed array mission design analysis. In addition, some further improvement might be obtained by specifically tailoring cell design to low intensity operation. Although accurate quantitative knowledge is presently unavailable to answer the previous comments, it would appear that LILT silicon cell performance could reasonably be expected to equal that of GaAs/Ge, at a lower cost.

Although not within the scope of this work, it is notable that the use of the contact barrier also has potential applications for cells that are operated in or exposed to unusually high temperature environments.

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