

Total Ionizing Dose Effects on High Resolution (12-bit) Analog-to-Digital Converters*

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Abstract

This paper reports total dose radiation test results for high resolution 12-bit A/D converters. Small changes in internal components can cause these devices to fail their specifications at relatively low total dose levels. Degradation of signal-to-noise ratio becomes increasingly important for high-accuracy converters. Rebound effects in the thick-oxide MOS devices cause these responses to be different at low and high dose rates, which is a major concern for space applications,

I. Introduction

Numerous advances have been made in the design of analog-to-digital converters to increase speed and accuracy. Operation of these devices depends on many factors, including close matching of internal components in the differential comparator and ladder switch networks that are used in successive-approximation type converters. Changes of only a few millivolts are sufficient to cause high-accuracy converters to exceed specification limits. Evaluating the suitability of these devices for space applications is quite complicated not only because of the close tolerances, but also because the overall function of the converter is complex, introducing many possible failure modes. This is further compounded by the use of BiCMOS technology, which may respond differently to ionizing radiation than conventional devices.

Many applications of analog-to-digital converters (ADCs) require improved speed and accuracy. In high resolution (12-bit or higher) and high speed applications, conventional dc parametric measurements are not always sufficient to characterize the performance of ADCs. It is possible for dynamic parameters of ADCs to exceed specification limits, particularly after radiation degradation, even though the dc parameters are well within the specification limits. Dynamic specifications are important for signal processing applications such as spectrum analysis and high speed data acquisition. Dynamic specifications of ADCs can be measured with a fast-Fourier transform (FFT) method that not only provides information about high-speed operation, but also allows characterization of individual transition code accuracy.

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This paper presents the results of detailed evaluations of high resolution successive approximation ADCs that are being used in various flight projects at the Jet Propulsion Laboratory. These converters utilize BiCMOS technology in order to reduce offset voltage in critical regions of the circuit, and reduce power consumption compared to older bipolar devices. Several 12-bit successive approximation (SA) ADCs were previously tested for static parameters only. [1] Dynamic test methods are compared with more traditional static testing approaches, and noise degradation is shown to be an important factor in high-speed converters. Various failure modes are evaluated, including dose rate effects and rebound,

H. Device Structure and Technology

BiCMOS structures used in successive approximation A/D converters are markedly different from BiCMOS devices used in high-speed logic circuits. Most ADCs require total chip voltages of 15-20 volts in order to accommodate a 10-V signal range; lower voltages place extreme demands on accuracy and resolution because the size of a least-significant bit (LSB) scales with the voltage range. Speed requirements are modest compared to digital technologies. Bipolar devices are generally used in only a few circuit areas where the low offset voltage and high transconductance of bipolar devices provide major advantages, such as the input stage of the comparator. Hence, the usual approach is to design bipolar devices that can be integrated into

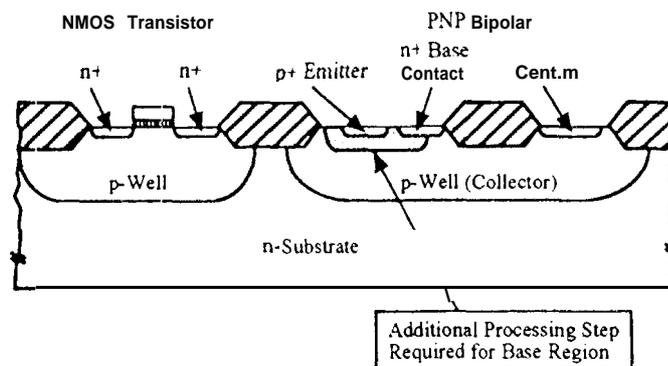


Figure 1. Bipolar Transistor Requiring One Additional Processing Step in a CMOS Process

Table 1. Device Construction of High Resolution ADCS

Device	Resolution	Ref Voltage	LSB (mV)	T _{gate ox} (A)	T _{field ox} (A)
MX674A	12-bit	Internal	2.44	900	11500
MX7672	12-bit	External	2.44	900	11500
AD7872	14-bit (Serial Output)	Internal	0.366	500	10000

a CMOS process with relatively few process steps. Figure 1 shows one approach, which requires a single additional diffusion step. Note that these processes use n-substrates, so that a vertical pnp transistor is produced,

Most of the internal circuits use CMOS. The CMOS devices have much thicker gate oxides than conventional digital CMOS processes because of the high breakdown voltage requirement. Three different A/D converters were evaluated in this work, as shown in Table 1. Two devices have an internal reference voltage which turns out to be an important total dose radiation failure mechanism, In addition the 14-bit converter has a much smaller LSB value (0.366 mV) than either of the 12-bit devices not only because of 2 additional bits but also because of the 6 V full scale input voltage range compared to 10 V for 12-bit converters.

111. Experimental Procedure

A. 12-bit ADCs (MX7672/MX674A)

Test Set-up

Test boards for static measurements were carefully designed and fabricated to reduce noise and interference. To minimize possible noise and hysteresis at the transition voltages of the converter, it is needed to closely follow the layout procedures that are given in the manufacturer's data book. [2] The test set-up consisted of a precision DC source (HP3245A), a DVM (HP3458A), and a dc power supply (HP6624A). A PC was used as a controller to measure static integral nonlinearity (INL) and differential nonlinearity (DNL) of ADCs. Shielded cables were used as interfaces to each test instrument to reduce noise in the test environment. DC parameters were measured with a HP82000M test system,

Static Performance Parameters

Unipolar DC input (0 to 10 V) was selected for both 12-bit ADCs to measure the static performance parameters, INL and DNL. The test algorithm measured the transfer curve at each

code transition. After the two end points of the transfer function are found, the LSB(actual) is calculated from the following equation.

$$LSB_{actual} = (V_{max} - V_{min}) / (2^N - 2)$$

$$V_{max} = \text{voltage at codes between } 2^N \text{ and } 2^N - 1$$

$$V_{min} = \text{voltage at codes between 0 and 1}$$

and $LSB_{ideal} = V_{FS} / (2^N - 1)$

$$\text{where } V_{FS} = V_{ref}$$

In order to find the full scale transfer function of an ADC, offset and gain of the transfer function must be found first. The offset is the voltage that the code transition 0 to 1 deviates from the ideal code at the input at 1/2 LSB. The gain is the difference in the slope of the actual transfer function and the ideal transfer function,

$$\text{Gain} = LSB_{ideal} / LSB_{actual}$$

$$\text{Offset} = \text{Gain} \times V_{min} - LSB_{ideal} / 2$$

Then, corrected voltage V_c can be calculated using

$$V_c = \text{Gain} \times V_{mea} - \text{Offset}$$

$$V_c = \text{actual corrected voltage at a code}$$

$$V_{mea} = \text{actual voltage applied to ADC input}$$

From this end point straight line approximation, DNL and INL for code n can be calculated as follows

$$DNL(n) = [(V_c(n+1) - V_c(n)) / LSB_{actual}] - 1$$

$$INL(n) = [V_c(n) - V_{ideal}(n)] / LSB_{actual}$$

With the equipment and control method used in this paper, it takes only 20 seconds for major transition codes testing and about 2 hours for all codes testing. It is clear that the test time can be reduced tremendously if only major codes testing is per-

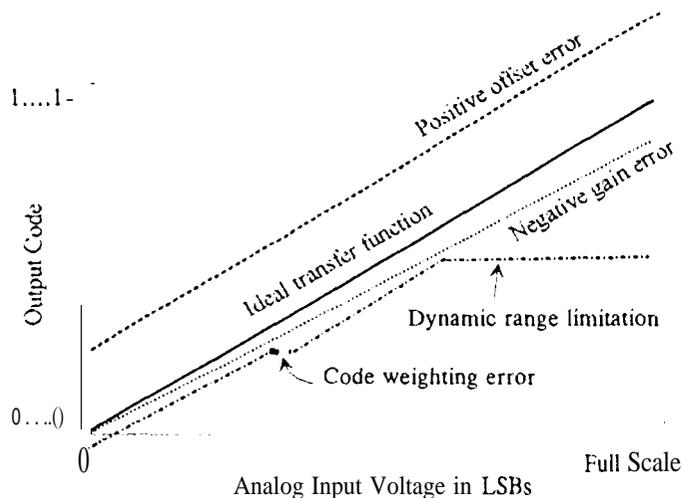


Figure 2. Ideal Unipolar Transfer Function

formed. Major transition codes testing provides most of the key information on the overall transfer curve due to the internal design implementation of the successive approximation type converter.

During test measurement, the propagation of the digital noise in the test setup had to be minimized, outputs of converter were tri-stated during data acquisition with a latch circuit to suppress transients which may result in feed back to the converter input signal. The HP 3245A precision dc source provided 10 V full scale with 10 UV resolution and reduced the wait time for full-scale slewing of the input signal. Other dc parametric testing, such as I_{oz} , I_{dd} , and V_{ol}/V_{oh} , was performed on the HP82000M mixed-signal test system.

Figure 2 shows a typical transfer function of an A/D converter. The figure also illustrates the effects of various failure modes on converter performance. The shape of the transfer curve provides useful insight into internal operation of the converter. Offset error shifts the transfer function curve parallel to itself along the code axis. The transfer curve shift indicated would occur for a positive offset drift, Gain error rotates the transfer curve around the point at which the offset error occurs, changing the slope. However, the slope can also be affected by changes in the internal reference voltage. The transfer curve shift indicated would occur for a negative gain error. For the unipolar A/D converter, gain and offset error are the results of independent error sources, and the combined net effect on the transfer curve as radiation level and internal noise level changes is unpredictable. Code-weighted errors often lead to INL/DNL errors of a converter. Dynamic limitations of a converter show missing codes at higher full scale voltages. At low radiation levels only small changes occur, such as slight changes in slope due to reference voltage changes. However, at high radiation levels, large discontinuities were often observed, corresponding to 10ss of major code transitions.

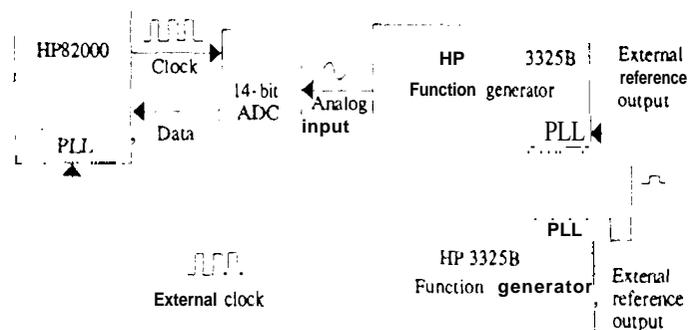


Figure 3. Synchronization of the signal generators

B. Dynamic Characterization of AD7872 14-bit ADC

DUT Board Layout

The difficulty associated with 14-bit ADC characterization was to exercise the converter in the same way that the designer will use this converter in the application. DUT board layout and input signal filtering and conditioning are critical issues to be dealt with as is the reduction in interference associated with combining the analog and digital circuitry in one board.

A custom circuit board was designed to adapt to the HP82000M test system and minimize the influence of the noise from digital circuitry on analog signals. Coaxial and shielded-twisted cables were used to interface the analog input signal. Digital and analog circuits were separated to reduce interference. A single-point analog ground was established close to the device to separate the digital ground pin and the converter analog ground pin. None of the other digital grounds were connected to this analog ground point.

To minimize noise coupling at the input signal, the input signal coaxial cable was directly connected to the input lead of the device pin. A low-pass filter and band-pass filter were designed to insure that the signal provided by the HP3325B function generator was a spectrally pure input sine-wave. Dynamic testing was then performed by capturing the serial digital output of the ADC with the HP82000M test system.

HP82000M Mixed Signal Test System Setup

A complex test setup is needed for realistic simulation of the actual application. Most high-resolution ADCs are used in applications converting a dynamic input signal into a stream of binary codes. Dynamic characterization was performed by generating a sine-wave input and then using digital signal processing (DSP) techniques to analyze the output data. Digital signal acquisition, data analysis, and instrument control were performed using an HP82000M mixed signal test system with visual engineering environment (VE) software.

Table 2. Device Failure Modes

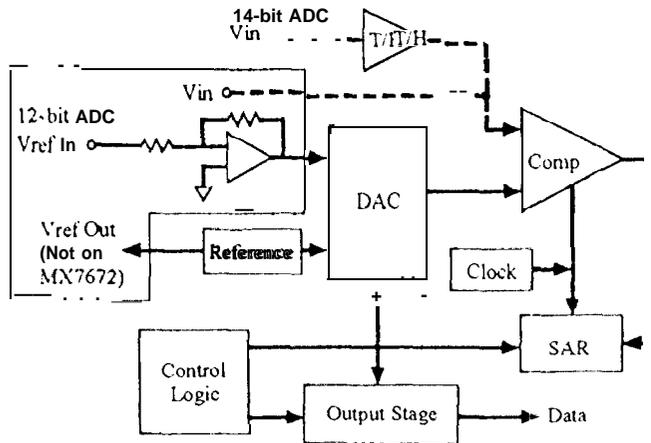


Figure 4. Functional block diagram

Figure 3 shows the synchronization of the input signal frequency and the clock signal for the HP82000M. The signals must be phase locked to ensure that sampling stays coherent, [3] One HP3325B synthesized function generator was used as a clock signal generator and its output was fed into the external clock input of the HP82000M. The output of the other function generator was fed into the ADC input.

Dynamic Performance Parameters (SNR/THD)

A 9.706 kHz sine wave was fed into the input of the ADC. The clock frequency was 1.826 MHz. The ADC output codes were used to calculate the signal-to-noise ratio (SNR), the magnitude of the fundamental frequency divided by the root-sum-squared of all the other frequencies, using the FFT to give a display similar to a spectrum analyzer. The ADC output waveform was reconstructed from the input sine wave and the FFT method was used to calculate the noise properties of the ADC in the frequency domain and compute the SNR.

IV. Analysis

High-resolution A/D converters consist of a DAC, a high speed comparator and successive approximation register (SAR), a track/hold amplifier, a buried Zener voltage reference, a clock oscillator and control logic. Figure 4 shows the functional block diagram of a typical high resolution A/D converter. The specific implementation varied slightly for different devices.

The 12-bit converters, MX674A and MX7672, do not have the internal track and hold amplifier. Thus, an external sample and hold circuit must be used for dynamic parameters (SNR/THD). Then the SNR measurement would apply to the whole system, including the external S/H amplifier and ADC. This would not be a real representation of the converter and the test results would not be a valid measurement. Therefore, dynamic parametric testing was not performed for the 12-bit ADCs.

Mechanism	Bipolar	CMOS	Net Effect
Vref	x		Gain, offset error
Comparator	x	y	INL/DNL
Internal Amp	x	x	Gain, offset, dynamic error
SAR		x	INL, dynamic error
Control logic		x	Functional failure
DAC		x	INL, dynamic error
Output stage		x	DC parametric, functional failure

The MX674A has an internal 10 V buried zener voltage reference for low noise and low temperature drift. This is the required reference voltage for the converter. The reference output voltage is fed into the reference input which is directly connected to an input of an amplifier whose output goes to the 12-bit DAC. Even though the reference voltage is designed for low noise, noise from the op-amp which is directly connected to the DAC will introduce gain and offset error in the converter, and eventually it will induce linearity errors. The other 12-bit converter (MX7672) does not have the internal reference voltage and it requires an external reference voltage for operation.

The linearity of the SA converter is determined primarily by the performance of the internal D/A converter. [4] Thus, transition voltages above and below codes of the interest must be measured because transition voltages can be shifted due to dynamic errors of the conversion process in addition to shifts caused by linearity errors of the internal DAC. The settling time of the internal DAC and the comparator affect the conversion time.

Although initial degradation in high-precision converters are usually caused by mismatches in analog circuits, parametric degradation and functional failure can also occur due to threshold-related changes in the digital output and control stages. Device failure modes and processing information on each subcircuit are listed in Table 2.

The 14-bit ADC, AD7872, has a serial output to improve the data acquisition and processing time. The internal S/H amplifier keeps the input signal stable to the desired accuracy while each bit is evaluated. The linearity of the S/H amplifier is important to the overall converter circuit.

As mentioned earlier, vertical PNP bipolar transistors are used in the input stage of the internal S/H amplifier to provide high input impedance. Bipolar transistors are also used in the input stages of the internal comparator to match the impedance of the circuitry where the voltage controlled mode DAC requires constant impedance.

Most manufacturers do not provide information on correlations between dynamic parameters and static DC parameters. However, the INI, is directly related to the total harmonic distortion (THD) for a SA converter. [5] INL is unlikely to

exhibit abrupt changes in the transfer function except at major transitions. Changes at major transition codes are followed by subsequent codes with same INL error ranges. This makes testing at the major transition codes possible without losing general INL information for all codes. In general, for 14-bit ADCs, if the SNR is above 80 dB and the THD is much greater than 80 dB the INL performance will be better than +/- 0.5 LSB. SNR degradation of about -6 dB will reduce INL performance by 1 bit, [6] The ideal SNR for an n-bit ADC can be calculated as following equation

$$\text{SNR} = 6.02N - 1.76 \text{ (dB)} \quad [7]$$

and the power spectrum is used to calculate the SNR.

$$\text{SNR} = 20 \log \left[\frac{\text{RMS Sum Signal}}{\text{Total RMS Sum Noise}} \right] \text{ (dB)}$$

The distortion of the spectrally pure input sine wave must be less than -90 dB. The sine wave was generated with cascading low pass and band pass filters to the HP3325A function generator to achieve the lowest noise floor level and fed into the input of the ADC.

The histogram test method is widely used to calculate INL/DNL of high resolution (12-bit and up) converters. However, a study showed that the output code histogram test of a 13-bit ADC showed large linearity errors due to increasing noise. [8] Therefore, differential linearity estimated by histogram test does not provide objective information on the performance of high resolution converters. In addition, due to the limitation of the memory size of the HP82000M test system, the histogram test was not possible to perform for the serial output 14-bit A/D converter. The input dynamic range is only 6 V for 14-bit which provides an LSB of 366 uV. That is sufficient to cause linearity errors with a very small fluctuations in test system noise level.

V. Total Ionizing Dose (TID) Test

All devices were irradiated and tested at room temperature. Radiation bias fixtures were designed and fabricated to operate devices during total dose irradiation. Due to the extremely fast annealing behavior of the devices, the ADCs were tested with various dose rates. Pre/post electrical parametric and functional tests were performed using the bench-top setup and the HP82000M test system with a specially designed DUT board to fit in to HP82000M interface board.

Since the results of previous total dose test showed that the static bias condition was the worst case, [1] both 12-bit ADCs were biased only static mode during irradiation. However, two different bias conditions for 14-bit ADC were used during irradiation: (1) static, which initialized the device to one state, but did not allow it to perform active conversions during the irradiation; and (2) dynamic, clocking the devices at 1.826 MHz and performing conversions at a frequency of 83 kHz.

VI. Results

4. 12-bit ADCs (MX674A/MX7672)

The dominant failure mode at high dose rate (100 rad(Si)/sec) was increase in the tri-state leakage current (I_{oz}) for both converters. I_{oz} exceeded its specification limit of 10 uA at about 6-8 krad(Si). Functional failures were observed at 20 krad(Si). Although large changes observed for the I_{oz} parameter, only slight changes occurred in other dc parameters until the devices were irradiated to much higher total dose levels. The power supply current remained relatively low even at the functional failure level of 20 krad(Si).

The MX674A was tested at 0.015 rad(Si)/sec. INL/DNL exceeded the specification limits at 10 krad(Si). The tri-state leakage current, I_{oz} , exceeded the limits at 19 krad(Si). The degraded transfer functions of the converter at 21 krad(Si) and 30 krad(Si) are compared to the ideal transfer function, shown in Figure 5.

After irradiation to 21 krad(Si), significant changes occurred in gain, as shown by the change in slope in Figure 5. These changes are approximately 4%, which is about two orders of magnitude greater than the initial specification. There are also some code weighting errors.

When devices were irradiated to 30 krad(Si), large deviations in the transfer curve were observed that correspond to missing codes. The example in Figure 5 shows a case where higher order codes are missing. Missing codes are partial functional failures, and are clearly more serious in applications than parametric failure. The net transfer curve is a combination of several failure modes, as shown in Figure 2.

The reference voltage degraded significantly during total dose irradiation and showed even more significant degradation after annealing. Figure 6 shows the reference voltage normal-

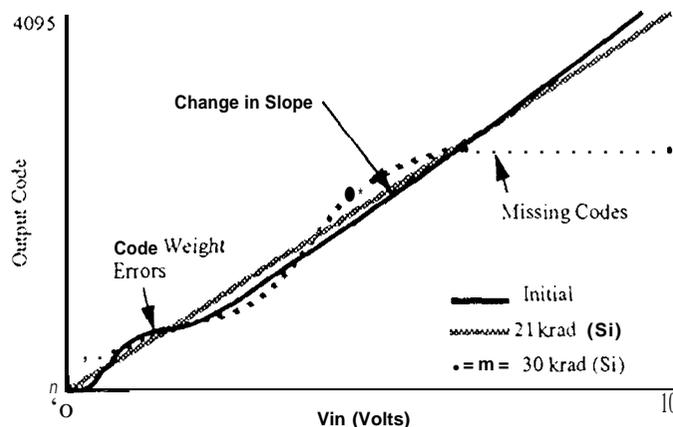


Figure 5. MX674A Transfer Curve After Irradiation

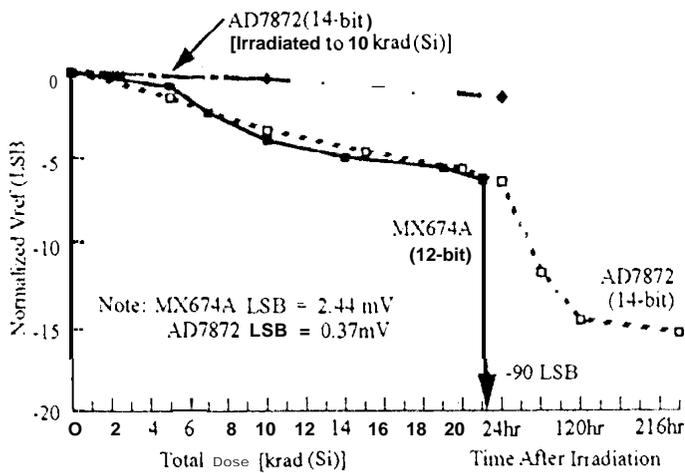


Figure 6. Reference Voltage Degradation

ized to a LSB of 2.44 mV to indicate linearity degradation. The normalized reference voltage after 240 hours of annealing time was about -93 LSBs which was cut out in the bottom of the scale in Figure 6. This rebound effect will lower the failure level of low dose rate test results.

The MX7672 was tested at the low dose rate of 0.005 rad(Si)/sec. INL and DNL stat-ted to exceed the specification limit at 11 krad(Si). DC parameters showed some degradation at that level of total dose, but all were within specification limits. The Vol parameter exceeded the specification limit at 12 krad(Si) and the Ioz parameter of all devices failed at 13 krad(Si). Total dose irradiation was stopped at 15 krad(Si), and an annealing test was started to investigate rebound effects.

B. 14-bit ADC (A [7872])

Initial tests were done with a dynamic bias condition and characterized for only static performance and dc parameters. These tests were done at 10 rad(Si)/sec. The output low voltage, Vol, stuck at high state and exceeded the specification limit at 4 krad(Si). INL and DNL also exceeded the specification limits at 6 krad(Si). No time dependent effects (TDE) testing was performed at that time.

Additional dynamically biased testing at 10 rad(Si)/sec was performed on devices with a newer lot date code (LDC 9402) to verify the initial test results. The first functional failure was observed at 6 krad(Si). Devices failed functionally, and the Vol parameter along with the conversion time failed. The devices could not make any conversions because the serial data output was stuck at high. A few minutes after the end of the irradiation, the failed devices recovered and were fully fictional. The ADCs that irradiated to 8 krad(Si) recovered within about 1 hour and those that irradiated to 10 krad(Si) recovered fully with in about 2 hours of room temperature annealing. The devices were further tested for time dependent effects (TDE) for 72 hours at 25 °C and 24 hours at 100 °C. All devices were still functional and no rebound behavior was observed.

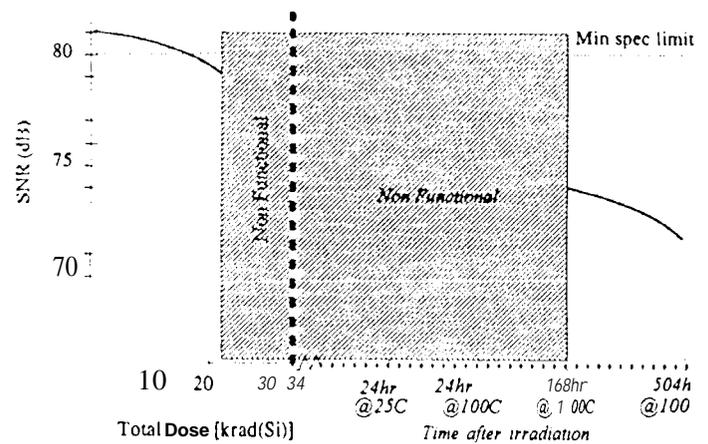


Figure 7. Low Dose Rate (0.025 rad(Si)/see) Test Result on AD7872

Because of the fast annealing characteristics of these A/D converters, they may satisfy a JPL project requirement of 38 krad(Si) if a very low dose rate test is performed, Therefore, additional tests were done with a dose rate of 0.75 rad(Si)/see, Parametric failures were observed at 25 krad(Si). SNR degraded only slightly, by \approx -3 dB. The devices were non-functional at 30 krad(Si).

The ADCs were further irradiated to the final level of 40 krad(Si), and they were still non-functional after 5 hrs of room temperature TDE test. Then, after a high temperature annealing test. 100OC for 24 hrs, all of the failed devices became functional again, However, large changes -approximately 8 dB- occurred in the SNR parameter after annealing. This is such a large change that even though the converter Will still function under DC conditions, it is effectively only a 10-11 bit converter under dynamic conditions.

Finally, a low dose rate. 0.025 rad(Si)/see, total dose test was performed further to study the low dose rate behavior and annealing effects of the devices. SNR degraded to 79 dB from initial value of 81 dB at 20 krad(Si). Devices functionally failed between 22-26 krad(Si). Because of the functional failure of the ADCs, no SNR could be measured for failed devices after total dose irradiations. SNR could only be measured when devices recovered during the annealing pried. Measurements of SNR are shown in Figure 7. Devices were non functional throughout 168 hour high temperature (100 °C) TDE testing. The SNR was further degraded to 74 dB, and the SNR was about 72 dB after 504 hours of high temperature annealing time.

The reference voltage degraded much like the 12-bit MX674A during TDE test, The normalized reference voltage is plotted in Figure 6. Note the large changes that occurred after annealing. This is a serious problem in using these devices in a low dose rate environment. All other dc parameters showed insignificant degradations after irradiation to 20 krad(Si) at low dose rate.

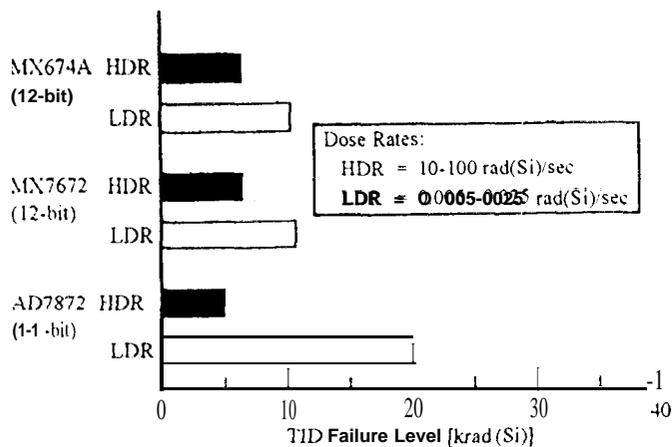


Figure 8. Parametric Failure Levels of BiCMOS ADCs

Two unbiased devices were also irradiated at low dose rate. Although the devices were still functional, SNR degraded to 68 dB at 30 krad(Si). The reference voltage showed only small degradation at that level of total dose. This indicates that the reference voltage degradation is strongly affected by bias conditions during irradiation. However, it degraded slightly after 24 hour of annealing time at room temperature. This degradation confirms the results of biased devices during TDE testing. SNR still remained at 68 dB after 24 hrs of annealing.

Figure 8 summarizes test results for the three converters after tests at low and high dose rates (parametric failure occurred at the right edge of bars in the figure). For all of the converters, parametric failure levels were substantially higher at low dose rates. Note, however, that these failures correspond to very small changes in converter characteristics that cause parametrics to exceed specifications that can only be detected with highly accurate measurements. A similar situation occurred for functional failure levels, functional failure occurred at significantly higher levels when devices were tested at low dose rates than at high dose rates,

VII. Discussion

The most sensitive parameters for the 12-bit ADCs were transfer curve nonlinearities, reference voltage, and tri-state leakage current. The converters functionally failed at lower dose level with the low dose rate testing due to rebound. The functional failure level was about three times higher than the parametric failure dose level.

The tri-state leakage current degradation for 12-bit ADCs from low dose rate test results showed very small improvement compared to the high dose rate test results. For MX7672, radiation test results at dose rate at 0.1-100 rad(Si)/sec indicated that at the lower dose rate of 0.005 rad(Si)/sec the tri-state leakage current failure level was expected to be at least 30 krad(Si) as shown in Figure 9. However, the 0.005 rad(Si)/sec

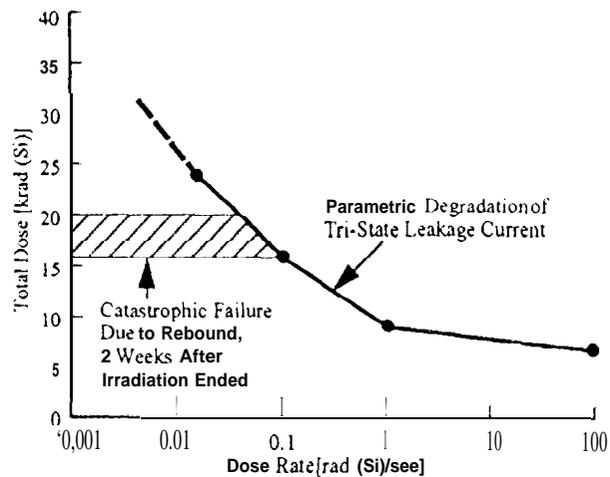


Figure 9. Catastrophic Rebound Failure in MX7672

low dose rate test result shows that 10z parameter exceeded the specification at 13 krad(Si). This is due to the lot-to-lot variation of the commercially processed BiCMOS devices.

It is clearly seen that after total dose irradiation the internal reference voltage degraded significantly for both 12- and 14-bit converters. Even a device irradiated to only 10 krad(Si) and annealed about 24 hrs shows a slight degradation. This will cause the linearity errors to exceed the specification after the annealing period. This can be a serious problem in determining the actual radiation failure levels for these devices. The reference voltage degradation during TDE test demonstrates the importance of annealing and rebound effects in space applications.

For the 14-bit ADC, signal-to-noise ratio and reference voltage were sensitive parameters due to total dose irradiation. Functional failure dominated at high dose rate testing, but the

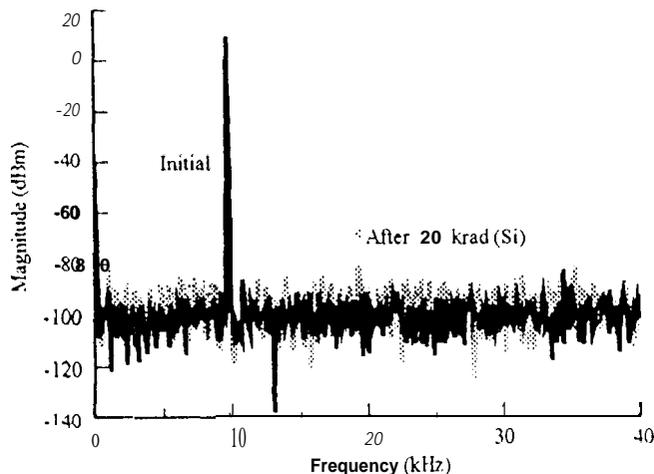


Figure 10. Magnitude Spectrum AD7872 14-bit ADC

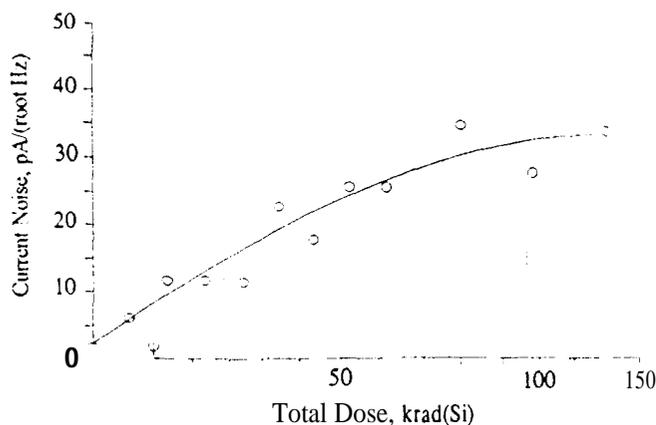


Figure 11. Current noise in the MX414 op-amp

functional failure level was much higher with low dose rate testing.

The internal track-and-hold amplifier on the analog input of the AD7872 allows the converter to accurately convert an input sine wave of 6 V peak-to-peak amplitude to 14-bit accuracy. The amplifier output is then fed into a CMOS comparator. Noise in this critical path along with internal reference noise will add significant distortions to the input sine wave and will eventually degrade the dynamic performance of the converter. The harmonic distortion of the converter increased substantially as the total dose radiation level increases. The 2nd harmonic distortion and the increased noise level of the converter at 20 krad(Si) is compared with an initial magnitude spectrum in Figure 10, SNR decreases significantly as the noise level and the number of harmonics increases. Some non-functional converter showed SNR of below -20 dB.

In terms of noise degradation in the 14-bit ADC converter, we have observed similar noise results for a low-noise operational amplifier after total dose irradiation. The voltage noise of this device was essentially unchanged by radiation, but the current noise degraded severely. The op-amp input stages are likely to be similar to the internal ADC. Data of op-amp is shown in Figure 11. Note that the noise increases more than one order of magnitude at 100 krad(Si). This is compatible with the degradation observed in SNR for the 14-bit A/D converter. The digital switching noise from the DAC and noise associated during sample and hold mode of the T/H amplifier are added to input current noise along with the threshold voltage shift of the comparator.

VIII. Conclusions

This paper has shown how various internal failure mechanisms contribute to the ionizing radiation response of A/D converters. Measurements of the transfer curve can be used to interpret failure mechanisms in complex devices, but require accurate measurements.

Significant parametric degradations were observed in the internal reference voltage, transfer curve linearity, and signal-to-noise ratio. The functional failure modes are caused by missing codes at higher code transitions and non-functional internal logic circuitry.

The classical static dc tests can reveal INL and DNL of some ADCs (12-bits). However, a more sophisticated test setup is required for the dynamic characterization of high speed and high resolution ADCs (14-bit or higher). The test results showed the sensitivity of the noise associated with the dynamic characteristics of the 14-bit converter.

The dominant failure modes in these BiCMOS devices were MOS components due to thick gate oxides. However, rebound effects cause their responses to be markedly different at low and high dose rates. This severely complicates application of these devices in space environments.

Acknowledgments

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