SMT SOLDER JOINT RELIABILITY/WORKMANSHIP ENVIRONMENTAL TEST RESULTS CORRELATION FOR LCC ASSEMBLIES

by

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ABSTRACT

Spacecraft electronics as used in the NASA community, including the Jet Propulsion Laboratory (JPL), demand production of highly reliable assemblies in an Ultra-Low Volume (ULV) environment. At JPL, different aspects of Surface Mount Technology (SMT) including design, manufacturing, test, and deployment (aging) cycles are being investigated. Extensive work has been done in these areas. Two hundred twenty five SMT assemblies with more than 10,000 solder joints have been tested to failure. By the end of our tests, over 50,000 solder joints will have been tested on a variety of Surface Mount Device (SMD) types.

One aspect is focused on identification of the critical manufacturing parameters, the effect of manufacturing defects on solder joint reliability, and integration of Quality Assurance (QA) procedures into the design and manufacturing so that the critical parameters could be bounded and controlled. In this paper, we present correlation between SMT solder joint manufacturing defects and damage propagation during thermal cycling, and the life of solder joints for Leadless Chip Carrier (LCC) assemblies that were tested to failure. Solder joint "defects" were logged prior to cycling and these sites were monitored throughout the tests. The daisy chained assemblies were monitored for electrical continuity throughout the tests to detect "opens" using slight changes in resistance as an idicator. Assemblies were periodically inspected visually at 20-50X magnifications and also at higher magnification using a scanning electron microscope (SEM) to validate visual results.

INTROD(JCTION

OBJECTIVES

NASA Headquarters has established an Electronic Packaging and Assembly Program to address the common needs of NASA programs. One of these programs is focused on the use of SMT for high reliability, ULV spacecraft electronics as used in the NASA community. Four RTOPS (Research & Technology Objectives & Plans) have been conducted at NASA's Jet Propulsion Laboratory each dealing with an aspect of SMT. These RTOPs are interdependent and are being conducted concurrently. Each RTOP concentrates its efforts on a particular aspect of the design, manufacturing, test, and deployment (aging) cycle. The primary objectives of the RTOPS are as follows:

- Identify the critical parameters of SMT manufacture. Determine the methods and tools required to integrate QA procedures into the design and manufacturing processes so that the critical parameters can be bounded and controlled

- Develop a thorough understanding of the creep-fatigue mechanisms underlying solder joint failures of surface mount electronic packaging systems. Develop generic, broadly applicable design guidelines, analysis methodologies, and data requirements.

- Develop an assembly level qualification test methodology for surface mount technology and apply this methodology to electronic packaging systems through the use of experimental design techniques and phased experimentation.

- Deliver the NASA Guidelines for SMT, developed from the knowledge gained from the JPL RTOPS, as well as the efforts of other NASA centers, industry knowledge centers, and industry partners.

References 1-6 document some of activities in these areas. In conjunction with the RTOPS, a survey and a series of Phase 1 and Phase 2 cooperative test programs involving all RTOPS are being performed, Results of the survey and Phase 1 test program for LCC assemblies with emphasis on the Quality Assurance efforts are presented

SMT SURVEY.

NASA centers involved with SMT were surveyed in 1993 (Reference 1). Representatives of aerospace and commercial organizations were included in order to

identify the status of SMT in industry and the specific issues that NASA centers and their industry partners were encountering in the process of incorporating SMT designs into their projects. One section of the survey addresses QA issues for SMT hardware. The questions asked centered on techniques, equipment and procedures used by these organizations to define their SMT QA methodologies.

The objectives of the SMT QA survey were to identify the critical parameters of the SMT manufacture and to determine the methods and tools presently used by industry to identify and control them. Some of the findings from the responses of nine organizations are as follows:

- Majority do not perform solderability testing and hand solder their fine pitch devices and half perform lead coplanarity inspection following lead forming
- The primary method of solder reflow is Ill, followed by hand soldering
- The assembly defects most reported were insufficient solder, no solder and poor wetting
- All use manual inspection for their hardware, 80% feel that dewetting is the single most important feature that inspector should flag
- All perform solder paste qualification tests at their facilities
- 80'% inspect following paste print, part placement and after solder reflow
- 70% use manufacturing analysis tools such as DOE, QFD and SPC/SQC
- 90% track solder defects, defect type and location, but only 25% have a formal method of tying these back to the manufacturing cycles

It was concluded that the leading causes of SMT rejects were solderability and solder paste deposition problems. Some operations did not have corrective action feedback loops to change a design or process even when data indicated a problem. The majority of these issues were addressed in the phases of the RTOPs' activities. Next, Phase 1 activities will be reviewed and results for LCCs will be presented in detail.

PHASE 1 TEST PROGRAM

The Phase 1 test involves use ofa single ceramic component, 0.050" pitch, soldered to an epoxy-fiberglass FR-4 board. LCCs, J-lead cerquads, and gull wing cerquads were the SMT components. The JPL SMT Training Facility assembled 20 and the Electronics Manufacturing Productivity Facility (EMPF) in Indianapolis, Indiana assembled 205 test boards.

Thermomechanical cycle testing (-55°C to 100"C, 45 minutes dwells and duration of 246 minutes) on Phase 1 assemblies having LCCS, began in August, 1993. All LCC assemblies have failed (open circuit). Phase 1 testing of the J-leads was initiated in January, 1994, and now has

reached more than 2,000 cycles with no failure. Testing of the gull wing cerquads started in July, and they have now (November 1995) accumulated more than 1,800 cycles with one failure at 1,720 cycles.

All Phase 1 assemblies were inspected prior to thermal cycling, and have been, or will be, periodically inspected as they are cycled to electrical (solder joint) failure. Correlation between manufacturing defects, dimensional characteristics, inspection observations and life of the solder joint have been analyzed for the failed LCCs and is presented (Figure 8 and 9).

Since JPL and organizations surveyed are using visual inspection for acceptance/rejection of solder joints, we also used this technique. To selectively validate observations we utilized other more powerful visual aids including SEM and cross-sectional microscopic evaluation, Crack initiation and propagation over time were documented using visual inspection and/or SEM. Inspection results will enable the creation of chronological crack maps, which will assist in the characterization of the severity of stress and the estimation of remaining solder life for various assembly configurations, lead materials and printed wiring board systems,

Observation of phenomena such as solder ball spreading, the appearance of "crack healing", and significant surface roughening emphasizes the importance of observing solder microstructural change and could be used to estimate the environmental exposure and remaining life of the solder joints. These changes also depend on the initial properties of solder including solder composition, solidification rate, and interface joint metallurgy. Information obtained from these activities is being incorporated into prediction guidelines for design and reliability and training materials for inspection and manufacturing personnel.

We are also monitoring cycling damage levels and the effect of manufacturing defects (i.e. insufficient or grainy solder, etc.) on damage growth. For example, we are closely monitoring crack initiation and propagation in the heel fillet of gull wing leads which are considered to be key factors in solder joint failure mechanisms. One solder joint showed signs of heel fillet cracking at 50 cycles, but did not continue propagating significantly up to 1,000 thermal cycles. However, this was not the case for the 68-pin LCC solder joint, discussed later.

Thermal cycling test has also yielded large quantities of inspection data, Two methods were developed for ease of inspection data visualization and trends identification. In the first method, inspection data were displayed in an innovative graph representation that allows instant visualization of damage progress levels and correlation to pin locations,

In the second method, the damage that progressed over time was plotted for a group of leads that had the same category of manufacturing defect

Analysis of damage growth enables the identification of the criticality of each defect type, and can lead to guidelines for the acceptance/rejection of manufacturing defects based on type and location. Qualification cycling test results interpretation could provide an indication of the level of damage and could be used to identify the solder joints with reliability problems. Additionally, these methods could be adapted for use with other types of data and other graphical display methods for ease of data visualization and trend recognition.

EXPERIMENTAL PROCEDURES

TEST VEHICLE ASSEMBLY

A general purpose printed wiring board (PWB) with foot print for three termination styles including LCCS with 0.050 inch pitch was used. Each PWB is 3.0 by 2.5 inches and is suitable for both microscopic and SEM examination. Figure 1 shows the layout of a representative test vehicle with a 68-pin LCC part and land patterns for 20- and 28- pin parts. The majority of components were daisy chained with the intention of using an Anatech® for continuous electrical continuity monitoring during thermal cycling to failure.

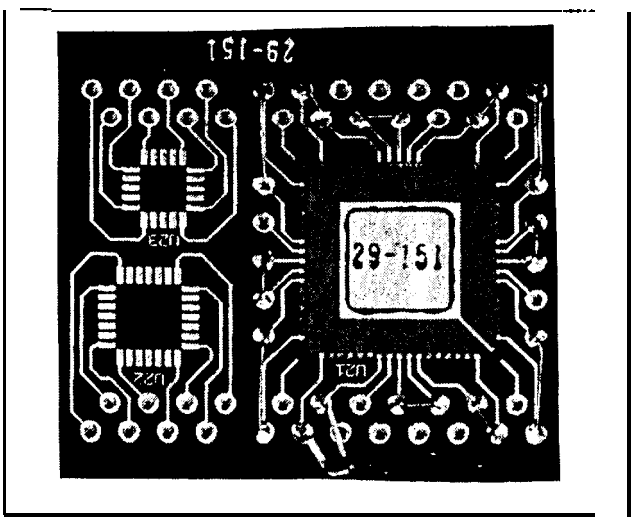


FIGURE 1. Phase 1 Test Vehicle

Two facilities were used for assemblies, the EMPF at Indianapolis and the JPL SMT Training Facility in Pasadena. A total of 84 LCC test vehicles were fabricated. The solder paste type used by the two facilities was 63/37 tin-lead solder paste meeting US Federal Specification QQ-S-571E. This particular composition was used because its wide range of applications and its mechanical properties are quite well understood. An IfraRed (IR) machine was used for solder reflow at EMPF whereas vapor phase (VP) reflow was used at JPL.

MANUFACTURING INSPECTION

All components and boards were visually inspected for quality condition prior to assembly. Solderability testing was performed on sample of the boards. Results were documented. Solder paste volume was also measured using laser scanning equipment. Assembled boards were inspected for solder volume and internal defects using X-ray laminography. Castelation dimensions and solder fillet/configurations were recorded. A list of solder defect codes were used during Phase 1 testing to document inspection observations and for database entry for analyses.

THERMAL CYCLING PROFILE

For cost effectiveness and engineering efficiency considerations, it is desirable to have the shortest possible test period. However, adequate high temperature dwells are necessary for solder creep and relaxation occurrence. On the other hand, excessive high temperature dwell may cause excessive aging resulting in brittle fracture. The ramping rates of heating and cooling are usually limited by the capacity of environmental test chamber, but a high ramping rate could change the state of stress and not be representative of the applications. At JPL, temperature cycle profile from -25°C to 10O°C with three hour duration was used for testing Galileo and Magellan spacecraft electronics. Because of the time lag between assemblies and oven program setting, especially at low temperature, the low temperature dwell was extremely short.

To assure sufficient dwells, it was decided to use the standard NASA thermal cycle. This cycle start at 25°C with a decrease rate of 2°C per minute to -55°C with an oven dwell setting of 45 minutes, The temperature increase to 10O°C at a rate of change of 2°C per minute with an oven dwell setting of 45 minutes, followed by a decrease of temperature to -25°C completes the cycling. The duration of one cycle is 246 minutes. Figure 2 shows the thermal cycle oven program setting and assembly profiles.

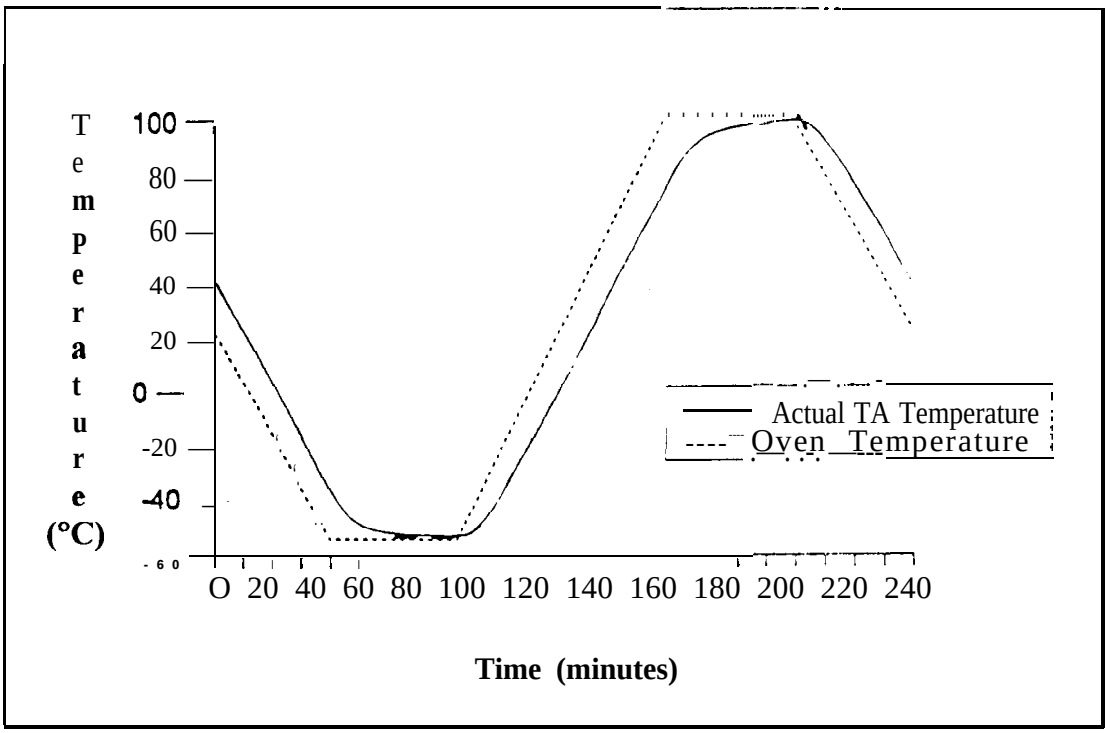


FIGURE 2. Thermal Cycling Profile for Environmental Testing

INSPECTION TECHNIQUES

Assemblies were inspected periodically during thermal cycling as they were cycled to solder joint failure. Three damage detection methods were employed: (1) open circuit detection using an Anatech®, (2) visual observation, and (3) SEM. The criterion for an open solder joint is stated in IPC-SM-785, Sect. 6,0, which reads: 'Solder joint open circuit is defined as the first interruption of electrical continuity that is confirmed by 9 additional interruptions within an additional 10°/0 of the cyclic life". Continuous monitoring of the daisy-chain continuity channel with continuity interruption of 1 microsecond (μsec) and an electrical discontinuity by a channel resistance of 200 ohms (Ωs) were used for the failure definition,

MANUFACTURING INSPECTION RESULTS

CASTELLATION/ SOLDER FILLET DIMENSIONS

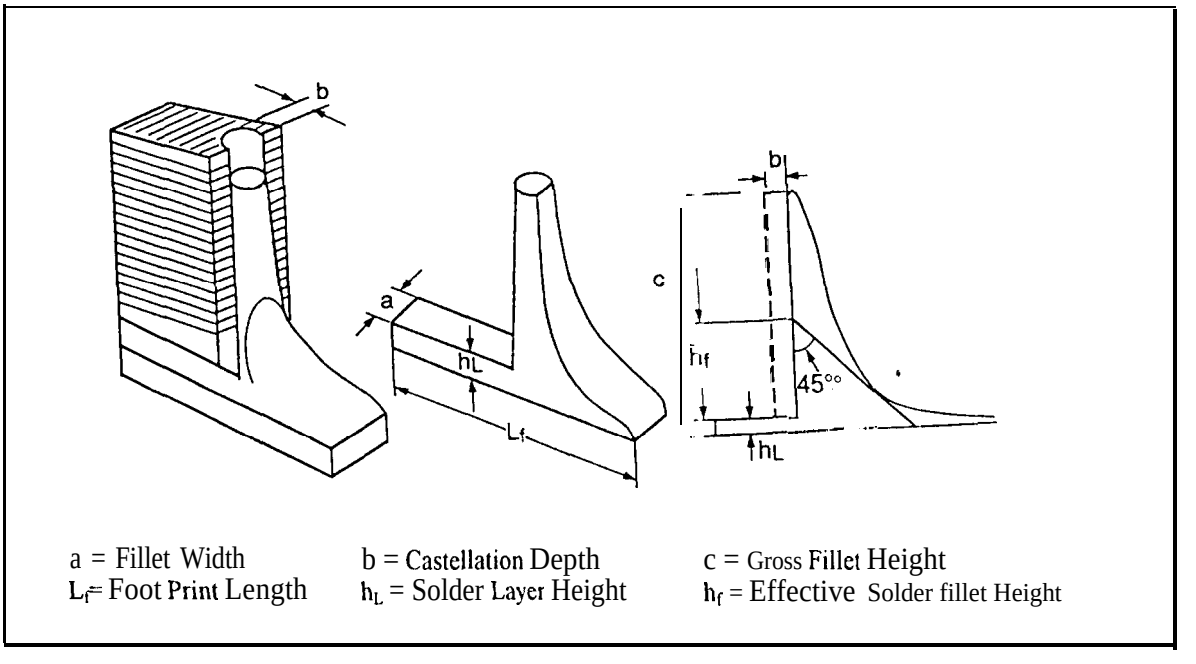
Measurements were made of a sample of the castellations on the three sizes of LCCs. One castellation on each of the four sides of a 20-, 28- and 68-pin was randomly chosen for measurement. Table 1 lists the width, depth and height of the castellations (Figure 3) and the effective solder joint height. All dimensions are in inches. Note that there is considerable variation in the depth of the castellations on the same part. This variation in depth may account for the difference in the depth of solder fillets observed when similar solder joints are sectioned.

Also note that the widths of the 20-pin and the 68-pin LCC castellations seem to be the same, while the 28-pin LCC castrations are wider. This may account for differences in fillet height for a given amount of solder. These translate to the variation of effective solder heights, one of the key parameters that define solder joint reliability of LCCS. For reference, the range of dimensions provided by MIL-STD- 1835, "Microcircuit Case Outlines", is also listed. Although the parts measured fall within acceptable tolerances, the tolerances are so broad, and the observed variations are so great, that no matter how accurately solder paste volume is controlled, solder joints will have considerable differences in shape due to the dimensions of the castellations.

Since the shape of the joints vary in accordance with the dimensions of the castellation and the solder paste volume, the inspector saw joints which had a range of shapes which were acceptable, but looked slightly different, even on the same part. The requirement's for acceptability are as defined in the inspection requirements applicable to the particular project. At present, there is no single industry accepted document which specifies the requirements for surface mount solder joints.

TABLE 1. Castellation Dimension and Solder Fillet Height

Type	Side	Width a	Depth b	Height c	Effective Solder Fillet Height h_f
20-pin LCC	1	.017	.0075	.068	.0236
	2	.013	.0039	.071	
	3	.017	.0080	.075	
	4	.017	.0100	.075	
28-pin LCC	1	.020	.0156	.063	.033
	2	.020	.0136	.067	
	3	.020	.0133	.066	
	4	.0198	.0145	.064	
68-pin LCC	1	.017	.0087	.067	.021
	2	.017	.0080	.068	
	3	.017	.0069	.068	
	4	.0165	.0060	.067	
MIL-STD-1835	LCCS 20,28,68	.006-.022	.003-.015	.05-.088	



a = Fillet Width
b = Castellation Depth
c = Gross Fillet Height
L_f = Foot Print Length
h_L = Solder Layer Height
h_f = Effective Solder fillet Height

FIGURE 3. Solder Joint Configuration for LCCs

LCC SOLDER JOINT MANUFACTURING DEFECTS

Table 2 lists summary defects observed for LCC assemblies during the manufacturing inspections prior to thermal cycling. This Table also includes defect codes used for Phase 1 testing that include other packages, e.g. code 29 for gull wing, as well as those generally used for crack propagation mapping (codes 13 to 20).

As the Table shows, no dewetting or non-wetting was observed. Defects such as icicles, solder bridging, inclusion, void, and light stress defects were extremely rare. The next most commonly occurring significant manufacturing defects were associated with the improper control of solder paste amount, including observations of excess and lumpy solder

TABLE 2. Defect Codes and Types for Identification of Solder Joint Quality

Defect Code/Type	68 LCC	28 LCC	20 LCC
1 NO MFG DEFECT	138	107	32
2 SOLDER BALLS	23	33	0
3 DEWETTING	0	0	0
4 NON-WETTING	0	2	0
5 INCLUSION	0	5	0
6 VOID	3	0	0
7 ICICLES	7	2	0
8 INSUFFICIENT SOLDER	401	64	46
9 EXCESS SOLDER	0	3	11
10 NO FILLET	0	0	0
11 LEAD OVERHANG	0	1	0
12 CONTAMINATION (ON SOLDER)	477	30	0
13 LIGHT STRESS	0	0	0
14 MODERATE STRESS	0	0	0
15 HEAVY STRESS	0	0	0
16 POSSIBLE CRACK	0	1	0
17 CRACK@ 25% FEATURE LENGTH		0	0
18 CRACK@ 50%	0	0	0
19 CRACK @ 75%	0	0	0
20 CRACK @ 100'%	0	0	0
Total assemblies*	24	73	8
Total Joints	1632	2044	160

Defect Code/Type	68 LCC	28 LCC	20 LCC
21 SOLDER BRIDGE	0	6	0
22 GRAINY SOLDER	1429	1866	90
23 LUMPY SOLDER	9	66	4
24 STRETCH MARKS	10	131	3
25 BOARD CONTAMINATION	623	364	20
26 INSUFFICIENT TINNING	0	2	0
27 LEAD SOLDERED TO BODY	0	0	0
28 LEAD TOO HIGH	0	0	0
29 TOE DOWN	0	0	0
30 LEAD DEFORMED	0	0	0
31 DAMAGED JOINT	0	0	0
32 CONTAMINATION (IN SOLDER)	0	0	0
33 HEEL NO FILLET	0	0	0
34 OPEN	0	0	0
35 LUMP SOLDER ON LEAD	0	0	0
36 CYCLING PEEL OFF	0	0	0
99 NO CYCLE STRESS DEFECT	0	0	0

* Note: Some of the assemblies fabricated were not inspected and thermally cycled

joints. Solder joints with excess solder were few while the number of joints with insufficient solder were very high. Solder and board contamination commonly occurred, The grainy solder (defect 22) was the single most frequently observed defect with a percentage of more than the total percentages of solders with other defect types,

THERMAL CYCLING TEST RESULTS

SOLDER JOINT CRACKING AND FAILURE D}; TECTION

At JPL, the conventional pass/fail criterion relies on visual inspection at 10x to 50x magnifications. For leaded parts, once cracking is observed, more than an one order of magnitude additional cycles are required before the failure. For leadless assemblies this is not the case. The cracks usually initiate inside the joint, at the corner underneath the part, and propagate outward. Figure 4 illustrates SEM photos of a corner solder joint of a 68-pin LCC assembly from initial to final failure showing damage propagation with cycles. For this particular test assembly, cracks were not observed until 47 cycles. Complete cracking and failure occurred after 71 cycles.

VISUAL INSPECTION-DATA PLOT AND CORRELATION TO SEM

Visual inspection during thermal cycling test has yielded large quantities of inspection data. When viewed as raw data or a data summary report of abstract numbers, it is difficult to visualize what is actually occurring, and one tends to get "lost" in the numbers. An innovative way of displaying inspection data has been developed which allows instant visualization of the data, especially the correlation with pin location on the inspected part. This method may be adapted for use with other types of data, and in conjunction with other graphical display methods to easily visualize data patterns.

Figures 5 illustrates the use of this type of plot for the 28-pin LCC assembly with the 29-235 serial number. This sample failed after 652 thermal cycles as detected by the Anatech®. The X and Y axes depict the pin locations of the part. The Z (vertical) axis depicts a qualitative relative value assigned to various levels of stress, from 1 (no visible damage) through 9 (100% feature length crack, dark bars

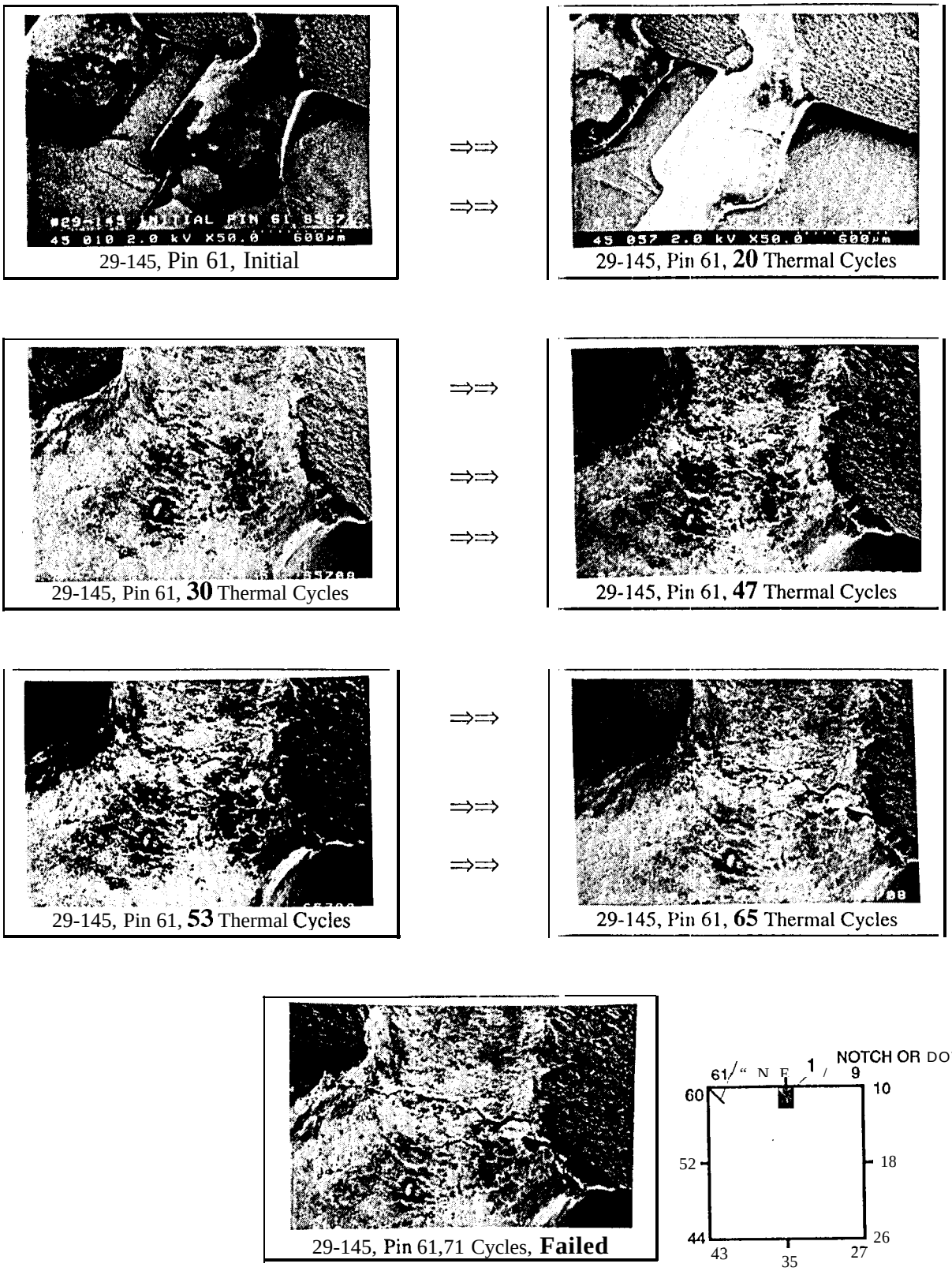


FIGURE 4. SEM Photos of Crack Propagation for 68-Pin Leadless Chip Carrier

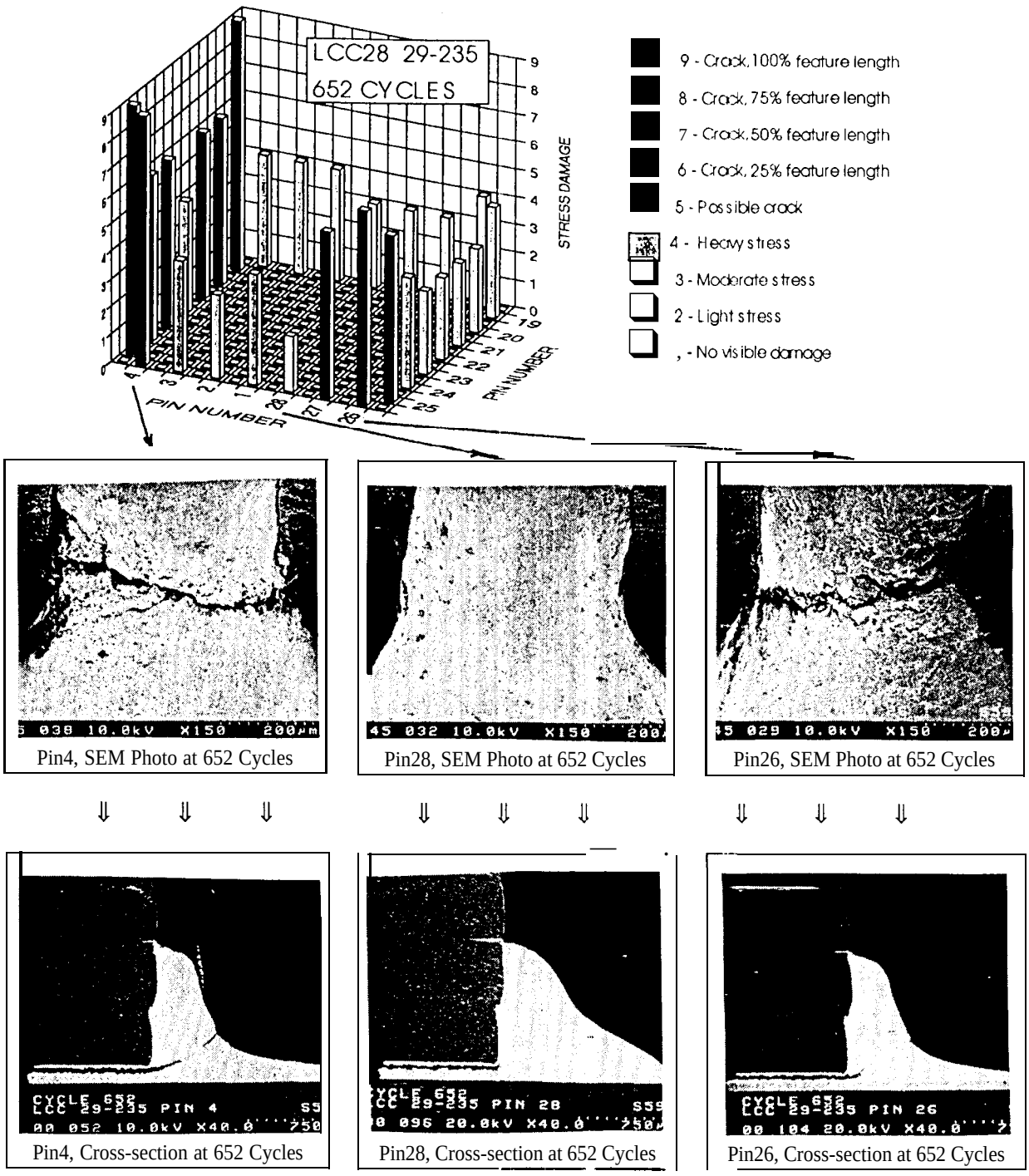


FIGURE 5. PLot of Ranking Solder Joint Damage Levels by Visual Inspection. SEM and Cross-sectional Photos for solder joints with different damage levels

The solder joints at one side of the assembly received considerably more damage than did the opposite side. Apparent damages also increase as moving away from center and are maximum at the corner solder joints. The results confirm the assumption generally made in theoretical modeling that the corner joints with the maximum Distance from Neutral Point (DNP), should typically fail first

Visual inspection results need to be verified by SEM and cross-sectional microscopy in order to gain confidence in data for analysis and crack propagation mapping. For comparison, SEM and cross-sectional micrographs for the selective leads with increasing damage levels are also shown (Figure 5). It appears that even though inspector does not access to the inner of solder joints that crack initiates, if they are trained, they will possess ability to provide inspection results that correlate well with cross-sectional micrograph results. To be effective in Qualification Inspection, the QA inspector need to be trained in inspection procedures and to be provided with a well categorized list of observable damages and correlation to inner solder joint characteristics and relationship to life cycles.

CYCLE STRESS AND CRACK MAPPING

Visual inspection results, proven to correlate well with SEM and cross-sectional evaluation, were used for crack propagation mapping during thermal cycling. The progress of crack propagation over time are graphed using data visualization technique developed (Figure 5). Figure 6 shows plots of data with thermal cycle for 29-235 assembly, a 28-pin LCC on FR-4. Eight inspections were performed on all 28-pin assemblies, but due to quantity of the assemblies and number of leads to inspect, during cycling inspections only the comer and center leads on each side were inspected. Full inspection similar to those after manufacturing were performed when failure detected by Anatech®.

The first visible indication of stress occurred between the 20th and 55th cycles, mainly in three corner solder joints. One of the lead was further damaged and showed signs of possible cracking at 203rd inspection cycles, {Unfortunately no inspections were performed between 203 and 589, when (apparently) much damaging activities occurred, The corner pin 4 showed almost full cracking at 589th cycles. This pin showed 100% cracking at the last inspection (652 cycles) performed after failure detection by Anatech®.

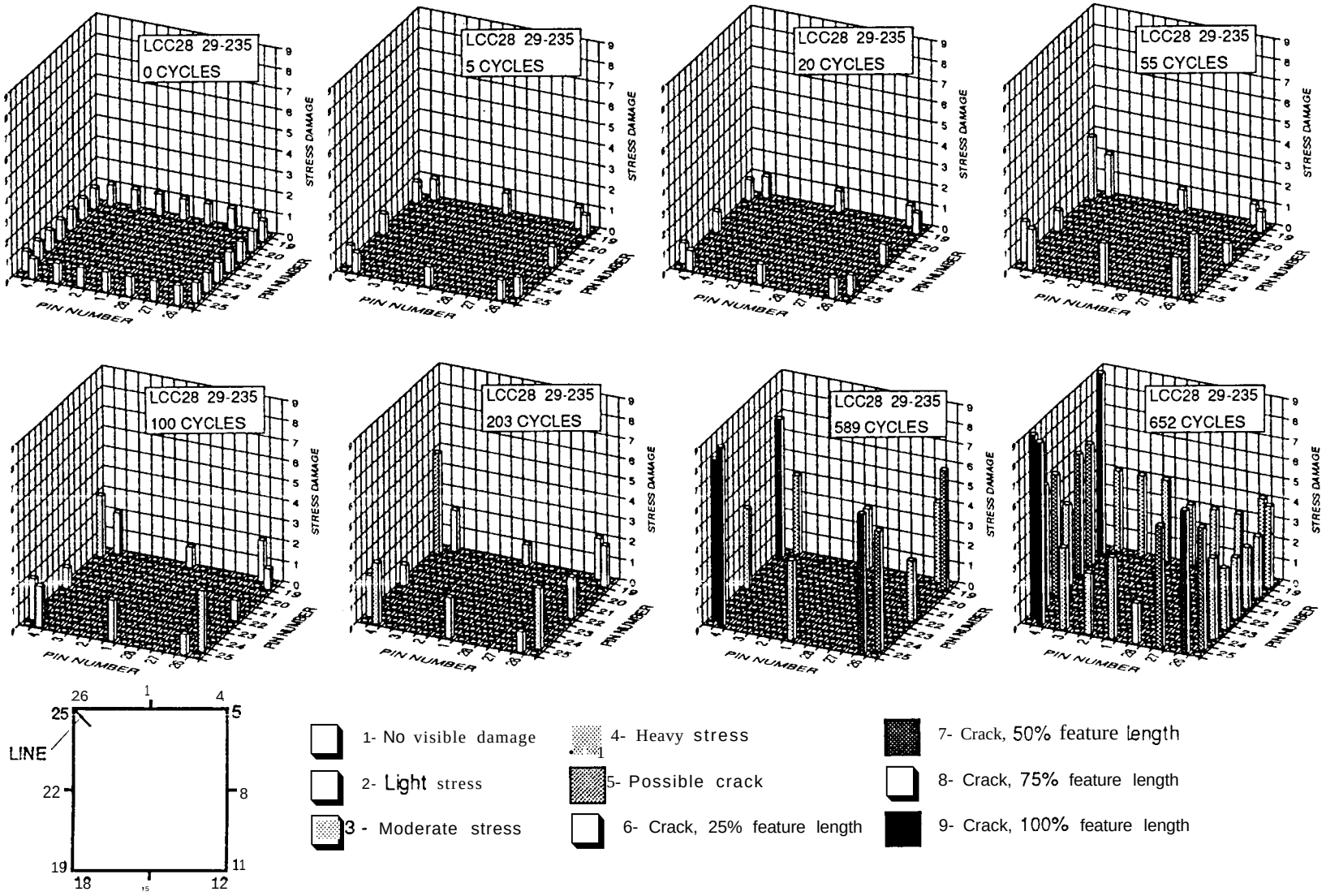


FIGURE 6. Cycling Stress and Crack Propagation for 28-Pin LCCC

CYCLES TO FAILURE AND WEIBULL DISTRIBUTION

Figure 7 shows cycles to failure for 68-, 28-, and 20-pin LCC assemblies. Failures were detected by Anatech® and verified by visual inspection. The failure distribution percentiles were approximated using median plotting, position, $F_i = (i-0.3)/((n+0.4)$. As expected, there was a large spread in cycles to failure because of variance in solder joint volume, quality and location. The first failure for the 68-pin LCCs was detected at 53 cycles while the last sample failed after 139 with 93 average cycles. 28-pin LCCs failed at much higher cycles in the range of 352 to 908 with 660 average cycles. The 20-pin cycles to failure were in the same range as for those of 28-pins and failed within 573 to 863 averaging 674 cycles.

If only DNPs are considered, the 20-pin LCCS should have failed at higher cycles. Cycles to failure is directly proportional to DNP. However, cycles to failure also inversely depends on the effective solder fillet height. As listed in Table 1, solder fillet height is lower for 20-pin (.02 1), which is lower that that for 28-pin (.033) I. CC. The difference in part size could have been off-set by the difference in the fillet height.

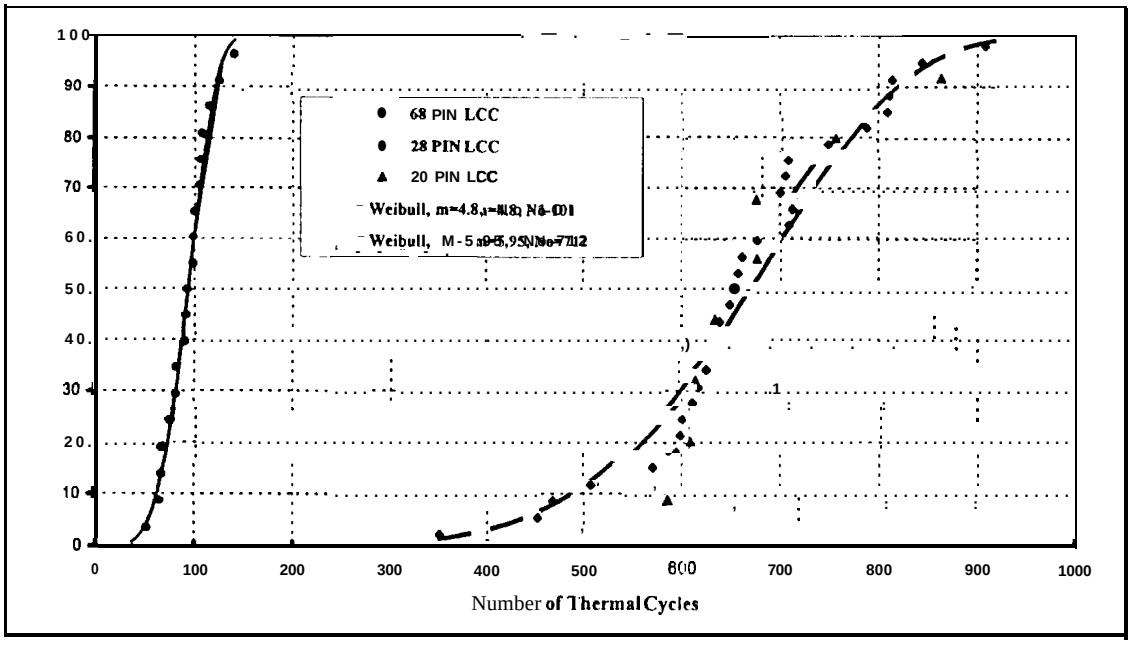


FIGURE 7. Cumulative Failure Distribution Plots for LCC Assemblies

Often, two-parameter Weibull distributions have been used to characterize failure distribution and provide modeling for prediction in the areas of interest. The Weibull cumulative failure distribution was used to fit 68- and 28- pin LCCs' cycles to failure data. The equation is

$$F(N) = 1 - \exp\left(-(N/N_0)^m\right)$$

where

F(N) is the cumulative failure distribution function
N is the number of thermal cycles
No is a scale parameter that commonly is referred to as characteristic life, and is the number of thermal cycles with 63 .2 °/0 failure occurrence
m is the shape parameter and is inversely proportional to the coefficient of variation (CV) by 1.2/CV, as m increases, spread in cycles to failure decreases

This equation, in double logarithm format, results in a straight line. The slope of the line will define the Weibull shape parameter. The cycle to failure data in log-log were fitted in a straight line and the two Weibull parameters were calculated. The Weibull graphs are plotted in Figure 7 as solid and dash lines for 68- and 28-pins, respectively. For 68-pin LCCs, the scale and shape parameters were 101 cycles and 4.8, respectively. These were 712 cycles and 5.95 for the 28-pin LCCs. Both data sets showed excellent linear correlation in log-log plots with a coefficient of correlation of at least 0.97.

MANUFACTURING DEFECTS AND RELIABILITY CORRELATION

Effects of manufacturing defects on solder joint reliability were determined using visual inspection data. The crack propagation was mapped over time for solder joints with a manufacturing defect categories including grainy and insufficient solder joints. Analysis of damage growth enable one to quantitatively define the criticality of each defect category, and based on the results, provide general or specific guidelines for the rejection of manufacturing defects.

Visual inspection data plots and interpretation could also provide a damage level indicator that could be used for identification of solder joint types with potential reliability problems. These methods could be adapted for use with other type of data, and other graphical display methods for ease of data visualization and trend recognition.

Inspection data collected for defects prior to and during cycling needed to be categorized for identification of trends and data analyses. Figures 8 and 9 show an approach that tracks damage growth of individual solder joints and graphs damage accumulation for solder joints with specific manufacturing defect categories. Steps used to develop these graphs are as follows:

1. Assigned a manufacturing defect type to each damaged lead. If a solder joint showed two or more defect types, then either one was selected or was not considered for data categorization. For example, occasionally solder joint lead with no defect (code 1 of Table 2) in one section also showed solder balls/splash (code 2). In this case, the effect of solder balls was considered to be minor in affecting reliability and therefore the lead was categorized as "no defect". In some cases, solder showed both grainy (code 22) and insufficient solder (code 8). For these cases, half of the leads were assigned code 22 and the other half were assigned code 8. They were then included in the new database.
2. Selected the most severe case of damage level when damage levels were different for the section of a solder joint lead.
3. Took into account damage level for each lead only one time, the first time that damage type was observed.
4. Categorized solder joints irrespective of joint location in the part.
5. Generated missing damage levels between two consecutive inspection observations by adding imaginary inspection cycles between the two.
6. Counted the number of leads with a specific damage level for each cycle including imaginary ones. Accumulated these numbers from low cycles to high cycles and then discarded the imaginary cycles.
7. Plotted accumulated number of damage level versus the number of cycles (Figure 8). Damage percentages were calculated using these numbers for different damage levels and then dividing them by the accumulated number of light stress damage observations (Figure 9).

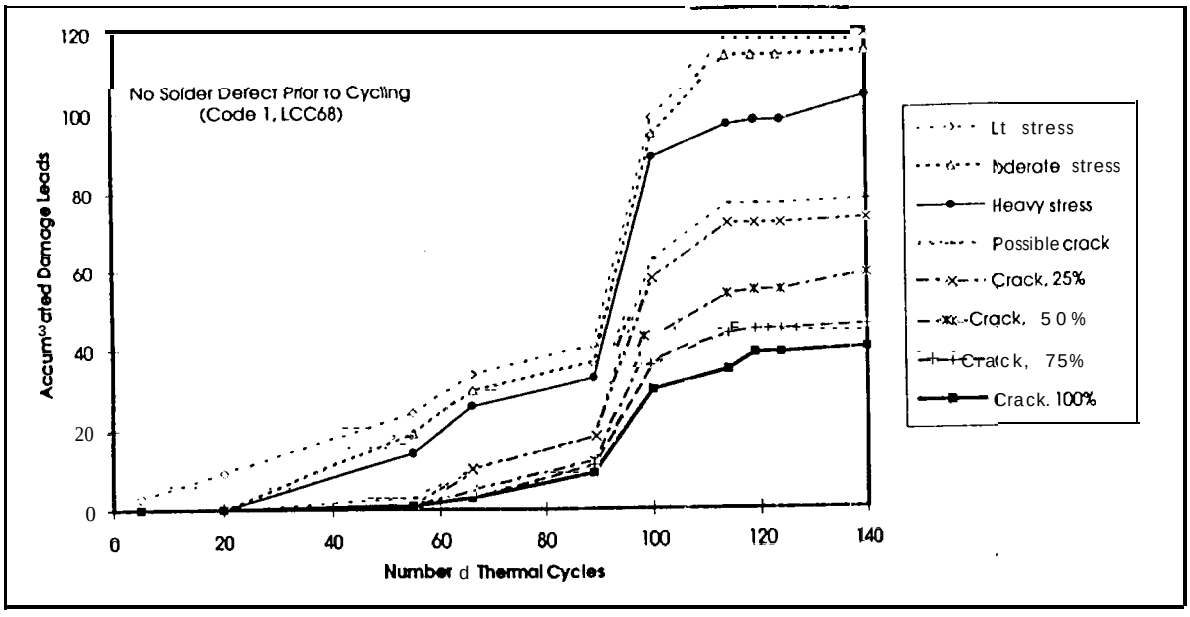
Plots include sound solder joint leads and those joints with either insufficient and/or grainy, or excess solder joint defects (code 8 and/or 22, or code 9) prior to thermal cycling. In each plot, the x axis represents cycles and data points are vertically lined up at cycles with the solder joints that were inspected, The y axis represents damage accumulation magnitude or percentages (light stress, heavy stress, crack with 100°/0 feature length, etc.).

For 68-pin. LCC, two types of defect categories were included in one plot, there were 930 grainy and 180 insufficient solder joints with 100 having both defects, It is clear from the plots, that the solder joints with a higher defect category showed earlier signs of damage growth as well as accounting for higher failed joint percentages.

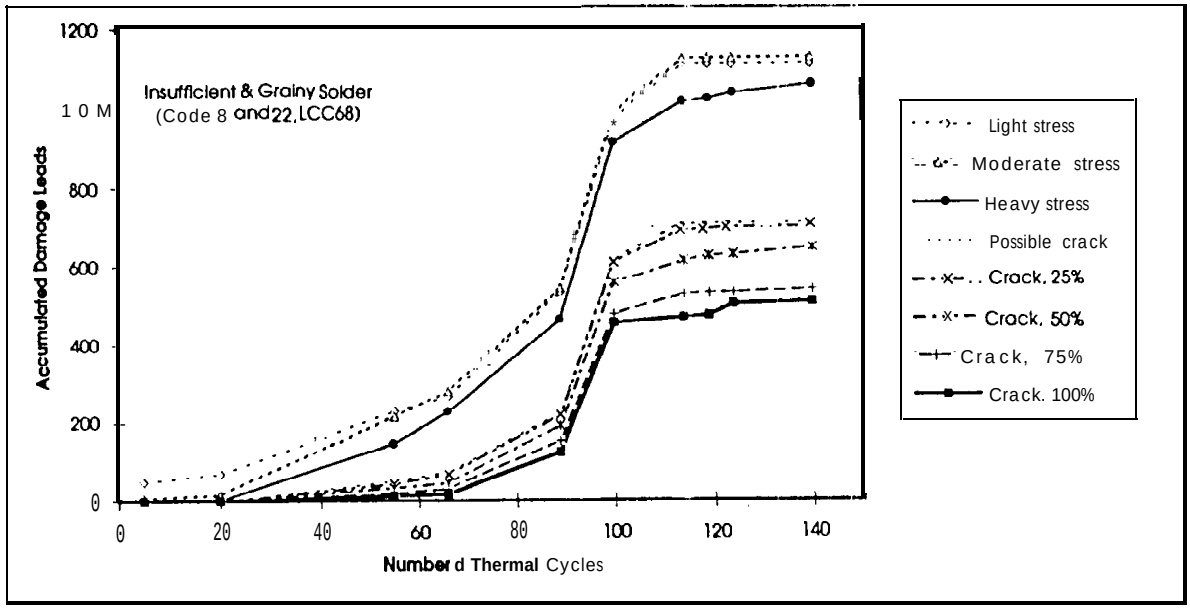
For 20-pin LCC, all joints showed signs of light stress damage after only a few cycles. They started to change rapidly to the more severe damage at approximately 200 cycles. Leads with excess solder showed a damage growth trend over cycle time similar to those with no visible manufacturing damage. On the other hand, grainy and insufficient solder leads with a roughly similar crack growth trend showed much higher levels of cracking above and below 600 cycles when compared to joints with the excess solder.

It was hoped that the results provide a visual damage level indicator such as signs of heavy stress for those solder joints with manufacturing defects that markedly differ from those with no defects. Therefore this could be used for qualification testing. Unfortunately, possibly because of short cycles to failure of 68-pin and missing inspection data for 20-pin LCC, we are unable to use these plots at this point to forecast reliability problems.

However, it can be seen from these figures that the percentages of failed leads for those with manufacturing defects are markedly higher than those with no defects. Additionally, the majority of leads with manufacturing defects failed earlier than those with no defects. The failure data points for these defective leads appear to be concentrated on the tail of the Weibull distribution, possibly from a different population than those leads with no manufacturing defects,

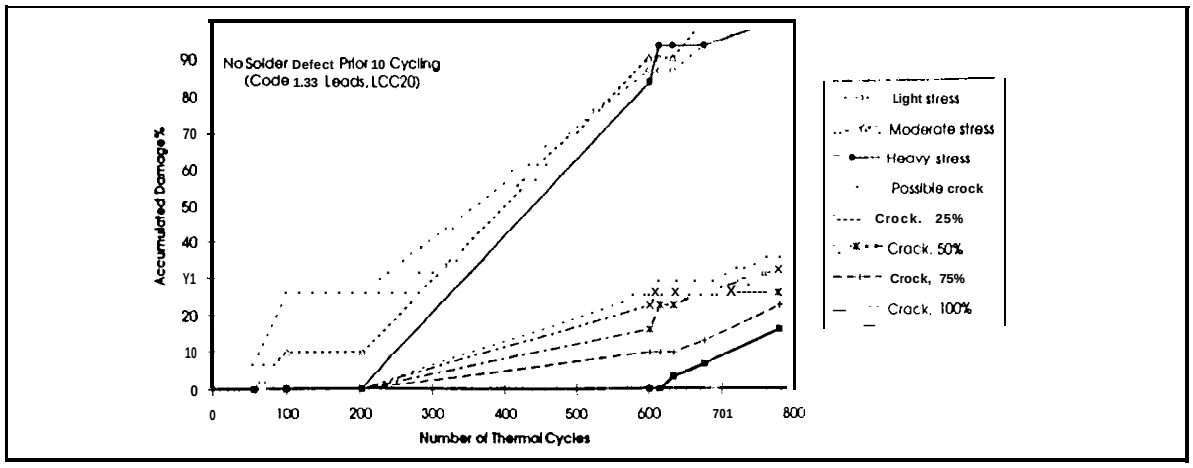


a) Solders With No Signs of Manufacturing Defects

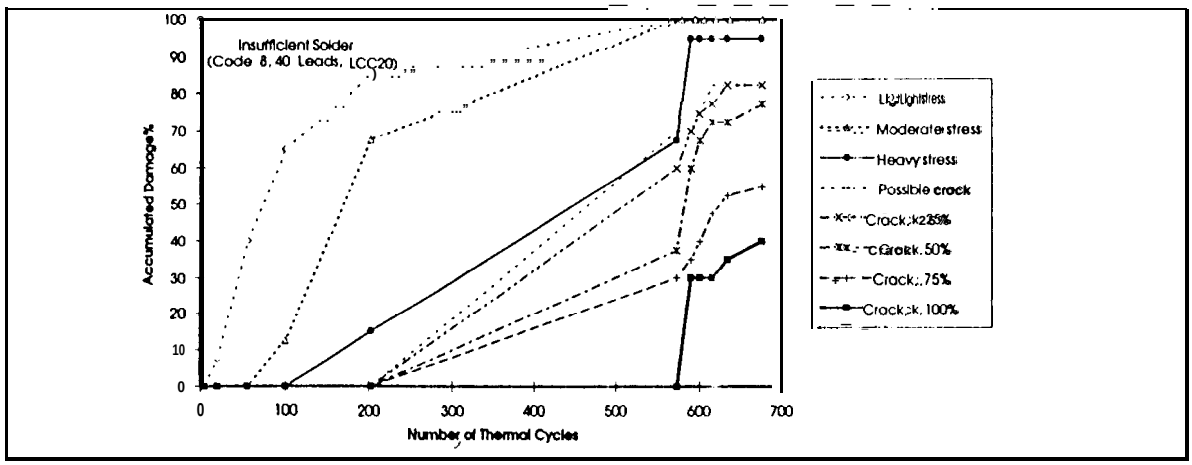


b) Solders With Signs of Insufficient and/or Grainy Solders

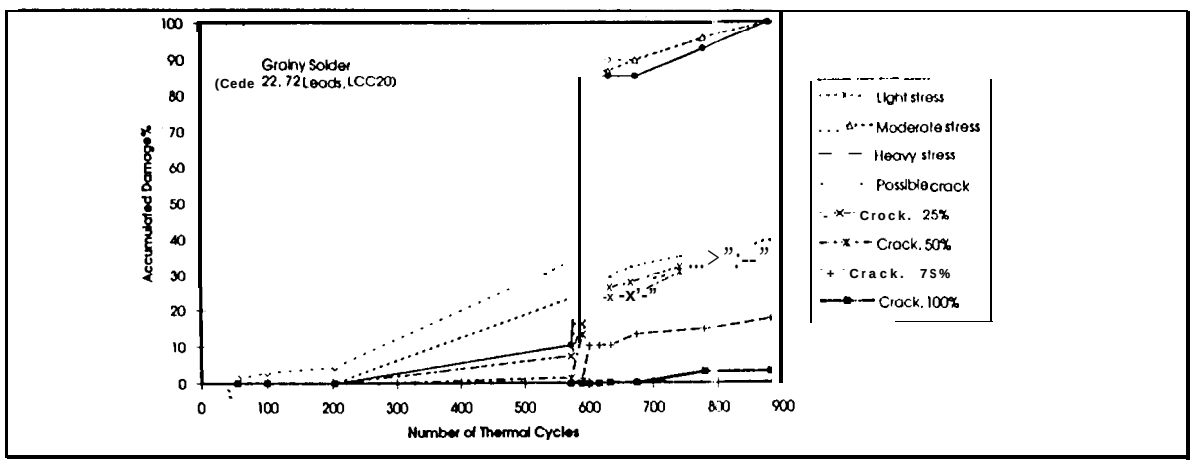
FIGURE 8. Accumulation Number of Damage Levels for 68-Pin LCC Solder Joints With No Signs of Manufacturing Defects and Those With Insufficient and Grainy Solders



Solder Joints With No Signs of Manufacturing Damage



Solder Joint Terminations With Insufficient Solders



Solder Joint Terminations With Grainy Solders

FIGURE 9. Accumulated Damage Level Percentages for 20-Pin LCCs With No Signs of Manufacturing Defects, Insufficient and Grainy Solders

DISCUSSION

Ultra-low volume surface mount assemblies considered for space applications do not permit the proof of process potential as commercial or military production quantities. This fact mandates that Quality Assurance involvement be proactive and be included throughout the process of validation and proof of process build, and as well as problem detection by inspection. The QA engineer should be responsible for ensuring that manufacturing controls are in place and that critical steps are considered and understood for inspection. In this cooperative investigation, the QA role being proactive and concurrent resulted in better understanding of some of the critical parameters in solder joint reliability as well as more confidence in the methodology of visual inspection. In correlating visual inspection results to those of SEM and microsectioning, it was clearly demonstrated that once trained, QA personnel would indeed be able to detect solder joints with potential reliability problems.

One aspect of this investigation is to better understand the interplay of manufacturing defects and reliability, and to provide QA personnel with the necessary tools to increase their effectiveness in detection of solder joints with potential reliability problems, To establish such criteria, visual criteria such as signs of heavy stress or crack initiation and possibly in combination with thermal aging including signs of grainy due to grain growth and ball spreading need to be investigated. The approaches demonstrated here including the crack propagation mapping over time for solder joints with a defect category was aimed to provide a quantitative definition about the criticality of each defect category. Qualitative indicators could be used to inspect these solder joints that do not meet cycle requirements for a mission thermal environment,

It was hoped that the interpretation of results of solder damage progress would provide the required quantitative visual indicator. Plots for cycles to failure for 20-pin and 68-pin, because of missing inspection data intervals and combining solder joints irrespective of lead location could be used only to come to conclusion that those defect categories investigated result in early failure and possibly cause reduction of the Weibull shape parameter (increase in coefficient of variation).

Elimination of the cause of such defect will decrease failure spread and therefore provide higher confidence in predicating reliability for a significantly lower rate of failure.

Currently results for 28-pin LCC with nearly 1,000 solder joints are being analyzed to determine if a more definite trend could be established. Results will be analyzed similarly to those presented here as well as considering corner and center joints separately. Similar techniques will also be used for leaded parts of SMT Phase l and Phase 2 test programs

and data will be presented as they become available. Phase 2 testing will include polyimide board assemblies with a variety of components that employ design of experiment methodology to include the effect of manufacturing variables as well as changes in thermal cycling range and testing in a vacuum environment. Based on the results, QA will provide general or specific guidelines for the acceptance/rejection of solder joints for a mission thermal environment.

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BIOGRAPHY

Dr. Reza Ghaffarian has more than fifteen years of industrial and academic experience in mechanical, materials, and manufacturing processes engineering. At JPL, He supports research and development activities in SMT for infusion in NASA' missions including projects in advanced electronics packaging, interconnection, and assembly. His responsibilities include technical coordination, Design of Experiment (DOE) statistical test vehicle implementation, manufacturing process, inspection methodology development, failure analysis, and environmental test data collection and analysis. Dr. Ghaffarian has authored or co-authored over 15 technical papers and numerous patentable innovations. He has also organized and chaired many technical sessions. He received his M. S. in 1979, Engineering Degree in 1980, and Ph.D. in 1982 all in Engineering from University of California at Los Angeles (UCLA).