Accelerated Testing of GaAs FETs; Dealing with the Nigtmare of Test Result Interpretation

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Paper Abstract

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The primary goal of accelerated tests is to determine in a relatively short or reasonable time period whether the parts are adequate for use. Good test results are normally an objective or a happy ending of any test; i.e., all parts pass the test, or the parts fail with a known failure mechanism. A nightmare happens when there appear failure modes never seen before, or the budget constraints require the use of tested devices even if the test results are questionable.

This paper presents three test cases:

1. Accelerated testing of the power GaAs FETs and the process and rationale of making an accept or reject decision;

2. Accelerated testing of the signal GaAs FETs and using results to derive a decision about the use of the devices at elevated temperatures;

3. Unknown failure modes found in accelerated testing that do not allow or as a minimum aggravate decision making process about qualification of these devices for use in any environment.

The paper addresses methods to prevent decision and failure mode problems associated with the accelerated testing of the GaAs FETs as follows:

- Method for well defined accelerated testing of the power GaAs FETs with the strict derating criteria.

- Method for accelerated test and monitoring of the signal GaAs FETs which would yield useful information for reliability estimation of the devices.

- Specific accelerated test set-up for MM] Cs, where electrostatic discharge and piesoelectricity are to be considered as a serious threat to the devices.

The paper presents case studies and conclusions made based on the extensive test experience.

About the Author:

Tien Nguyen is a Member of Technical Staff in the Project Reliability Section of the Jet Propulsion Laboratory in Pasadena, California. His specialties are: Device Physics, Device Modeling and Failure Physics, Electronic Circuit Analysis (Worst Case, FMEA, Part Stress, Sneak Circuit/Path Analysis, and Electromagnetic Compatibility). He has worked on various JPL Space projects such as Galileo, Magellan, Mars Observer, Cassini, and others. Prior to joining JPL, Mr. Nguyen was a design engineer at Burrough, working on design of the EMC processor for the P5 project, and the instrumentation Control Engineer at Bechtel working on the ANPP project.

Tien Nguyen holds three Bachelor of Science degrees in Electrical Engineering, Mechanical Engineering and Physics from California State University Fullerton, and two Master of Science degrees in Electrical and Mechanical Engineering, also from the CSUF.