

Hardness Assurance and Testing Techniques for High Resolution (12-to 16-bit) Analog-to-Digital Converters*

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Introduction

During the last two years, many different analog-to-digital converters (ADCs) from different manufacturers have been total dose radiation tested and electrically characterized. Because these high-speed, high resolution ADCs are critical parts in a digital signal processing or data acquisition system, the evaluation of performance in the early design phase is very important. However, the electrical characterization test set-up is complex and time consuming, and requires expensive high-speed mixed-signal test systems with delicate handling and care. For example, the dynamic range of a 16-bit ADC is between 120-130 dB. Setting-up an electrical characterization test system with a noise floor below this level is a challenge and requires a tremendous effort.

This paper discusses techniques to test and evaluate total dose radiation on high-resolution successive-approximation converters that eliminate the need to test each individual bit or transition. With a few critical parametric measurements, one can determine an approximate radiation failure level for the converters, that will provide a good approximation of the converter response for total dose radiation evaluations and significantly reduce testing costs.

ADCs from three different manufacturers are discussed in this paper. They are designed and fabricated with commercial BiCMOS and CMOS processes. The 16-bit converter is designed by Crystal Semiconductor, the 14-bit converter is from Analog Devices, and the 12-bit converters are manufactured by Maxim. All three devices use much higher power supply voltages than digital CMOS, and consequently they have much thicker gate oxides, which adversely affects their radiation hardness.

As converter designs have evolved to increase resolution, speed, and accuracy, their radiation tolerance has diminished. The total dose radiation failure level for 12-bit converters was about 8 krad(Si), the 14-bit converter was about 4 krad(Si), and the 16-bit converter was 2 krad(Si). Even though newer designs

have much smaller steps between successive bits, the failure modes are generally more global, and can be detected without the extreme accuracy required to reduce single LSB errors. When a converter fails functionally, some parameters can not even be measured. Therefore, it is also important to check the converter functionally. This must be done over the entire voltage range, but can be limited to major code transitions.

Each converter has its own characteristics to fit various circuit applications and provides flexibility for many design applications. The three converters use different architectures. The 16-bit device is an unusual design that uses an internal microprocessor and error register to provide self-calibration of first-order inaccuracies. A simplified functional block diagram is shown in Figure 1. In addition to the microcontroller and calibration circuits, this device uses a switched-capacitor digital-to-analog converter (DAC). Although one would expect this approach to improve total dose radiation hardness, this device was by far the most sensitive to total dose degradation.

The 12-bit converters have an internal reference voltage and clock along with conventional digital subfunctions such as SAR, control and timing logic. They are fabricated with a BiCMOS process.

Testing Techniques and Test Results

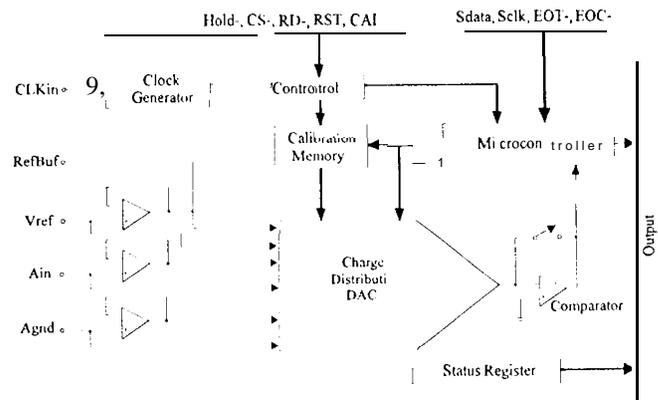


Figure 1. (S5016 Functions] Block Diagram [1]

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16-bit ADC (CS5016)

Recently, a radiation test of Crystal Semiconductor's 16-bit A/D converter, CS5016 was completed for the JPL Cassini project. The converter is fabricated with a 3 μm CMOS process with a total power supply voltage of 10 V. However, the analog input range is only 4.5 V in unipolar mode resulting in an LSB of 68,7 μV . It uses a switched capacitor based architecture, with internal microprocessor control and error calibration. Most other ADCs use a laser trimmed thin film technology with a ladder network based on current sources.

Despite the internal self-calibration circuitry, the converter failed functionally and parametrically at very low total dose levels when tested at a high dose rate of 50 rad(Si)/sec. Converters recovered both functionally and parametrically during a room temperature (25 °C) annealing test and did not show any rebound during a high temperature (100 °C) annealing test.

A histogram based test was setup to measure the converter linearity. The histogram test is a statistical method of deriving the converter's differential nonlinearity (DNL). A spectrally pure sine wave along with an active low pass filter was applied at the input of the converter. Only one million samples were taken due to the limited radiation test time period, but it provided enough information about the 16-bit converter performance. In this test, a code with more or less occurrences than average appears as a DNL, greater or less than zero LSB.

Using this approach, DNL failed below 5 krad(Si) as shown by the large number of missing codes in Figure 2. DNL errors in successive-approximation A/D converters are caused by bit weighted errors and comparator dynamic errors. In this self-calibrating converter, the comparator dynamic errors are the major factor in DNL errors. The comparator does not have enough time to settle during each bit decision making process in

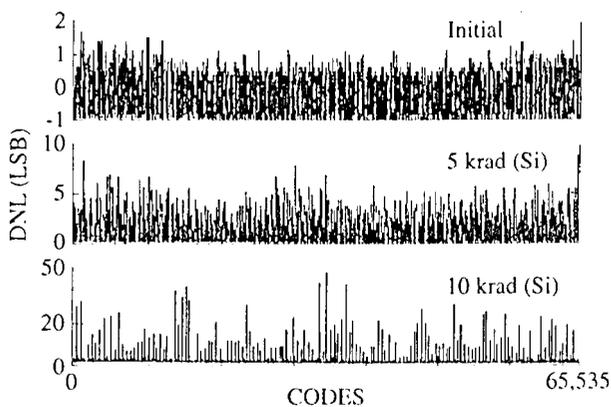


Figure 2. DNL Degradation of 16-bit A/D Converter

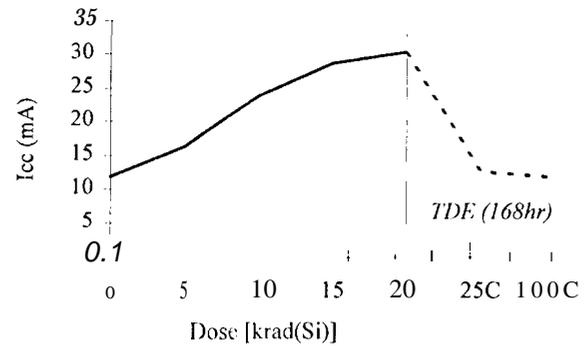


Figure 3. Power Supply Current (Spec. Max = 25 mA) of 16-bit A/D Converter

the successive-approximation algorithm. The worst-case codes for comparator dynamic errors are the major transition codes, especially at the half of the full scale codes.

Power supply current exceeded the specification limit at 10 krad(Si). Figure 3 shows the power supply current degradation; its specification limit is 25 mA. Devices functionally failed at 15 krad(Si). This data indicates that the converter is extremely vulnerable to total dose irradiation. The data was taken with a test set-up using an internal clock.

A reference voltage is one of the most critical parameters in A/D converters because the reference voltage sets the gain of the converter stage since the digital output should correspond to the ratio of the analog input signal to the reference voltage. An external reference voltage of 4.5 V is required for operation of the CS5016 and it passes through an internal CMOS buffer amplifier and fed to the internal 16-bit DAC. The CS5016 uses several CMOS buffers, and the offset of the buffer can be measured with the standard pinout of the circuit (see Figure 1).

The value of the voltage at the output of the buffer amplifier was measured during radiation and it degraded severely enough to cause the converter to fail functionally as shown in Figure 4. Note that significant changes begin to occur at approximately 2 krad(Si), an extremely low level. This may be due to threshold voltage changes in the buffer amplifier. Note that similar buffer amplifiers are used in the analog input and analog ground paths.

The reference voltage of an A/D converter must be extremely stable and precise. The internal buffer amplifier in the CS5016 was designed to help the robustness of an external reference voltage. However, the result was a severely degraded reference voltage after irradiation because of the large offset in the buffer. It was the largest degradation in the converter's performance measurements.

Once an external reference voltage is applied to the converter, internal capacitors in the calibrated capacitor array of the

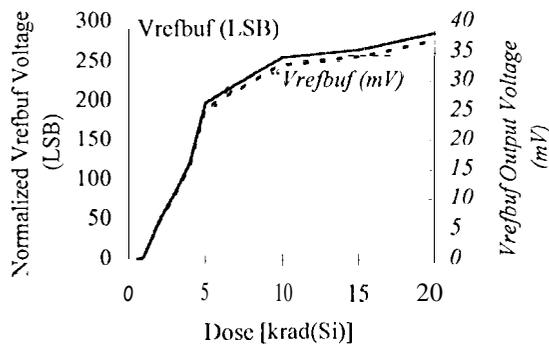


Figure 4. Vref Buffer Output Voltage Degradation of 16-bit A/D Converter

converter switch from the reference voltage to the analog ground level, due to the SAR algorithm. The same CMOS amplifier is used in the internal analog input, analog ground, and comparator circuitry. The internal comparator connects a critical path between the output of the internal DAC and the microcontroller. Degradation in the reference buffer amplifier indicates that the other three application circuits will behave the same way under total dose irradiation, and that will definitely cause conversion errors and parametric failures for the converter.

The 16-bit converter will be tested using Fast Fourier Transform (FFT) techniques to analyze the dynamic performance. Low dose rate testing with internal and external clock applications will be also done for the full paper to compare the results at a low dose rate with high dose rate results.

14-bit ADC (AD7872)

This device is a 14-bit analog-to-digital converter, fabricated in BiCMOS technology. It uses a conventional architecture, with a comparator, internal reference, and successive-approximation register (SAR) using a current-switch ladder network.

The failure level in this device had an unusual dependence on the clock mode. Total dose data showed that SNR and functional tests failed at 4 krad(Si) using an external clock. When the internal clock was used, failure did not occur until 40 krad(Si). These test results show that the usage of the internal or external clock can dominate the total dose radiation failure mechanism. The functional failure level of the converter can be improved significantly, an order of magnitude, using the internal clock rather than the external clock in a circuit application.

The external clock bypasses the laser trimmed internal clock oscillator, connecting the output of the clock circuit directly with the internal CMOS comparator. The input circuitry of the external clock input of the converter uses a CMOS analog switch to bypass the internal clock. The on-characteris-

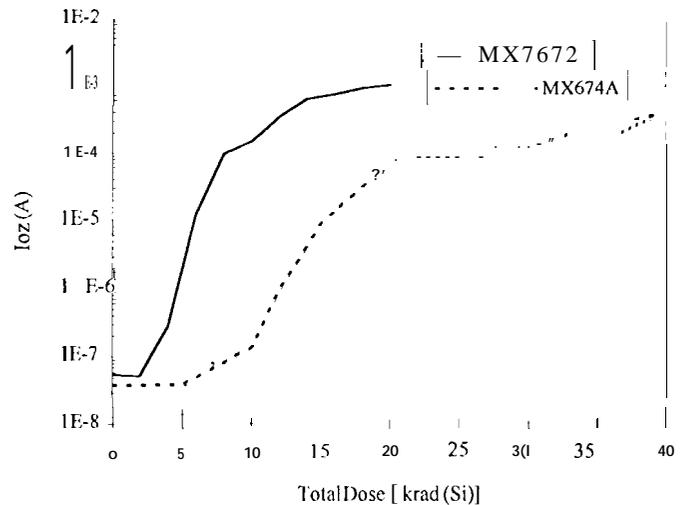


Figure 5. Ioz Degradation of 12-bit BiCMOS ADCs

tics of CMOS switches are often highly sensitive to radiation degradation, which may explain the large difference in the circuit hardness with different clock modes.

Further study is planned to investigate the internal/external clock circuitry of the converter for radiation sensitivity. A localized irradiation test will be performed to analyze the internal clock circuitry with delidded parts since it is not possible to get test structures from the manufacturer.

12-bit ADC (MX7672/MX674A)

These devices are also fabricated with BiCMOS processes, and use a conventional architecture. The CMOS devices have thick gate oxides because of the 18 V voltage rating of these parts. The MX674A has an internal reference voltage, which exceeded the specification limit at relatively low total dose levels. Otherwise, the response of the two devices were very similar.

The tri-state leakage current, Ioz, is one of the most important dc parameters and failed at early levels of radiation. If this parameter is solely tested for radiation without any other parametric test setup, that would still give a very good indication of the radiation failure level for the converter. The leakage current in internal MOS transistors increases due to radiation because the output stage of the converters are fabricated with CMOS devices.

The Ioz parametric failure is caused by oxide traps in the output transistors for these BiCMOS devices. The increase in Ioz with devices statically biased during radiation is shown in the Figure 5. The rapid recovery during an annealing time period indicates that the total dose hardness is strongly affected by the dose rate. [3]

Even though setting up electrical parametric test for these 12-bit converters is simpler than the other two high-resolution converters, it is not a trivial task. However, with the reference voltage and I/O measurements in addition to a functional test (transfer curve) at major transition codes will be more than sufficient for the radiation characterization on these converters.

Conclusions

High-speed, high resolution A/D converters are one of the key components in many new space electronic systems. Testing such devices is a challenging task, especially radiation testing. A simplified testing strategy is crucial for evaluation of these converters within a projected budget and schedule.

A great deal of effort was expended to test these converters to the limits of their precision and accuracy. However, small changes in SNR, INL, and DNL were unimportant until other more easily measured dc parameters exhibited substantial changes. Thus, doing less elaborate tests of dynamic parameters and linearities appears to be adequate, and will save considerable effort and cost, particularly for converters with high resolution.

The 16-bit self-calibration converter, CS50 16 was designed with the latest design technique to improve the performance of the converter. However, due to a basic monolithic CMOS process fabrication, and the way that the circuit design is implemented, it actually performs worse than the other two BiCMOS process converters. Changes in the internal CMOS devices are the dominant failure mode in this commercially fabricated converter, even those fabricated with BiCMOS converters.

Finally, the dominant failure mechanism (typical CMOS radiation failure modes) of internal CMOS devices for low levels of total dose irradiation is common in all converters from three different manufacturers. Therefore, a few parametric tests of internal CMOS devices along with a minimal functional test are the best solution for radiation characterization of these complicated high resolution A/D converters. However, the large difference in failure levels of the 14-bit converter when the clock mode was changed is a new discovery. This will be further investigated for the final paper in both 14- and 16-bit converters.

References

[1]. Crystal Semiconductor Corp. Data Book, "Analog/Digital Conversion IC's," Vol 1, (1992).
[2]. J.R. Naylor, "Testing Digital/Analog and Analog/Digital Converters," IEEE Trans. on Circuits and Systems, CAS-25, 526 (1978).
[3]. C. L. I AX, B. G. Rax, and A. H. Johnston, "Total Ionizing Dose Effects on High Resolution (12-14-bit) Analog-to-Digital Converters," IEEE Trans. Nucl. Sci., NS-41, 2459-2466 (1994).

[4]. S. Pei and S. P. Chan, "New Approach to Linearity Testing of A/D Converters," Int J. Electronics, 1991, vol. 70, No 6, 1049-1062,

[5]. J. Doernberg, H. Lee, and D.A. Hodges, "Full-Speed Testing of A/D Converters," IEEE J. Solid St. Circuits, SC-19 820 (1984),