An Experimental Survey of Heavy Ion Induced Dielectric Rupture in Actel Field Programmable Gate Arrays (FPGAs)*

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Actel FPGAs are very attractive to spacecraft designers and indeed are included on many planned missions [1o wcvci, as highly-scaled, commercial, non radiation hardened devices, they are accompanied by a variety of `radiation issues. Incorporating a unique and patented "antifuse" technology. they may also present special problems. Indeed, in the cou sc 01' routine SEE testing with heavy ions, a new failure mod e was encountered [1] which ultimately was related to ion-induced rupture of antifuses [2] and named single event dielectric rupture (SEDR) for its similarity to gate rupture (SEGR) seen in power M O SFETs [e g 3 and 4]

This paper relates the approach taken and the results obtained during a series of follow-up heavy ion tests to quantify SEDR susceptibility. The experimental approach allows the collection of a statistically significant number of events on a given test part for this destructive mechanism. For all three Actel families of devices, SEDR cross sections were obtained as eight parameters were varied: normal LET, angle, lot, feature size, bias, temperature, operating frequency, and data pattern, as illustrated in Figure 1 for a set of irradiations of ACT II or 1280 devices.

Background

The Actel FPGAs' silicon real estate is about half devoted to logic modules and half to an interconnection matrix (ignoring peripheral circuitry for programming and control functions). The matrix consists of horizontal and vertical conductors with an antifuse occupying, at each crossing, a

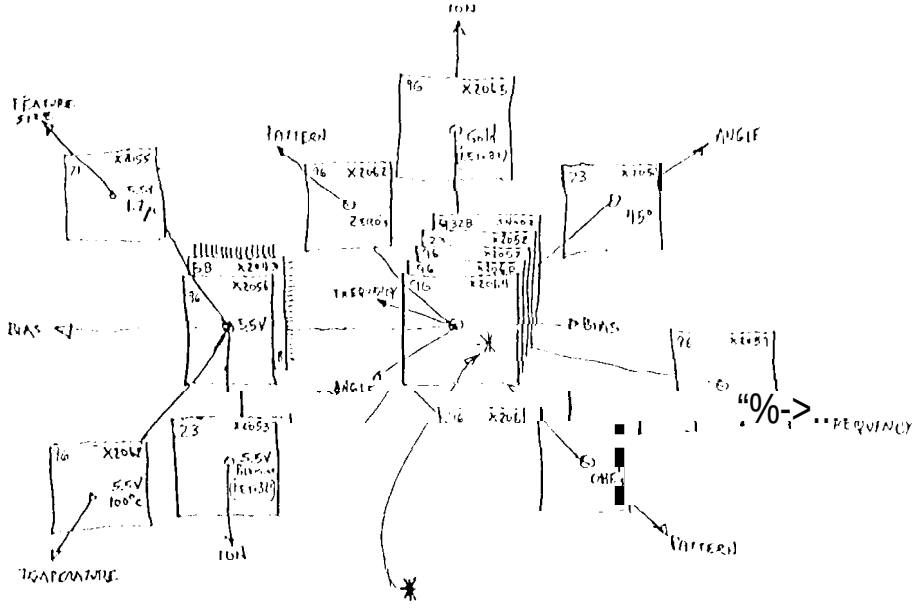

Figure i. 1280 SEDR Test Matrix form BNL Test, 8/2/94
Note the asterisk indicates the matrix "center" of: bias= 5V, size= 1.0 micron, pattern= alternating, ion= iodine (1 .ET= 60 MeV per mg/sq cm, angle= normal, frequency= 2.5 MHz, temperature= room

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circular area defined by the line width. The antifuse dielectric is a thin sandwich of oxide-nitride-oxide or ONO measuring ~80 to 90 angstrom oxide-equivalent thickness. A typical FPGA design will have a few per cent of these connected via electrically induced dielectric breakdown (or rupture). A random unconnected antifuse will be biased when the logic levels on the two crossing conductors are different which obviously depends on the duty cycle and phase of the two signals. There are many of these unconnected antifuses: ~175,000 for 1020s, ~650,000 for 1280s, and ~550,000 for 1460s.

Operating within the 5.5V spec limit, the electric field on the insulating ONO of a biased antifuse is about 6 MV/cm in magnitude, either positive or negative. An undesired connection occurs when a heavy ion "breaks" a biased antifuse. The symptoms of such a connection can be benign with a small current increase only, intermittent due to reduced timing and voltage margins, or hard faults. Obviously, the seriousness of a particular SEDR depends on circuit considerations surrounding the heavy ion programmed antifuse.

Experimental Approach

To measure cross sections for a destructive phenomenon like SEDR, it is important to establish a test method that allows collecting and counting a statistically significant number of events. This is particularly problematic in SEGR testing of power MOSFETs where the test device is destroyed. The two most interesting aspects of the approach of this investigation are the test device program and the methods for counting SEDR events. Since multiple events were accumulated on individual test devices, care was taken to ensure that the cross section lowering, caused by the previous events was not too large.

The test FPGAs were programmed as shift registers with (mostly) triple module redundancy (TMR). Each TMR shift element need only have two of three flip/flops functioning for the test device to continue working, and single flip/flop failures would not change the biasing on the substantial majority of the antifuses. Some details of the TMR design can be found in Ref. 1. During irradiations, a pattern (all ones, all zeros, or alternations) was clocked through the shift registers while SEUs were counted and segment failures were noted. A crude count of SEDR events could be made from the strip charts of the dynamic current drawn (see Figure 2).

Additionally, two other SEDR counting methods have been employed. First, emission microscopy techniques (EMMI) were employed to identify high current nodes. Those noted at antifuse locations correspond to damage sites. These high current nodes could be turned on and off with

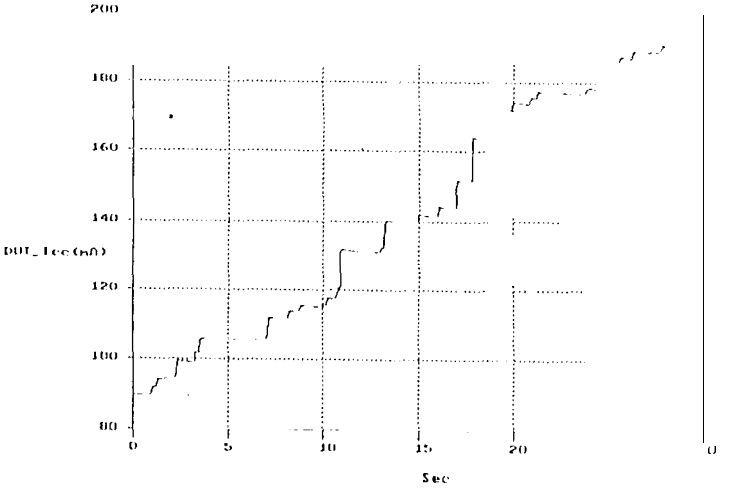

Figure 2. Current during Irradiation of 1280A Device (s/n 350) to a Fluence of 2.5E5/sq. cm of **iodine** (LET = 60 Mev per mg/sq. cm). Other parameters: 5.5V, room temperature, 1.0 micron, 2.5 MHz, alternating pattern.

appropriate vectors in the TMR shift registers. Second, an I_{DDQ} technique was developed consisting of walking a one (and, later, a zero) through each shift element against a background of the opposite state in all the other elements. It was found that this was very revealing, yielding, from the size and magnitude of the current change for each element, the most exact number and type of ion-induced connections. Details of this technique will be forthcoming [5]

Results

Results for tile 1280 devices are summarized in Table 1. (The full paper will expand these, as well as present results for 1020s and 1460s.) The cross sections given are based on the 95%-confidence-level worst-case value for the expected number of SEDR sites from the observed number, This Poisson treatment is necessary because of the small actual numbers 0 to 30

TABLE 1. SEDR Cross Section Variations for Eight Parameters on the Actel 1280

Parameter:		# tested	95% Worst Case Cross Sections (cm^2) Mean	Min	Max.	Note
Ion:	Au (LET= 82)	1	8.7E-4			5V
	Xe (LET =63)	1	2.0E5			5 v
	I (LET= 60)	5	2.2E-5	1.1E-5	4.5 E-5	5V
	Br (LET= 3 7)	1	3.0E-7			5V
	Xe (LET= 63)	9	1.5 E-4	1.1E-4	1.9E-4	
	Kr (LET= 40)	2	2.3 E-7	1.8 E-7	2.8 E-7	
	Br (LET=37)	2	6. 0E-7	1.9 E-7	1.0E-6	
Angle:	0 degrees	5	2.2 E-5	1.1E-5	4.5 E-5	5V, LET=60
	45 degrees	1	4.9E-6			5V, LET=60
Lot:	U1H96	1	1.3 E-4			1ET=60
	U1H58	1	1.2E-4			LET=60
	U1H58	1	1.6E-4			
	U1H80	3	1.7E-4	1.5 E-4	1.9 E-4	
	U1H82	2	1.5E-4	1.4 E-4	1.5 E-4	
	U1H83	2	1.4E-4	1.1E-4	1.6 E-4	
Size:	1.0 micron	1	2. 0E-5			5V
	1.0 micron	5	2.2E-5	1.1E-5	4.5 E-5	5V, LET=60
	1.2 micron	1	8.5E-5			5V, LET=60
	1.0 micron	9	1.5E-4	1.1E-4	1.9 E-4	
	1.2 micron	1	1.2E-4			
Bias:	5.5 v	9	1.5 E-4	1.1E-4	1.9 E-4	
	5.0 v	1	2.0E-5			
	4.5V	1	4.0E-7			
	5.0 v	5	2.2 E-5	1.1E-5	4.5 E-5	LET=60
Temperature:	30 degrees	9	1.5E-4	1.1E-4	1.9E-4	
	100 degrees	1	1.4E-4			
Frequency:	2.5 MHz	5	2.2E-5	1.1E-5	4.5 E-5	5V, LET=60
	0.675 Mtk	1	1.8 E-5			5V, LET=60
Pattern:	alternating	5	2.2 E-5	1.1 E-5	4.5E-5	5V, LET=60
	all zeros	1	7.4E-6			5V, LET=60
	ail ones	1	1.6 E-5			5V, LET=60

Except where specifically noted in the "Parameter" or "'Note" columns, the parameters are: Ion=Xe(LET=63), Angle=0 degrees, Lot=various, Size= 1.0 micron, Bias=5.5V, Temperature=30 degrees C., Frequency=2.5MHz, Pattern=alternating.

Note: All LETs are in MeV per mg/cm^2.

Future Experimental Approach

The present approach works reasonably well, taking advantage of the TMR design to maintain functionality even with several ruptured anti fuses However, better statistics and more accuracy in the counts of biased antifuses are desirable goals Onc attempt at achieving those goals using 1280A (1.0 micron) devices turned on the programming pass transistors so that essentially allthe antifuses were biased with an external source applied to the Vpp pin Unfortunately, in this mode, large susceptibilities to latchup and control register upsets interfered, making collection of SEDR data unreliable. (Note that SEL has not been observed during extensive irradiations for the1280A in normal operation, implying that the susceptible area is only used during programming.) Biasing most of the antifuses using the logic modules' outputs by programming a few selected antifuses has proven more successful, yielding results consistent with those already discussed 'J'bough this method requires the use of either the EMMI or current strip chart techniques to count the ruptured sites, it is the preferred choice for future testing.

Conclusions

Of'the parameters investigated, only bias, normal LET, and angle exhibited strong enough effects to be considered significant, given the inherent statistical uncertainties Susceptibility to SEDR increases rapidly with an ion's normally incident LET and with applied voltage. For a given ion and energy, susceptibility falls sharply as incident angle deviates from perpendicular to the silicon surface. Other dependencies, if any, are more subtle

Folding these dependencies into a calculation of the rate of SEDR in the 1 O°A worst case GCR environment yields very low numbers: less than 3×10^{-5} per device-year for 1280s and 7×10^{-6} for 1020s assuming operation at or below 5.5V. Note two additional assumptions that a "real" design has no more than 5 times the average number of biased antifuses relative to the test design and that the heaviest fractions of the GCR environment are known to within a factor of three [6]. Thus, one can conclude that, although the existence of this new heavy ion induced failure mechanism is somewhat disturbing, the increment in mission risk from SEDR is very small. Even the eight month Mars Pathfinder primary mission, a rather extreme case having seventeen 1280s in single-stling mission-critical circuits, has a 99.960/0 chance of not experiencing an SEDR.

These results apply to all feature sizes of all families of currently available, commercial quality Actel devices, consistent with minor differences in the antifuse. Interest in using these FPGAs in radiation environments is quite high. Thus, Phillips Laboratory has commissioned Loral to produce them using their radiation-hardened process. However, SEDR susceptibility would be essentially unchanged unless special steps (such as thickening the antifuse) are taken As a consequence of this work, Loral is evaluating strategies for SEDR hardening.

References

[1] R Katz, R Barto, J). McKerracher, B. Carkhuff, and R Koga, "SEU Hardening of Field Programmable Gate Arrays (FPGAs) for Space Applications and Device Characterization," *IEEE Trans. Nucl. Sci.*, Dec 1994, p. 2179.

[2] R B. Katz, G. M. Swift, and R L Barto, "Anti-fuse/FPGA Reliability in the Heavy Ion Environment," submitted to NSREC 95.

[3] Haskell M. Joseph, "Radiation-Induced Effects on Special Super Large N-Channel Power MOSFETs for Space Applications," *Proc. RADECS 9/.* Sept 1991, p 1 28.

[4] D. K Nichols, J. R Coss, K P. McCarty, "Single Event Gate Rupture in Commercial Power MOSFETs," *Proc. RADECS 93*, Sept. 1993, p. 462.

[5] R B. Katz and G. M. Swift, "An Efficient IDDQ Technique for Counting Multiple Faults," *IEEE Trans. Test A feas.*, 10 be submitted

[6] Martin Ratliff, personal communication.