CHARACTERIZATION AND MODELING OF STRESS IN MULTILAYER MCM-D SUBSTRATES

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ABSTRACT

The application of' fracture mechanics to analyze the crack growth and propagation in thin film-based multichip module (MCM-D) substrates requires a detailed knowledge of the stress distribution within the layers. The MCM-D substrate consists of a multilayer interconnect structure built on the substrate using thin film deposition techniques. A significant level of stress is expected in the sc interconnect structures as a consequence of the mismatch in the coefficients of thermal expansion (CTE) between the substrate and thin film layers (thermal stress) and due to the fabrication and deposition processes (intrinsic stress). The stresses can compromise the reliability of MCMS if they are allowed to drive any of the failure modes.

In this study, thin film layers of silicon dioxide dielectric deposited by plasma enhanced chemical vapor deposition (PECVD), aluminum alloy conductors deposited by sputtering, and anodized aluminum thin film capacitors, all deposited on a silicon wafer, comprise the MCM interconnect structure. The stress in the layers of this structure is measured using the substrate curvature. The radius of curvature of silicon wafers, at different stages of interconnect fabrication, was measured using the x-ray rocking curves technique. The values of the "composite" stress were then deconvolved to yield in-plane stress values in each layer. This method is especially useful in determination of stress in noncrystalline thin films, such as silicon dioxide. The experimental stress values were used to calibrate a finite element analysis of the MCM interconnect structure in order to characterize **the local** stresses that drive flaw propagation.

This paper is part of a study that has been initiated to evaluate and control the failure risk of thin film-based MCMs in order to utilize. this technology in Mars exploration missions or in other extreme temperature environments.

INTRODUCTION

The thin film multilayer structures used in multichip module substrates in high density electronic packaging are subject to failure due to thermally induced stress cycling. These thin film structures consist of layers of interconnections, dielectrics and vias deposited and patterned using a variety of thin film techniques, Aluminum or copper are often used for interconnections and silicon dioxide or polymers for dielectric layers. The whole structure can be deposited on ceramic substrates, such as alumina or aluminum nitride or on silicon wafers. In this paper, the stress slate of thin film layers in a MCM substrate with aluminum conductor skips, embedded in a silicon dioxide matrix supported on a single crystal silicon substrate, is considered. This thin film structure is illustrated in Figure 1. Typical dimensions of the aluminum interconnections are 2 μm thickness and 10 μm width and the thickness of the silicon dioxide layers vary from 1 to 7 pm.

The aluminum interconnect strips and vias in the thin film structure exist at an elevated stress state that is in part induced by the manufacturing process and is in part due to the surface effects associated with thin films. Significant stress cycling can cause the propagation of flaws or defects induced during manufacturing of the multilayer structure. The propagation or growth of flaws in the interconnects and vias can be modeled and predicted only if the stress during thermal cycling is accurately characterized.
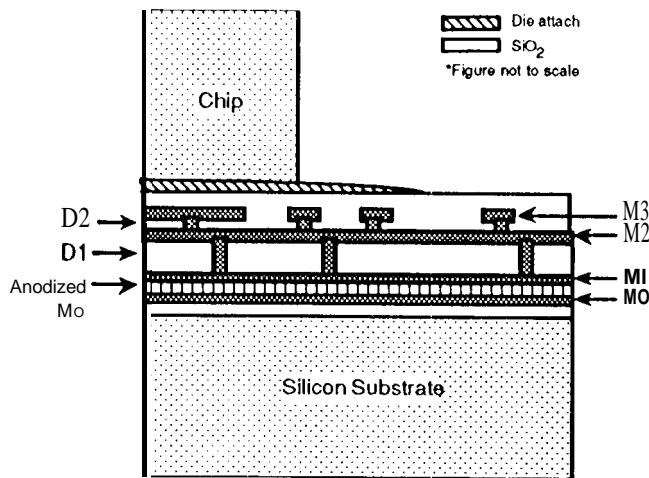
FIGURE 1 SCHEME OF THE MCM-D MULTILAYER
INTERCONNECTION SUBSTRATE

The average stress at room temperature of each of the layers of the multilayer thin film structure is determined by measuring the radius of curvature of the silicon substrate. Substrate samples were available at different steps in the manufacturing process as the multilayer tack was built up. The technique used to measure radius of curvature is described in a following section of this paper. The average stress in different layers of the substrate was calculated using the Stoney equation (Stoney, 1909). The average stress in a layer and the corresponding radius of curvature were then used to calibrate a finite element model of the multilayer structure. The calibrated finite element model can then determine stress at specific locations in the aluminum interconnect strips.

With stress determined, a flaw propagation analysis to predict fatigue life of the interconnect strips and vias can be performed. The flaw propagation analysis must also include

information about thin film fracture properties and about flaws or defects in the multilayer structure. Because the information needed to perform the fatigue analysis is incomplete and uncertain, the probabilistic physics of failure approach described by Moore, et al. (1993) and shown in Figure 2. is being used. This probabilistic approach enables sensitivity analysis to be performed to identify information acquisition activities most needed to improve failure prediction accuracy.

In the following sections of this paper, the methods and results of the experimental stress determination are presented, the finite, element model is described, and preliminary results are given. In future papers, the flaw propagation analysis and probabilistic fatigue life prediction of the multistack layers will be presented.

MCM SUBSTRATE DESCRIPTION

The multichip module substrates used in this study were manufactured by the n-CHIP company (Figure 1). In order to obtain samples at each major step of the manufacturing process, wafers were pulled out at each major manufacturing step from a main batch in the production line. The samples and their abbreviations used throughout the paper are described below:

The first sample, Metal O, consists of 0.8 μm of thermally grown silicon dioxide and 1 pm of aluminum deposited by sputtering at room temperature. The aluminum layer was anodized to form 2000 Å of aluminum oxide for an interlayer capacitor (Anodization). The. 1 pm aluminum layer was then deposited on top of the anodized layer by sputtering at room temperature. Next, a 7 pm thick layer of silicon dioxide was fabricated using PECVD process at 400°C and vias patterned (Dielectric 1). Metal 2 was deposited on top of the silicon dioxide and consists of a 2 μm thick layer of Al-1% Si deposited by sputtering at 350°C . The Dielectric 2 layer is 4.5 pm thick, deposited at the same conditions as Dielectric 1. The Metal 3 sample was fabricated by adding 2 μm of
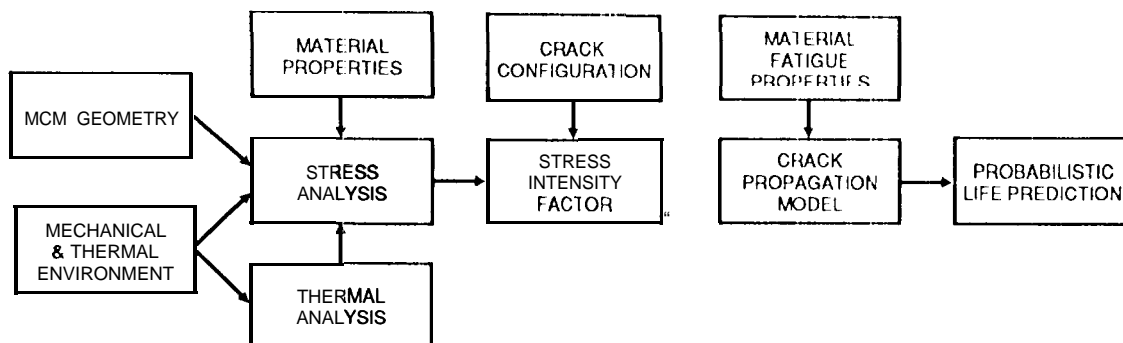

FIGURE 2 THE PROBABILISTIC PHYSICS OF FAILURE APPROACH IN APPLICATION TO MCM TECHNOLOGY
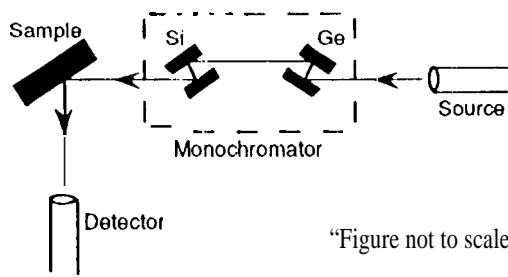
FIGURE 3 X-RAY ROCKING CURVE EQUIPMENT SCHEME

Al-1 % Si layer using the same deposition condition as Metal 2. The Completed Wafer was obtained by depositing of 3.75 μm of silicon dioxide and a 0.25 μm silicon nitride passivation layer.

X-RAY ROCKING CURVES ANALYSIS

Stress in a film deposited on a crystalline substrate causes bending of the substrate in the plane of the film. The bending may be related to the average stresses in the plane of the film and the elastic properties of the sample. The radius of curvature of the bent crystal can be measured using an x-ray rocking curves (curves of diffracted intensity vs. angle) method. The x-my rocking system configuration is shown in Figure 3. The x-ray source used for this experiment consisted of a sealed x-ray tube with a Cu target. In order to obtain sharp diffraction peaks necessary for high angular resolution, the combination of Ge and Si channel-cut crystals were used as a double monochromator. A NaI scintillation detector with photomultiplier was used as the x-ray detector. The sample goniometer has three motor driven axes of rotation and two of translation, capable of angular adjustments of the sample with a step size of about 10^{-4} degrees. The translation stage allowed measurement of a crystalline substrate diffraction peak at different lateral positions of the sample. The radius of curvature of the substrate in the diffraction plane can then be determined from the peak shifts using Equation (1):

$$R = s / \theta \qquad (1)$$

where s = scan length and θ = angular shift of the substrate diffraction peak. The average stress in polycrystalline or noncrystalline films deposited on a crystalline substrate can then be calculated from the radius of curvature and elastic data of the substrate using the Stoney equation. The Stoney equation is a special case of the Timoshenko bimaterial strip equation (Timoshenko, 1925) for a thin film on a relatively thick substrate base.

TABLE 1 RADII AND STRESSES FROM X-RAY MEASUREMENTS

Sample (1)	Total Multilayer Thickness [μm] (2)	Radius of Curvature [m] (3)	Top Layer Stresses [M Pa] (4)	Average Stress of Multilayers [M Pa] (5)
Metal 0	1.8	64	52	69
Anodization	1.8	63	78	70
Metal 1	2.8	-210	-165	-14
Dielectric 1	9.8	-23	-43	-35
Metal 2	11.8	-18	-53	-38
Dielectric 2	16.3	-17	-9	-30
Metal 3	18.8	-14	-30	-30
Completed Wafer	22.3	-36	82	-10

Table 1 shows the results of radius of curvature measurements using the x-ray rocking curves technique. The radii of curvature given in Table. 1 are due to the stresses of all the films on the substrate at a certain level of the manufacturing process. The average stress of the multilayer in the table is calculated using the Stoney equation, with total thickness of all the layers present on the wafer. The average stress up to the anodization layer is tensile and it remains compressive for the rest of the processing, as well as, in the completed wafer.

The stress in a thin layer is nearly uniform through the thickness and most of it is through axial loading and hence will scale as the layer thickness changes. This enables the stresses in the individual thin film layers to be deconvolved using

$$S_n = (s_1 h_1 + s_2 h_2 + s_3 h_3 + \ldots + s_n h_n) / H_n \qquad (2)$$

where S_n = average stress of the thin film stack with n layers, h_1, h_2 = thickness of individual layer in the stack, s_1, S_2 = stress of individual layers in the stack, and H_n = total thickness of the thin film stack (i.e., $h_1 + h_2 + h_3 + \ldots + h_n$). This equation can be written in terms of the average stress for the $(n-1)$ layers as follows:

$$S_n = (S_{n-1} H_{n-1} + s_n h_n) / H_n \qquad (3)$$

The stresses in the top layer s_n given in column (4) of Table 1 are obtained from the average stress S_n of the n layered sample and average stress S_{n-1} for the $n-1$ layered sample using Equation 3.

Since the stresses in the layers change minimally we can use the average stress in the layers from the previous sample to estimate stress in the top layer of the next progressive sample. This assumption of previous layer stresses remaining unchanged at each stage of manufacturing was checked

TABLE2 RADII AND STRESSES FROM FE ANALYSES

Sample (1)	Radius of Curvature [m]		Iop Layer Stress [MPa]			Reference Temperature T, [°C]
	Measured (2)	FE Thermal (3)	Total (4)	Thermal (5)	Intrinsic (6)	Specified (7)
Metal 0	64	−205	87	0	87	20
Anodization	63	−205	87	0	87	20
Metal 1	-210	-54	−146	+	−146	20
Dielectric 1	-23	-84	−35	18	-53	400
Metal 2	-18	· 5	−49	815	-864	350
Dielectric 2	-17	24	-10"	20	-30	400
Metal 3	-14	- 6	−36	816	-852	350
Completed Wafer	−36	17	74	20	53.0	400

by **substituting all of the top layer** stresses from Table 1 in Equation 2 for the completed wafer and comparing the resulting average stress value to the average stress for the completed wafer sample calculated based on the Stoney equation. The top layer stresses in the Metal O layer and in the anodized aluminum are tensile but they are compressive for the rest of the layers, except in the final passivation, where it is tensile.

The stress of thermally grown films on top of the wafer silicon dioxide was obtained by measuring the curvature of the silicon wafer after selective etching of the aluminum layer (Metal O). The stress for this layer is 156 MPa.

FINITE ELEMENT STRESS ANALYSIS

The finite element (FE) method has been used to determine the stresses in the thin film layers of high density electronic packaging during manufacture and when subjected to thermal or mechanical loads. To accurately predict stresses, the FE analysis should follow through the steps of the manufacturing process to account for material nonlinearity and change in geometry from adding or deleting (e.g., etching) of layers. Using a method recommended by Cifuentes and Shareef (1 992), a single FE model that uses artificial nodes to model material interfaces was developed to analyze the structure through its complete set of manufacturing steps. The depositing of layers (bonding) or etching (debonding) is done by a series of multi-point constraints that uses the artificial nodes and the boundary nodes for each layer. The results of a linear elastic analysis of this FE model is presented here to illustrate a technique for calibrating this model using radius measurements 10 account for intrinsic stresses in the thin films that result from manufacturing. The FE analysis procedure used alone can only account for the thermally induced stresses from thermal expansion of the material due to a change in temperature of the layer and due to the difference in the coefficient of thermal expansion between the different layer materials. It cannot explicitly account for the intrinsic stresses that are developed in these layers during deposition.

Since the direct measurement of the stresses in thin films is impractical, the residual stress state after manufacturing of the wafer was established by calibrating the FE model using experimental radii measurements of sample wafers that were pulled out at different steps during its manufacture. The total stresses in these layers at each stage of the manufacture were implicitly obtained by measuring the radius of curvature of the sample and matching the radii in the FE model for each **sample. The radii in the. FE model were matched** in the following manner:

(1) analyze each sample with the reference temperature T_r of the new layer set to the specified deposition temperature for that layer (e.g., column (7) Table 2) and calculate the radius of the wafer using the nodal displacements in the FE model,

(2) adjust the T_r for this layer by iteration until the radii predicted by the FE model matches the radii measured for this wafer.

(3) repeat the same for the next wafer in the manufacturing step and iterate to estimate the T_r for the newly added layer while maintaining t he T_r for the earlier (step) layers at their final values.

The MSC/Nastran for Windows (1994) was used to perform the FE analysis. The FE mode.1 that was used had 2D plane strain elements and represented 100 μm width of the sample along the. radius measurement direction and is shown in Figure 4. The model consisted of 560 quadrilateral and triangular elements and the mesh density
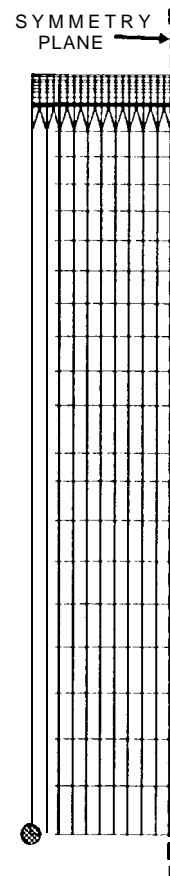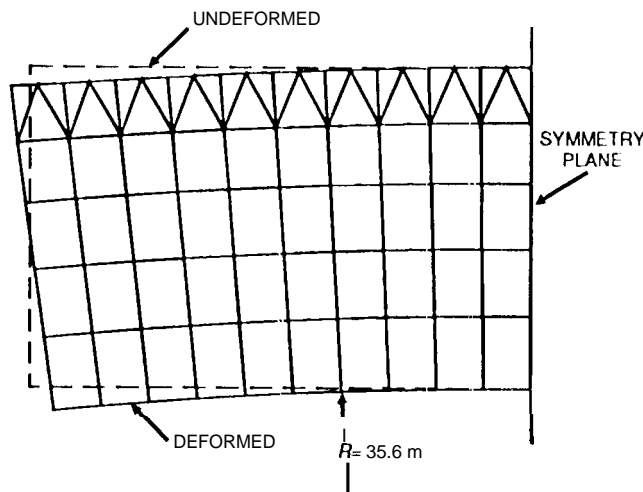
SYMMETRY
PLANE

FIGURE 4 FE MODEL

FIGURE 5 **DEFORMED SHAPE OF THE Si BASE** FROM FE ANALYSIS FOR THE COM-PLETED WAFER

was coarse at the Si base and it was transitioned to a fine mesh for the thin layers at the top to maintain acceptable element aspect ratios. A symmetry boundary condition was imposed along one edge of the FE model and a "plane-sec-tion" condition was assigned via multi-point constraints along the other edge. The latter constraint is reasonable for a segment in the middle of a sample and for the types of thermal loadings that were considered here.

DISCUSSION

The results of the FE analysis are presented in Table 2. Column 2 in the table gives the radii of curvature for different samples as measured by x-ray analysis (same as column 3 of **Table 1).** Figure 5 gives the deformed shape of the silicon base at a 35.6 m radius for the completed wafer, The radii of curvature obtained from the FE analysis, assuming only thermal stress, are listed in column 3. Column 4 shows the stress values of the top layer in each multilayer sample calculated using FE analyses whose radii were calibrated by adjusting T_r to give the experimental radii of curvature. The thermal (extrinsic) and intrinsic parts of the total stress for each layer are presented in **columns 5 and 6,** respectively. The processing temperatures used in the FE analysis to calculate thermal stress given in column 5 are listed in **c o l u m n   7** .

By comparing **columns** 4 in both Tables 1 and 2, it can be concluded that FE model predictions of the total stress agree very well with stress values obtained from the Stoney equa-tion and experimental radii of curvature. Furthermore, the top layer stresses from the FE models for different samples **given in column** 4 of Table 2 closely matches the stresses in **each layer from the completed wafer** FE model in Table 3 in

TABLE 3 RADII AND STRESSES FROM THERMAL EXCURSION

	20'C (RT)	100"C	-50'C
Radius [m]	35.6	5.3	-17.3
Stress [MPa]:			
Si Base	-1.0	-59	34
0.8 µm Si₃N₄ SiO₂	39	36	41
Metal 0	87	-232	**259**
Anodized M0	88	-232	259
Metal 11	-146	**-465**	26
7 µm SiO₂	-35	**-38**	-33
Metal 2	-49	-368	123
4 µm SiO₂	-10	-13	-9
Metal 3	-37	-356	1 335
3.75 SiO₂ & SiN	73	70	7 5

the column labeled 20°C. Hence this again confirms the assumption about the stresses in thin film layers.

Thus the FE **model has** been calibrated to include both the intrinsic and thermal stress contributions to the total stress for these MCM **substrates and perhaps** for others that use the same manufacturing steps. This work also shows that the intrinsic contribution to the total stress is large and cannot be ignored in the FE analysis. Consequently this FE model and subsequent detailed three-dimensional FE models will be used to calculate the local stresses in the multilayer structures to enable crack propagation analysis at its critical failure locations.

THERMAL LOAD ANALYSIS

Having established the residual stress state of the MCM, the completed wafer was subjected to a thermal cycle analysis. That is, a linear elastic FE analysis was performed by subjecting the **entire** MCM structure to a thermal load excursion. The results for the extremes of a 100°C to -50°C thermal load excursion are presented along with the residual stresses at room temperature (RT) in Table 3, which gives the maximum stresses in each layer and the final radii. The stress range from such a stress cycle will be used to perform a probabilistic crack growth analysis due to thermal cyclic loads in the next phase of this study.

SUMMARY

The **combination of** experimental stress **characterization and finite** element modeling permits the stress at specific locations within thin film multilayer structures to be deter-mined. With local stress known, a fracture mechanics analysis can be performed probabilistically to evaluate fatigue **life of such structures.**

The experimentally determined average stress in individual layers of a thin **film multilayer structure has been** used to calibrate a finite element model. This finite element

model can calculate the local stress at specific features within an individual thin film layer. This capability 10 determine stress at specific locations within individual thin film layers is to be used in a fracture mechanics analysis to evaluate fatigue life of multilayer structures subjected to thermal cycling.

ACKNOWLEDGEMENTS

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