Compact Multimedia Systems in Multi-chip Module Technology

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Abstract

This tutorial paper shows advanced multimedia system designs based on multi-chip module (MCM) technologies that provide essential computing, compression, communication, and storage capabilities for various large scale information highway applications. Section two presents the system configurations and the hardware architecture of an advanced multimedia system that offers the telecommuters and home office users with a powerful computing/communication infrastructure. Section three presents state-of-the-art MCM technologies that play a critical role in meeting these challenges for creating smaller and faster multimedia systems with better video, graphics, computing, storage, and networks. Section four reports a three-dimensional mu] ti-chip module design for advanced multimedia-intensive telecommunication applications.

1. Introduction

A multimedia system is characterized by the computer-based integrated generation, manipulation, presentation, storage, and communication ı of independent digital information which is most often coded in continuous-time dependent-media (e.g., video, audio) and discrete-time independent-media (e.g., text, graphics) [1 ,2]. The key defining characteristics of the information superhighway are: (1) easy access to network intelligence to serve multitudes of end-user demands; (2) fully open network and access solutions to communicate in any desired form including point-to-point, multipoint and broadcast; (3) to all types of information service providers globally; (4) seamless interoperability across applications, communication services, media and hardware plus software platforms; (5) scalable application dependent features and technical characteristics of platforms and network resources under end-user control [3]. Rapid advancements in microelectronics, signal processing, computing, telecommunication and mass production of highly complex computing and communication oriented devices have established unique opportunities for creating advanced multimedia-intensive telecommunication applications for the era of information superhighway, The need for a smaller and faster multimedia system with better video, graphics, computing, and networks will continue to grow. By the turn of the century, the multimedia PCs of today will evolve into a portable/nctworkable advanced multimedia computer which typically provides 1 GIPS,16MB cache, 2 GB system memory, 1 gega-bit-per-second networking bandwidth and offers the telecommuters and home office users with a powerful computing/communication infrastructure [4]. Submicron technologies and VLSI integration will play a critical role in meeting these challenges.

This tutorial paper shows advanced multimedia system designs based on multi-chip module (M CM) technologies that provide essential computing, compression, communication, and storage capabilities for various large scale information highway applications. Section two presents multi-chip module technologies that provide effective VLSI integration of computing, multimedia processing, storage, and communication subsystems for the creation of new advanced multimedia systems. Section three describes

multi-chip module technologies and VLSI integration that are critical to create the proposed multimedia systems, Section four reports a three-dimensional multi-chip module design for advanced multimedia-intensive telecommunication applications.

2. Advanced Multimedia Systems

This section presents the system configurations and the architecture of advanced multimedia systems that are driven by the interface, storage, processing, compression, and communication requirements targeted for information highway applications planned for the late 1990s and 2000s.

An advanced multimedia system for distributed multimedia applications consists four subsystems: processor , storage, multimedia payload, and communication subsystems as shown in Fig. 1. The architecture design involves the specification of these basic building blocks and the determination of the way they are interconnected, The basic subsystems are described as follows:

2.1. Processor Subsystem

In an advanced multimedia system, the processor subsystem executes a multi-tasking operating system and performs many task such as interactive multimedia tasks. A processor subsystem usually includes a RISC CPU, a memory management unit, a cache memory, a secondary cache memory, and a system memory.

A Pentium-based CPU MCM was reported in the 1995 MCM Conference. The CPU MCM contains a Pentium CPU chip, a cache controller chip, 512K-byte secondary cache memory, and 18 SRAM chips. The interconnect substrate for the MCM is fabricated on an Aluminum wafer which serves as a ground plane. Layers of polyimide and copper are deposited on the substrate to make one power plane, two interconnect layers, and one surface bounding and die attach layer. The 3.68cmx7.52cm substrate is mounted in a 349-pin Grid Array (PGA) package having 0.1 inch pin pitch. The high performance of this 66-MHz system is achieved by isolating the critical address, data, and control signals associated with the second level cache so that they remain in the superior environment of the MCM.

2.2. Storage Subsystem

The storage subsystem for continuous media requires large volume, low latency, and high data transfer bandwidth. A storage subsystem includes a local storage controller, a cache memory, a mass storage memory, and a direct memory access. The local storage controller is used to relieves the CPU of time-consuming storage management task. The cache memory can be configured as a video data buffer thus freeing system memory. The data transfer between the storage subsystem and system memory is carried out using DMA to relieves the CPU of word-by-word data transfers.

Three-dimensional (3-D) packaging technology provides memory density improvements that are more than an order of magnetite more dense than competitive planar packaging techniques. The 3-D memory stacking techniques become more cost effective in quantity and broaden the range of applications. By using commercial available **64** Mbit DRAM dies, a 2 Gbit mass memory is accommodate.d by a single 1" x 1" MCM. As densities and performance increase, and prices drop below the cost of DRAM, flash memory may become an integral part of adwmced multimedia systems. In 1993, a 256-Mbyte 68-pin PCMCIA memory card was implemented using 8-layer short stacks in a credit card-size form factor (about 3.366" x 2.126"). Flash memory may be cost less than $5 per megabyte by 1988. Today, an 8-MB hard-disk drive in PCMCIA form factor is

available for approximately $500. Rotating media based storage subsystem such as hard disk may be replaced with solid-state disk based on high-density flash memory.

2.3. Multimedia Subsystem

The multimedia subsystem is a programmable parallel computing and multiple 1/0s platform to support various real-time multimedia computing tasks for multimedia instruments. The various tasks include video processing, 2D and 3D graphics generation, audio signal processing, compression and decompression, full-motion video capture and display, and graphical user interface. The video 1/0 block is able to capture, process, compress, store, decompress, and display full-motion video in real time. The audio 1/0 block is capable of capturing, processing, compression, and playing quality audio in real time. The Texas Instruments introduced the Multimedia Video Processor (MVP) in 1994. The MVP is a programmable parallel processor that can perform more than two billion operations per second. It includes four parallel processing, 32-bit DSPs combined with an integrated RISC CPU and floating point unit, a transfer controller and video controllers with shared access to on-chip SRAM via a crossbar.

2.4. Communication Subsystem

The multimedia communication subsystem should support high-speed networking and wireless communication. Deployment of B-ISDN, ATM, or SONET provides the necessary high-speed network for the seamless multimedia data at adequate data rate, The ATM transmission of continuous multimedia stream is becoming popular for the high-speed public network telecommunication services. The ATM networks generally provide high-speed transmission with SONET OC-3 at 155 Mbps and DS-3 at 45 Mbps. The ATM switching technology will form the next generation of broadband communication network [8]. A RF Modem MCM provides wireless communication capabilities with data rates in access of megabits/second at carriers in the low GHz range [9]. Yamada et al have also developed an 8x8 ATM switch module with clock speed of 622 Mb/s and power consumption of 60 watts by using MCM-C technology with low temperature co-fired ceramic 86 mm x 86 mm substrates and surface mounting technology [12].

2.5. Host Bus and Media Bus

The host bus for continuous multimedia requires low latency, and high data transfer bandwidth, All data transfer from storage subsystem to the video and graphics subsystems take place over the host bus. For example, the digital video playback (640x480RGB 16 @30fps) requires 18 MB/see decompressed data rate and 1.2 MB/sec compressed data rate. The VESA Local Bus is based on the Intel 486 and is typically synchronous to the 32-bit processor. The VESA Local Bus 2.0 provides support for up to 64-bit processor running up to 66 MHz. The Peripheral Component Interconnect bus (PCI) is processor independent and supports for both 32 and 64-bit wide data buses operated at 33 MHz.

A standardized multimedia interface between multimedia payloads and devices is required to transfer many compressed/uncompressed multimedia steams. For example, the VESA Media Channel (VM-Channel) is a recently introduced standard allow the interconnection of a wide range of multimedia payloads **[5].** Integrated video and graphics subsystem is desired for a multimedia system [6] . The VESA Advanced Feature Connector (VAFC) has been proposed by VESA [7], which allows high bandwidth data exchange between the video and graphics subsystem with a throughput of up to 150 megabytes/scc.

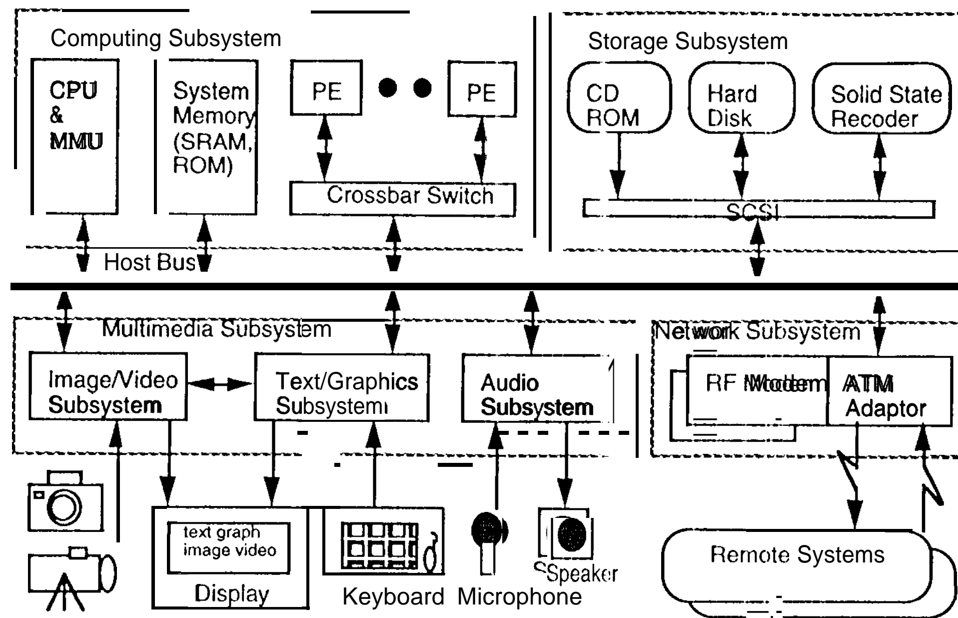

Figure 1. Functional block diagram of an advanced multimedia system.

3. Multi-chip Module Technologies: An Overview

This section introduces fundamentals of MCM technologies. Advanced 3-D MCM technologies are also introduced.

3.1. Introduction

Conventional microelectronic packaging technology packs bare dies into single-chip packages (SCPs) and then mounts these SCPs onto printed-circuit boards (PCBs). The ratio of the total area occupied by silicon to the total board area is typically around 5% for traditional through-hole and surface mount technologies. The conventional SCP-on-PCB packing results in inefficiency in packaging density, speed, size, weight, power consumption and reliability. In recent years, conventional packaging has not been able to keep pace with the advances in the performance and density of integrated circuits for the most demanding applications (e.g. portable computing, multimedia computing, high-speed networking, etc.). The microelectronics packaging industry has been looking to multi-chip modules (MCMs) as a possible solution to conventional package bottleneck.

The basic idea of the MCM is to eliminate the SCP and interconnect several bare dies directly onto one package. Recently, multi-chip modules have been demonstrated to achieve higher densities and improved performance. The state-of-the-art MCMS are high-performance high-density hybrid circuits in which a variety of bare dies are interconnected on a substrate whose multilayer structures combine low-dielectric-constant interlayer dielectric with very fine line interconnection features. MCMS arc capable of producing high-speed circuits and achieve weight and volume reductions over ten-fold better than PCBs. MCMS are being used in diverse applications for military, space, medical, commercial, and consumer products.

3.2. MCM Technologies

There are three major types of multi-chip modules: MCM-D deposited thin film, MCM-C cofired ceramic, and MCM-L plastic laminate.

MCM-D deposited thin film: Deposited thin-film MCMS consist of alternate thin-film dielectric and metalization layers deposited on a silicon, ceramic or aluminum substrate. The metalization is usually aluminum or copper, while the dielectric layers include polyimide and silicon dioxide.

MCM-C cofired ceramic: The MCM-C substrate is a multilayer ceramic substrate which are constructed using layers of a mixture of ceramic and glass power. These layers are customized by punching hole for the vias and forming wiring patterns using molybdenum paste. The layers are then stacked together and baked to obtain a multilayer aluminum substrate. Dies are bounded to the top layer of the substrate, typically using flip-chip bounding,

MCM-L plastic laminate: The MCM-L substrate consists of a copper lead frame sandwiched in a copper/BT resin multilayer structure. Opening in the multilayer structure allow die attach to the copper lead frame. MCM-L substrates can provide line widths and spacing as fine as 75 microns.

MCM-D is generally recognized as the highest performance among the three major MCM technologies. The routing density possible with thin-film material makes MCM-D the winning option for many applications. High density MCM-D substrate can support substrate wire bond pads on a tight pitch, while MCM-L substrates with their relatively large vias require careful bound pad fanout design. However, MCM-L is the most cost-effective approach for low-end applications due to the current infrastructure. MCM-C is frequently seen as falling in the middle in density, performance, and cost. The advantages of the MCM-C include the excellent dimensional stability and mechanical properties of ceramics, which lead to high reliability and module power (dissipation capability. The maturity of this MCM-C technology also allows it to be competitive in cost. The disadvantage of the MCM-C is that many wiring layers may be required for a complex design due to the relatively low wring density achievable for each interconnect wiring layer. To address the broad spectrum of industrial applications and cost-performance target, it is believed MCM-D, MCM-C, and MCM-L technologies will be all required either as separate or hybrid technologies. Potentially, the best performance/cost balance may come from combination of these different approaches.

3.3. 3-D MCM Technologies

Three-dimensional MCM technology has been pursued as a possible means of achieving very high performance and compact systems. The PCB approach involves connecting MCMS to PCB holders which are in turn stacked on top of one another using flexible elastomeric material for electrical interconnections. The AIN approach employs hermetic AIN carriers for the MCMS which are stacked together with metalized AIN spacers and solder bumps for electrical connections. The GE HDI approach involves bonding GE HDI MCMS together in a stack with interconnections provided by another HDI overlay applied to the sides of the stack.

4. Three-Dimensional MCM for Advanced Multimedia Systems

The design of low mass, volume, and power multi-chip module computer demonstrated in the NASA Advanced Flight Computing (AFC) program [10] is applicable to the growing commercial multimedia industry. The goal of the AFC program is to designed and implement a core avionics open architecture which consists 'a 3D stack of MCM modules. This 3-D MCM architecture can also used for advanced multimedia systems. Three distinct 3-D MCM approaches has been shown useful for the AFC program [11].

4.1. 3-D MCM Architecture

The key to attaining a compact advanced multimedia system will be the utilization of advanced electronic packaging and VLSI technologies, including multi-chip module (MCM) technology, three-dimensional MCM stacking, and die stacking for memory, These technologies will be used to create MCMS containing the major electronics components of an advanced multimedia system. These MCMS will then be integrated into a single three-dimensional assembly or stack. An illustration of this concept is given in Figure 2.

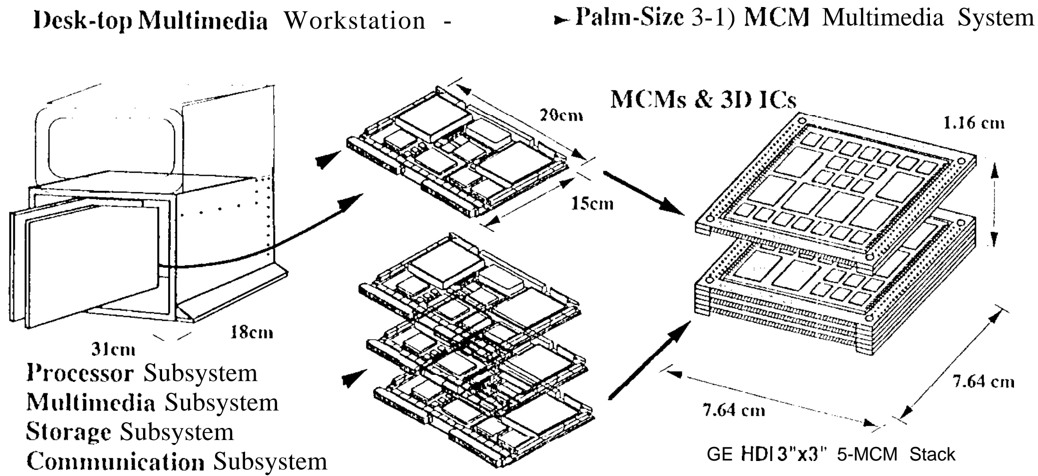

Figure 2. Three-dimensional MCM microelectronics assembly concept for advanced multimedia systems.

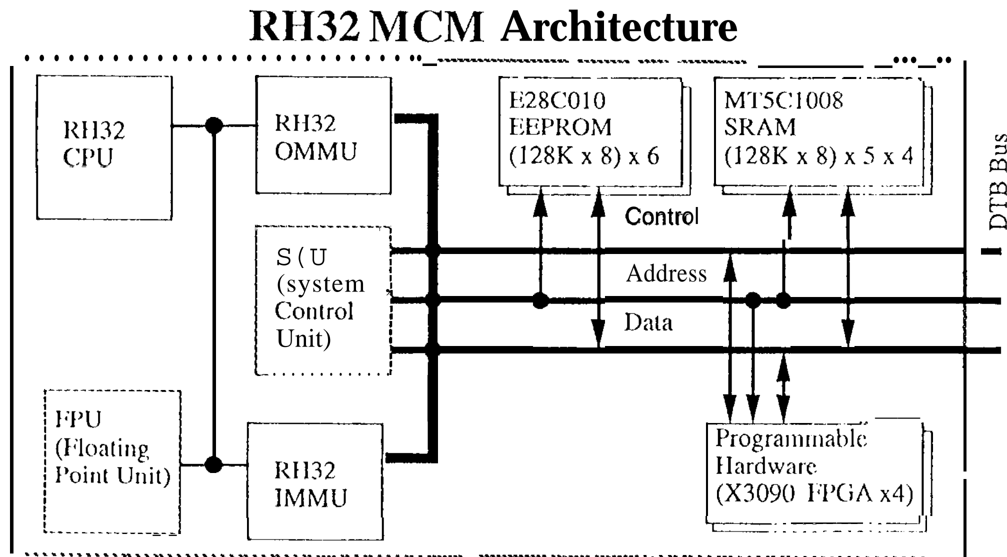

Figure 3. System block diagram of the RH32-based flight computer MCM.

4.2. Design and Implementation of the Computer MCM

The flight computer MCM is one of the most advanced computer with MCM technology developed for NASA's future small and microspacecraft missions by the Jet Propulsion Lab, which worked in conjunction with nCHIP Inc. (San Jose, Calif.) and TRW. This flight computer MCM contains 33 dies in a single 2 by 4 inch 442-pin AIN package from Coors. This MCM also uses nCHIP's 3-D die stack for both SRAM and EEPROM. The architecture of the processor MCM is shown in Figure 3. The dice that were used on the MCM includes: one TRW 32-bit RISC processor, one TRW operand MMU (memory management unit), one TRW Instruction MMU, twenty Micron 128x8 SRAMS, six Atmel 128x8 EEPROMS, and four Xlinx XC3090 FPGAs. All dice in the MCM are wire bonded to the silicon substrate by using the nCHIP MCM-D technology, A graphical representation of the AFC flight computer MCM is shown in Figure 4, and the actual layout is shown in Figure 5.

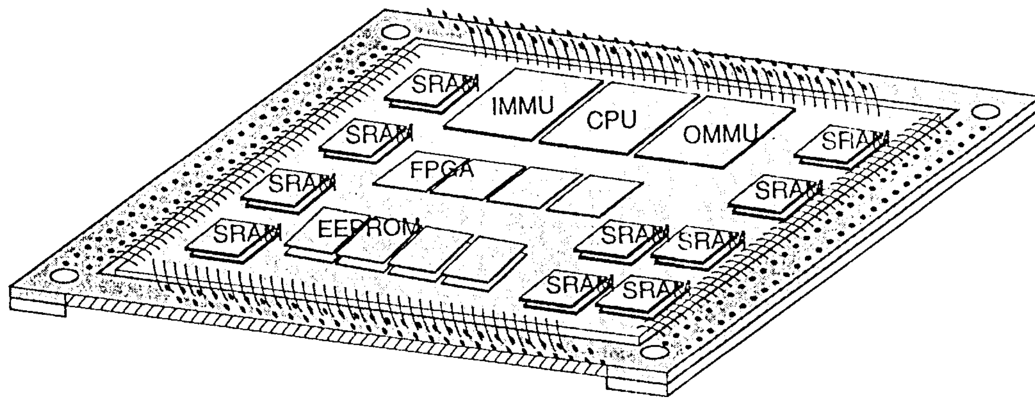

Figure 4. Flight computer MCM layout.

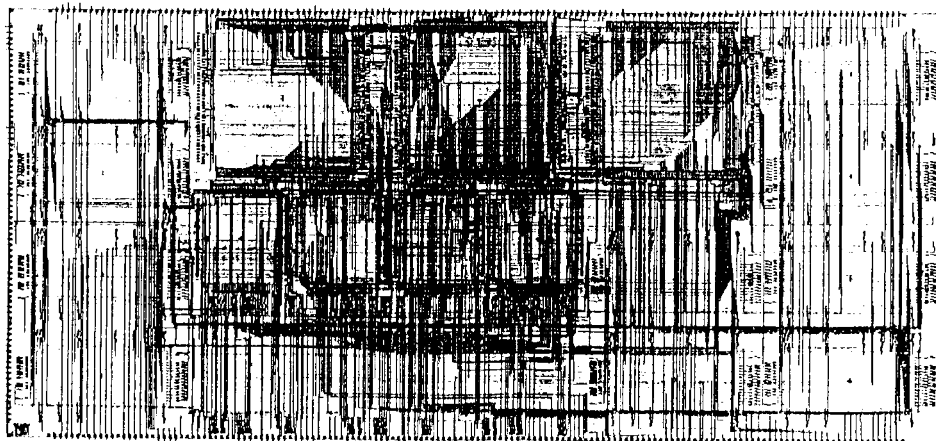

Figure 5. Actual flight computer MCM layout and routing using nCHIP MCM-D technology.