

Sandbox CCDs

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ABSTRACT

Seven new CCDs are presented. The devices will be used in a variety of applications ranging from generating color cinema movies to adaptive optics camera systems to compensate for atmospheric turbulence at major astronomical observatories. This paper highlights areas of design, fabrication, and operation techniques to achieve state-of-the-art performance. We discuss current limitations of CCD technology for several key parameters.

Keywords: Charge-coupled devices, solid state imagers, charge transfer efficiency, dynamic range, quantum efficiency, dark current, well capacity, read noise, x-ray, ultra-violet, high speed readout.

1. INTRODUCTION

CCD technology, now celebrating its twenty-fifth birthday, has matured to a remarkable degree. Through much of the 1970s, CCD fabrication was beset by countless difficulties, including contamination, variable and incompletely understood processing steps, rudimentary design tools, deficient modeling of device performance and absolute characterization testing techniques. As a consequence, a great deal of trial and error was involved. Technological progress took place despite these instabilities and unknowns but the price was high. As an example, two early JPL CCD programs, the Galileo Orbiter Solid State Imager and the initial Hubble Space Telescope Wide Field/Planetary Camera (WF/PC) entailed a total of approximately 150 production lots to develop and produce suitable CCDs.

In contrast, today it is not uncommon for a new custom CCD to be successfully produced on the first attempt. This maturation has enabled the production of CCDs at prices that are more widely affordable and has spawned an explosion in CCD applications. Some new applications include HDTV cameras, consumer electronics (e.g., camcorders), biological x-ray microscopes, medical x-ray cameras (e.g., spot mammography), dental x-ray cameras, document and graphic archiving scanners, ultra-large format astronomical imaging and spectroscopy cameras, modest-format amateur astronomy cameras, space-borne imaging camera systems, 35 mm still and motion picture cameras, industrial robotic cameras and PC cameras and scanners.

Indicators of this maturity are numerous:

- 1) Charge transfer efficiency (0.9999995 for a $1620 e^-$ signal) and production yield have progressed to the point where CCDs having 10^8 pixels are being planned. Device shorts have been reduced where it is now feasible to build wafer-scale arrays. The largest CCD (in pixel count) that could be theoretically fabricated today is a $16k \times 21k$, 5-micron pixel CCD (fabricated on a six-inch wafer).

- 2). Readout noise is as low as 2-3 e⁻ (rms) for conventional on-chip amplifiers. Values well below one e⁻ are achieved with floating gate amplifiers. Well capacity has been improved almost a factor of ten compared to CCDs fabricated 15 years ago. Dynamic range for some CCDs today is > 10⁶.
- 3). The quantum efficiency (QE) of these devices is remarkably high (> 0.5) over unprecedented range of wavelengths, approximately 1-10,000 Å. One can now routinely obtain thinned, back illuminated devices with QE's in excess of 70-90 % from 380 to >700 nm. New anti-reflection (AR) coatings are being developed to extend the useful response of the CCD well into the UV. One such coating will yield 50 % at 300 nm and > 20 % at 200 nm. Phosphor coatings applied directly to the CCD extend sensitivity into the hard x-ray regime (0.1-1 Å) further exceeding its useful range.

In view of this maturity, it is perhaps surprising to note the many areas in which CCD technology opportunities remain. For example, it appears that the potential for high speed CCD (>10⁹ pixels/sec) remains largely untapped. This delay in large part can be attributed to the lack of availability of high speed computers with lots of memory and relatively easy-to-use image processing software packages. Today CCD groups are designing 1024 x 1024 sensors that readout at 1000 frames/sec (over a billion pixels/sec). Similarly, the maximization of dynamic range for small pixels (< 10 microns) appear to be far from complete.

The authors represent three organizations that have participated in aggressively pushing the limits of CCD technology. Through several recent CCD development programs, we have developed a set of design and production techniques that reliably produces CCDs of high scientific performance. These programs include: the Cassini cameras that are to be launched towards Saturn in 1998, the replacement Hubble Space Telescope that was installed on-orbit in December 1993, the Multi-angle Imaging Spectro Radiometer (MISR) that is to be launched as part of NASA's Earth Observing System, an astronomical x-ray camera that is to study the distant x-ray background radiation, a high speed 1024 x 512 camera that records fluid dynamical phenomena by recording two images separated in time by only 200 ns with read noise <5 e⁻, and a high speed/low noise CCD used in adaptive optics systems. All of these CCDs share common design and fabrication characteristics. Collectively, these characteristics represent an excellent baseline from which to investigate additional technology problems and develop additional custom CCDs.

The "Sandbox lot" is an effort to capitalize upon this technology maturity to reduce the cost of CCD development and production. In doing so, our approach enables the development of custom CCDs whose cost would formerly have been unaffordable and also research of important CCD issues (such as dynamic range optimization) at greatly reduced cost. These savings are realized by combining several devices on a single development lot, thus filling, the production costs among several customers.

This paper consists of two major sections. The first section describes seven specific CCDs that are being developed in this manner. The second section discusses the performance, design and production issues that are involved in developing these seven devices. Many of the designs incorporate features that further push the limits of CCD technology. Key areas that are discussed include: dark current generation, charge transfer, well capacity, high speed readout, QE, read noise, and high energy radiation tolerance.

The first six Sandbox CCDs listed above will be fabricated in one single lot run at Reticon. The seventh CCD (Big CIT) will occupy an entire 4-inch wafer and will be fabricated at Loral Fairchild. The wafer runs fabricated at both Reticon and Loral Fairchild will be made with a standard three poly, two metal NMOS CCD process. Two of the sensors (Advanced Camera and Big CIT) are rear-illuminated and therefore will require thinning and backside coatings (AR and phosphor). These tasks will be performed at Reticon (Ref. 2). Wafer testing, backside accumulation, screening and calibration tests will be done at JPL. All Sandbox CCD designs were created at JPL in collaboration with Reticon and Loral Fairchild design engineers.

2. SANDBOX CCD DESCRIPTIONS

2.1 Cinema CCD

The Cinema CCD is a first generation 4096 x 4096, 3-phase, 9-micron pixel, frame transfer, color CCD. The sensor is intended to replace photographic film used in Hollywood moving picture cameras. The new CCD offers several new design challenges.

For example, the CCD will be readout at 30 frames/sec at an effective pixel rate of a quarter billion pixels per second. To achieve such rates the CCD is divided up into 32 sections for parallel readout. The array itself is split into four 1024 (V) x 4096 (H) regions forming two image and two storage sections. The split image is transferred towards the top and bottom of the array. From each storage region there are 16 horizontal registers that report to sixteen 3-stage on-chip amplifiers (Figure 1a). Each channel reads at approximately 8 M pixels/sec. Each pixel will be digitized in the camera 12-bits deep. A three-chip approach *will* be employed to obtain color information.

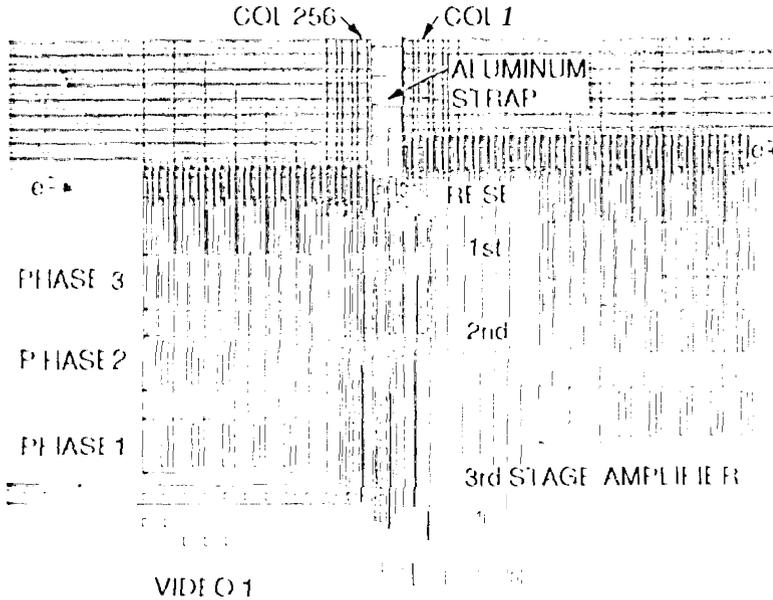


Figure 1a The Cinema CCD three-stage output amplifier. Thirty-two amplifiers are used to read the sensor at approximately 8 M pixels / sec / channel. The illustration shows staggered horizontal registers to access sense node. An aluminum strap is bussed into the array to improve high speed drive characteristics. Image processing performed by a large computer will remove the 12-bit from images generated.

Each image generated by the Cinema CCD *will* be processed by a large computer system. Some image processing requirements performed are: (1) gain/offset correction for each channel, (2) cosmetic removal, (3) image compression, and (4) color correction and alignment between the three CCDs. Since images are in digital format, "special effects" can be added to processed images at the same time.

2.2 Advanced Camera CCD

The Advanced Camera CCD is a high performance 4096 (V) x 4096 (H), 3-phase, 9-micron pixel, full frame, backside illuminated, CCD. The sensor is intended to be used on a third generation Hubble Space Telescope instrument. The array and two horizontal registers are split allowing 4 channel parallel readout. Two floating diffusion and two floating gate (Skipper) amplifiers are employed for ultra-low-noise performance (sub-electron rms). The chip *will* be thinned and use AR and phosphor coatings to cover a wide wavelength range (100 - 1000 Å). The backside will be accumulated with a molecular beam epitaxial process. For the Sandbox lot, this CCD is being built with a format of 4098 x 3071.

2.3 MACH II CCD

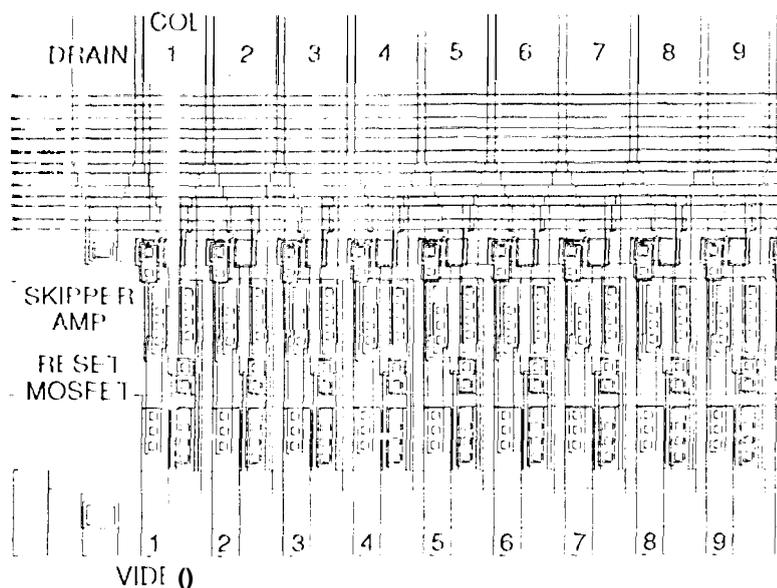
The MACH II CCD is a second generation 1024 x 1024, 6-phase, 36 (V) x 18 (H)-micron pixel, interlaced-frame transfer CCD. The sensor will be used to take two sequential 512 (V) x 1024 (H) images separated in time by less than 1- μ sec. Phases 4, 5, and 6 are masked off with a light shield serving as a storage region. The first image is collected in phases 1-3 and then quickly transferred (<1-micro-sec) into storage phases 4-6. A second image is then taken. The two interlaced images are then readout slow-scan (50 kpixels/sec) to achieve 4e- noise performance. Six-phase design is employed for high QE performance, low optical cross-talk between the two images and high speed operation. The CCD also incorporates a high speed readout channel for fast-scan applications where low-noise performance is not required.

2.4 Adapt II CCD

The Adapt II CCD is a second generation 128 (V) x 64 (H), 6 phase, 36-micron pixel, frame store, CCD. The CCD *will* be used

for wavefront sensing in *Adaptive Optics* camera systems. The device *will scan at 2000 frames/sec* at a *read noise < 3 e- rms*. *Sixty-four amplifiers* are provided, one amplifier *per column* (Figure 1b). The amplifiers are *Skipper type* to allow for multiple sampling and low-noise.

Figure 1 b. *Adapt 11* CCD output Skipper amplifiers. Sixty-four amplifiers are provided, one *for* each column. Column pitch is 36-microns. Six-phase (6-microns / phase) *clocking* is employed for high speed frame transfer operation.



2.5 PLUTO Flyby CCD

The Pluto Flyby CCD is a first generation 2048 (V) x 1024 (H), 3-phase, 9-micron pixel, frame store, CCD. The CCD will potentially be used in a NASA planetary mission to planet Pluto. One simple floating diffusion amplifier is used to readout the array.

2.6 Circulator CCD

The Circulator CCD is a 16 pixel, circular, test CCD (Figure 1c). The device is intended to interrogate a single electron. To do this, a Skipper amplifier takes a sample each time the electron makes one revolution around the circuit. The amplifier and signal channel have been designed for the lowest noise possible (e.g., signal channel width is only 5-microns wide to reduce readout capacitance). Thousands of samples can be taken to reduce the noise below 0.1 e- rms. At the center of the array is a diode which can be slightly forward biased to emit photons and generate charge in the signal channel if desired. We intend to inject a single electron thermally by controlling operating temperature. A dump gate and drain are also provided to erase charge in the channel before the experiment is performed.

2.7 Big CIT CCD

The Big CIT (California Institute of Technology) CCD is a 4096 x 4096, 3-phase, 15-micron, full frame, backside illuminated, CCD. The device will be used in ground based astronomical applications. The CCD is configured similar to the Advanced Camera CCD (i.e., quad array), allowing four channel readout if desired. The CCD will be one of the largest CCDs manufactured today.

3. PERFORMANCE CONSIDERATIONS

3.1 Dark current

A critical CCD parameter is thermally generated dark current. For CCD imagers there are three main sources of dark current.

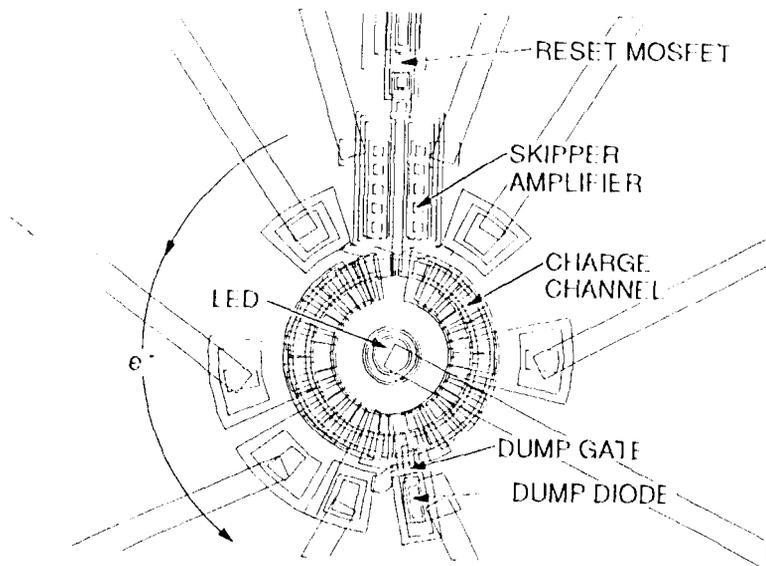


Figure 1c. Circulator CCD showing, 16 three-phase pixels. Charge is readout nondestructively by a Skipper amplifier to achieve sub electron noise performance. A dump gate and dump diode are used to quickly erase charge in signal channel. A 1.11 is provided to perform photon transfer calibration. The purpose of the device is to detect and locate a single thermal electron when generated.

These are: (1) thermal generation and diffusion in the neutral bulk, (2) thermal generation in the depletion region and (3) thermal generation due to surface states at the Si-SiO₂ interface. Of these sources, the contribution from surface states has been the dominant contributor for CCDs. Surface dark current varies significantly among manufacturers depending on processing details associated with oxide growth and surface passivation. Recent dark current tests show that dark levels vary widely for CCD manufacturers from 60 pA/cm² to 10 nA/cm² for noninverted CCDs (unless otherwise specified dark current figures in this paper are referenced to room temperature operation). Still higher generation rates (10,000 nA/cm²) are exhibited for backside illuminated CCDs when not properly accumulated.

Dark current generation at the Si-SiO₂ interface is primarily determined by two factors, namely the density of interface states and the density of free carriers (holes or electrons) that populate the interface. Electrons can thermally "hop" from the valence band to an interface state and into the conduction band as a free electron. The electron is then collected in a potential well as real signal. The presence of free carriers can fill these states inhibiting the hopping conduction process and in turn substantially reduce the dark generation rate. Noninverted CCDs maximize the amount of dark current generated since the interface is completely depleted of free carriers. However, when the CCD is inverted (e.g., M⁺), holes from the channel stop collect and populate the interface eliminating surface dark current. The only remaining dark current is produced in the bulk silicon.

Bulk dark current (i.e., M⁺ operation) also varies significantly from manufacturer to manufacturer. Levels as low as 2 pA/cm² and as high as 1 nA/cm² have been measured. Dark rate may also vary significantly from lot to lot for a single manufacturer using a single process. For example, three consecutive lots were fabricated for the recent W⁺ '11 project. Dark rates for these CCDs ranged from 20 to 400 pA/cm². The difference noted was related to the quality of the silicon wafers used and bulk state density.

Bulk states are lattice imperfections or impurities of some kind (e.g., gold). High quality silicon implies that bulk state density is very low. Bulk states generate dark current also via "hopping conduction" by jumping through states in the band-gap. When a CCD is "bulk state limited" individual spikes often dominate the dark floor seen. For example, Figure 2a shows a dark current line stacking plot generated by a 1024x1024 pixel Fairchild MPP CCD. The average dark floor measured for the sensor is < 10 pA/cm². Note that each spike generates approximately the same amount of charge indicating a specific impurity is at work. Some pixels exhibit multiple spikes explaining why several distinct signal levels are seen in the plot. The dark current pedestal on which the spikes ride is believed to be in part generated in the "bird's beak" near the channel stop region where inversion is not fully achieved (refer to Section 7). Also, surface dark current is generated each time a line is transferred since the phases must come out of inversion for a brief period of time.

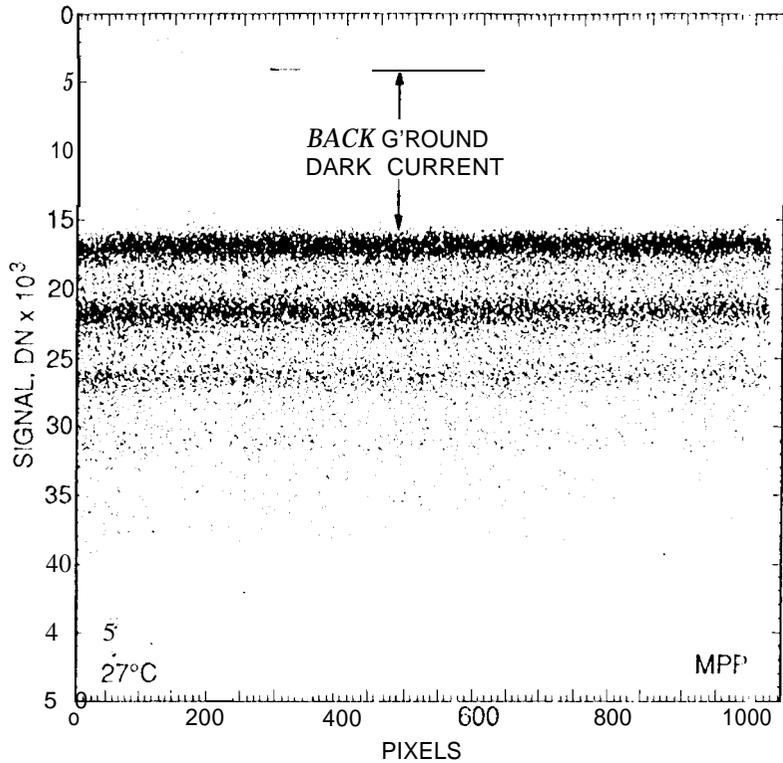
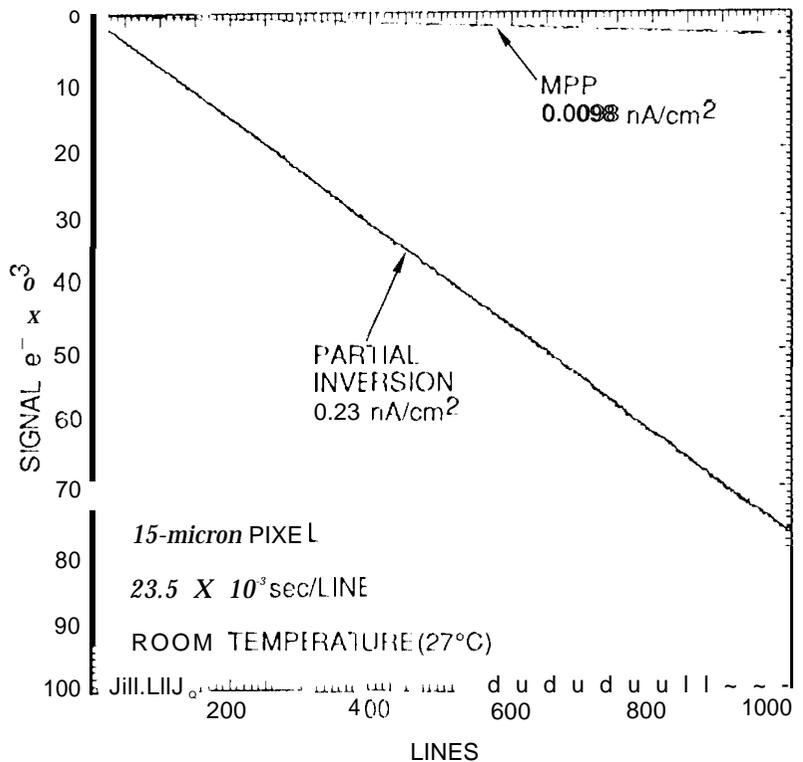


Figure 2a. Dark spike pattern generated by a MPP CCD. Spikes are associated with a specific bulk state that generates the same amount of charge per unit time. Some pixels contain multiple spikes resulting in discrete signal levels shown. Background dark current is generated from several sources including surface dark current when phases come out of inversion during line transfer.

The CCD tested in Figure 2a can integrate charge for six minutes at room temperature before saturating Figure 2b plots average dark current build up as a function of lines readout (each line takes 23.5 ins). Partial inverted and MPP responses are shown. After one frame readout (23 seconds) the MPP dark floor has only risen by 3000 e⁻.

Figure 2b. MPP and PI average dark current build-up after the CCD is quickly erased and then slowly readout at room temperature. MPP dark rate is 20 times less than partially inverted (PI) operation. Dark current for PI clocking is 5 times lower than non inverted (NI) clocking.



Experimental CCD lot runs are sometimes fabricated to find good silicon and achieve low dark current generation. These lots are usually "split" using different types of silicon that are processed identically. Test results have been surprising. For example, silicon purchased from one foundry with the same specifications showed a large variance, 10 pA/cm² to 0.6 nA/cm² operating, MPP. Large dark spikes were observed from silicon purchased from another foundry. These spikes generated charge at a rate as high as 10,000 nA/cm². These spikes were later found to be associated with lattice slacking faults that were visible to the naked eye.

As a rule of thumb, bulk dark current for quality silicon is roughly equal to the thickness of the epitaxial layer when expressed in units of pA/cm². For example, a 10-micron epitaxial CCD typically exhibits 10 pA/cm² when fully inverted. Ultra-low dark rates can be achieved by thinning the CCD thereby eliminating substrate and epitaxial interface dark current. For example, MPP dark current for thinned Reticon CCDs exhibit less than 5 pA/cm².

3.2 Charge transfer efficiency

CTE performance varies significantly among CCDs and is also very dependent on silicon material. CTE and MPP dark current performance typically go hand in hand. That is, if bulk dark current is low then CTE performance is also well behaved. This correlation assumes that there are not other CTE impediments that limit performance such as design or process CTE traps.

CTE is specified in pixel transfers at a specified test x-ray signal level. CTE is especially critical to Advanced Camera because ultra-small charge packets will be transferred. For example, the CTE specified for this CCD is 0.99999 for a charge packet size of 1620 e⁻. A deferred charge loss of 7 e⁻ is expected for 4096 pixel transfers.

Bulk traps that happen to lie within the charge transfer channel can trap charge, typically involving a single electron. Figure 3a shows an Fe-55 x-ray (1620 e⁻) response generated by a 800 x 800, 01 al Fairchild three-phase CCD that is bulk state limited. We stack, accumulate and display 1024 lines of data into the single trace shown. Note that the single pixel x-ray event line rapidly decreases as more and more charge is fed to trailing pixels (also seen in the plot). Horizontal CTE (HCTE) is very poor (<0.996) wherein vertical CTE (VCTE) is perfect (also measured by x-rays by stacking columns). Data was generated at an operating temperature of -130 C and using, a horizontal clock overlap of 1 micro-sec operating the CCD at a warmer

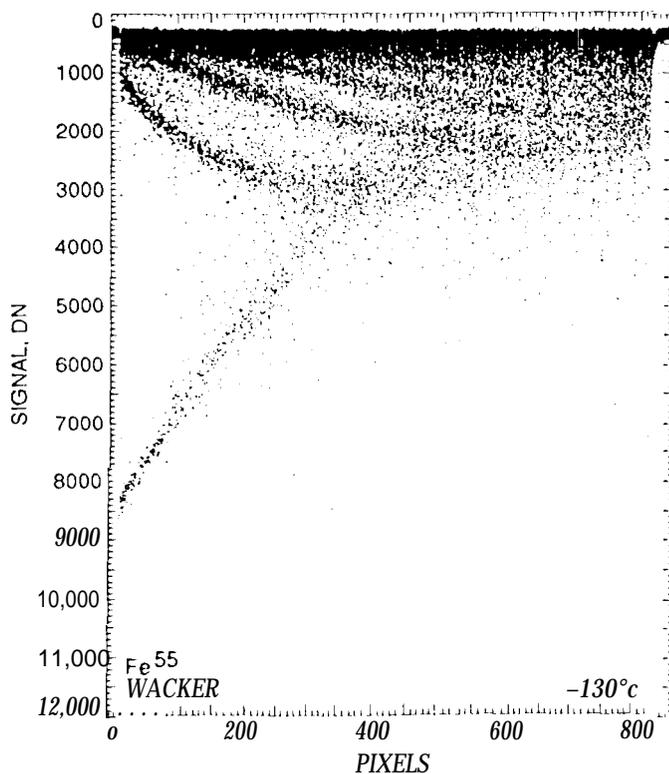


Figure 3a. HCTE x-ray response (Fe-55, 1620 e⁻ / event) for a WF/PC II CCD fabricated on silicon material that exhibits shallow bulk traps. The bulk states result in severe trapping and poor CTE only in the horizontal direction (VCTE is perfect). Deferred charge levels associated with trailing pixels are clearly seen. Note after 300 pixel transfers that more charge is contained in trailing pixels than the target pixel.

temperature or increasing the clock overlap period improves HCTE significantly. For example, Figure 3b and c show horizontal x-ray responses for two different clock overlaps (1 micro-sec compared to 4 micro-sec respectively) at an operating temperature of -110C. The improvement in CTE is clearly evident when the overlap and temperature is increased. Figure 3d shows HCTE improvement as a function of operating temperature. The response is the composite of nine line stacking x-ray measurements, data taken from the center of the horizontal register. Note that HCTE degrades rapidly for operating temperatures below -80 C. CCDs made on different silicon material in the same lot run did not exhibit the CTE problems over the temperature range or clock overlap period investigated. The difference is striking.

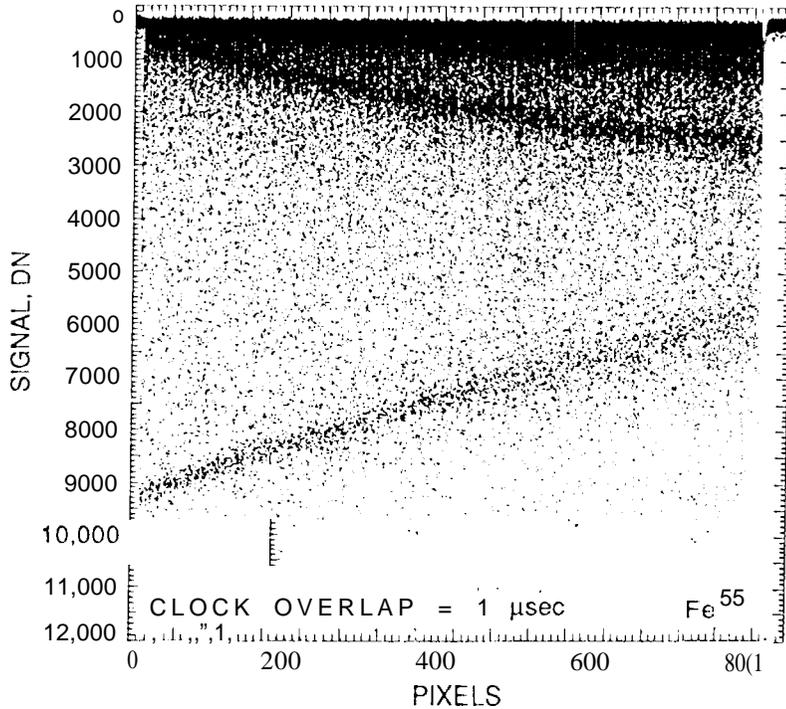
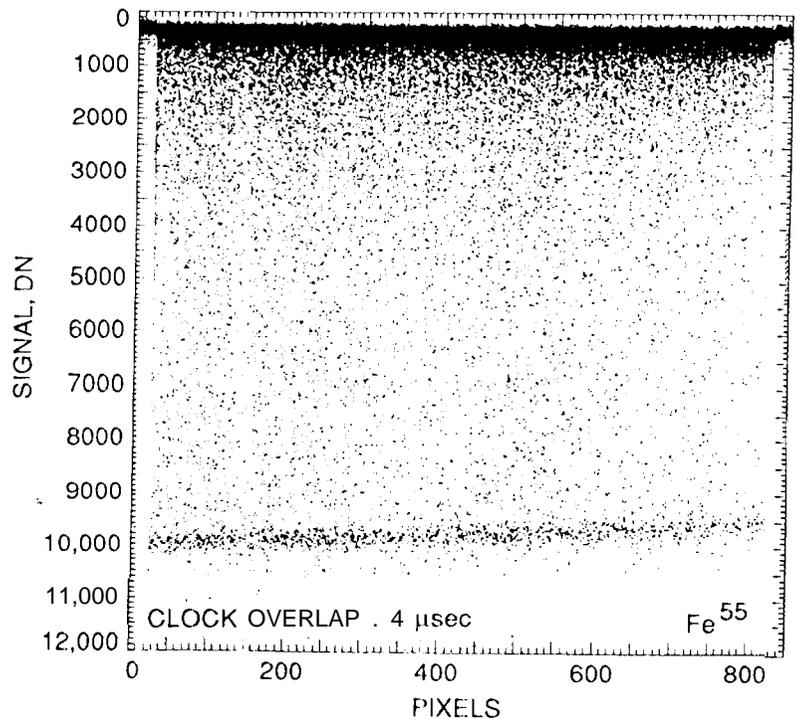


Figure 3b. HCTE x-ray response for the same WF/PC 11 CCD at a elevated temperature (from -130 C to -110 C). CTE improves significantly because bulk traps detrapp charge at a faster rate within the 1-micro-sec clock-overlap period used. Single pixel and deferred charge event lines are clearly seen. Target pixels loose approximately 40 % of charge after 800 pixel transfers.

Figure 3c. HCTE x-ray response when the clock-overlap is increased to 4 micro-sec. Additional transfer time allows charge to escape from traps. CTE performance is nearly perfect. Target pixels at the end of the horizontal register only suffer a 7 % loss making the device usable for most scientific applications..



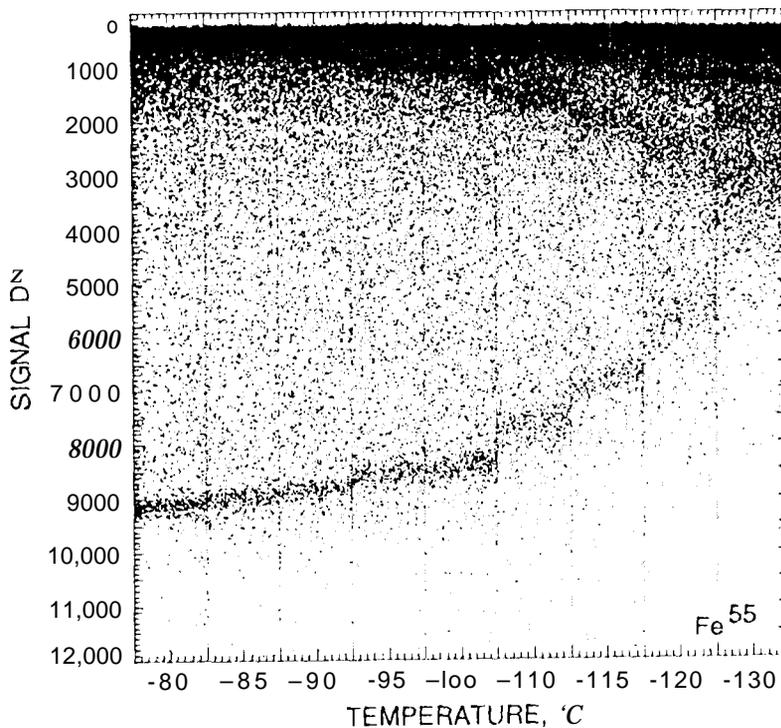


Figure 3d. HCTE x-ray responses generated as a function of operating temperature (data taken from a 400-500 pixel region). Operating temperatures above -80 C exhibit perfect HCTE when tile clock-overlap period is greater than 1-micro-see. These operating specifications are supplied when sensors are delivered for use.

Curiously CTE characteristics for the WF/PC II CCD exhibits completely opposite behavior to the data presented in Figure 3. For example, Figure 4a shows two x-ray stacking column tracts for two MPP WF/PC II CCDs built indifferent silicon wafers (referred to as Type "B" and Type "A"). Data was taken at an operating temperature of -30 C. Note that the VCTE for Type B silicon is poor compared to Type A. HCTE for both sensors is perfect (also opposite to the data presented in Figure 3). Lowering the operating temperature to -90 C for Type A material improves VCTE significantly as shown in Figure 4c. Figure 4d shows similar CTE responses at 0 C. Here CTE varies significantly for Type A material whereas Type B exhibits no temperature dependence. Note also that the MPP dark floor indicated for Type A silicon is much greater compared to Type B (approximately 20 times higher). As mentioned above, CTE and MPP dark current performance go hand-in-hand when performance is bulk state limited. Unfortunately WF/PC 11 ended up flying silicon Type A material because of schedule problems.

The radical difference between the responses observed in Figures 3 and 4 is due to the emission time constant (T_e) related to bulk traps. For example, the bulk traps that degrade CTE in Figure 3 are relatively shallow traps (trap depth is measured from the conduction band edge). When charge is trapped by a shallow trap it can thermally escape in a short period of time back into the conduction band. CTE can be improved by increasing the operating temperature thereby giving more thermal energy to the carriers to escape the traps faster. Increasing the clock overlap period allows more time for charge to escape the traps. This effect explains why the VCTE is superior to HCTE in Figure 3a. A vertical clock overlap period of 60 micro-see was used, long enough to allow charge to escape the bulk traps vertically.

When the traps are deep, like those that plague the WF/PC II CCD, completely opposite test results are recorded. Also different solutions are applied to improve CTE. Operating the CCD at a very cold temperature keeps carriers confined to deep traps by removing kT agitation. Once the trap is filled it can remain filled for a long period of time and not trap new charge. As long as there is a small amount of background charge around, the traps will be satisfied resulting in well behaved CTE. Fat-zero charge can come from various sources that are often unknown to the user because levels required are very small (sources of dark charge, spurious charge, sky background, cosmic rays, etc.). Extended images (such as the moon) typically exhibit no CTE difficulties since traps are satisfied by the first charge packets that move through the array (i.e., in this case the first pixels that define the limb of the moon).

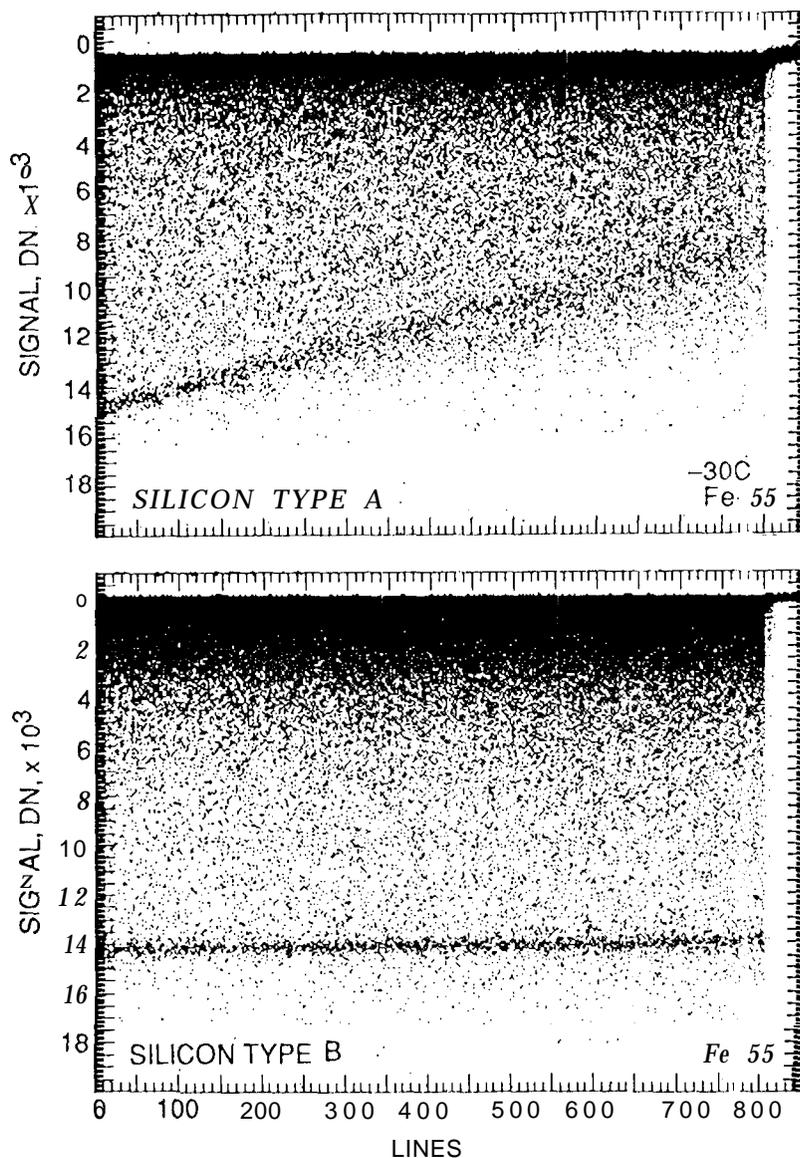


Figure 4a. VCTE responses for two WF/PC II CCDs fabricated on two different types of silicon. Type A silicon shows poor CTE performance because of deep level active bulk states whereas type B exhibits near perfect CTE over all operating temperatures tested. Unfortunately, WF/PC 11 used Type A silicon because of schedule reasons. However, studying the problem yielded a solution described in text.

When bulk state limited, transferring point images is more difficult especially if widely separated. For example, t_c for the WF/PC 11 traps are on the order of a thousand seconds when operating at -80 C. At this temperature approximately 10 % of the charge is deferred when measured at the top of the array (assuming a 1620 e⁻ charge packet). This photometry error is based on measuring standard star clusters without fat-zero charge present. Cooling the device to -90 C improves accuracy to 2 % because the traps remain satisfied for a longer period of time because less background charge is required (refer to Figure 4b).

Note that all CTE tests performed above stimulate the CCD with x-rays. X-rays generate an exact known amount of charge making CTE measurements straightforward and absolute. There have been many relative CTE test techniques invented (EPER, dark spike stimulus, optical point source, edge stimulus, electrical charge injection via input diode/gate, etc.) methods that compare the amplitude of the charge contained in the target pixel to the deferred charge that follows. These techniques usually yield incorrect estimates of CTE by overestimating its true value. For example, WF/PC 11 star images at -60 C appear sharp with no evidence of deferred charge. Relative CTE methods would have proclaimed perfect CTE for the CCD (in fact photometry error is $> 20\%$). However, as mentioned above, the long emission time constant for the traps spreads deferred charge across the array and is not apparent in the read noise. Only x-rays (or an absolute source such as standard stars) can measure true CTE.

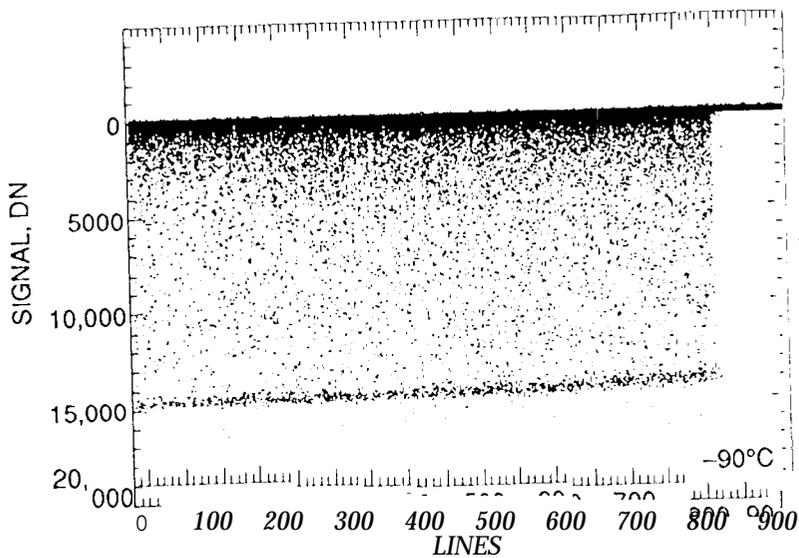


Figure 4b. Type A silicon tested at -90 C exhibiting improved CTE performance (WF/PC 11 nominal operating temperature on the Hubble Space Telescope). Photometry error at the top of the array (i.e., line 800) is approximately 3% for a 1620 e^- point source of charge. Computer image processing algorithms are used to correct this error below 1%, WF/PCs photometry spec.HCTE performance is perfect for all temperatures tested.

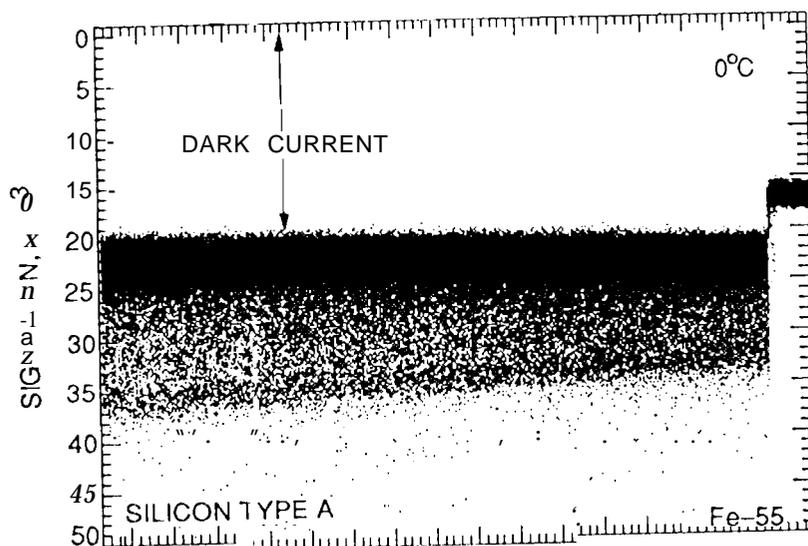
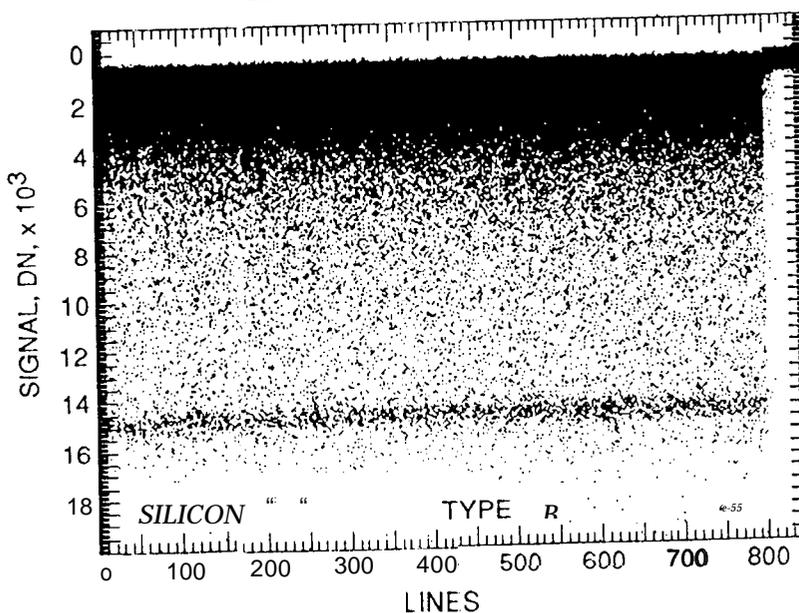


Figure 4c. VCTE responses at 0 C showing differences in MPP dark current generation. Dark current is 20 times higher for Type A silicon compared to type B. CTE and bulk dark current performance are typically related because of bulk states.



Many CCD manufacturers fall victim to relative CTE measurement Techniques. We demonstrate the problem in Figure 5a for a 1024 x 1024 CCD with a CTE problem (the sensor was purposely irradiated with neutrons to induce deep level traps, approximately 0.45 eV deep). The 50 x 50 sub-area of pixels shown was taken at the top of the CCD opposite from the lower on-chip amplifier (selected 10 accentuate VCTE charge problems in the array). After integrating for several seconds charge is transferred down and to the left in the images shown. Horizontal CTE appears perfect because the traps are deep level (i.e., traps are satisfied in the horizontal register because they are constantly being fed). The region selected contains several dark spikes (also induced by the neutrons) and are used as point signal sources (each that generate a constant amount of charge per unit time). The top image exhibits deferred charge tails following each dark spike indicating a CTE problem for the CCD. The lower image shows the same region except that the vertical clocking rate is increased by a factor of 12 (i.e., from 44.5 to 514 lines/sec). Note that the deferred charge tails completely disappear suggesting that CTE has been enhanced by simply clocking the CCD faster. The apparent CTE improvement seen when clocking the CCD faster is investigated further in Figure 5b. A single column trace is presented that contains a large dark spike. The spike and corresponding deferred tail was measured at different array readout rates (23 see, 19 see, etc.). Charge is transferred from right to left in the plot. A large deferred tail is seen following the dark spike for a readout time of 23 seconds. As the vertical clock rate is increased the deferred tail becomes smaller and smaller. At a frame time of 1.99 sec the tail is almost eliminated. Although CTE appears to improve (in a relative sense), the amplitude of the dark spike remains roughly the same size independent of clock rate. Since the dark spike generates the same amount of charge during integration deferred charge must also be fixed for each frame time. This behavior indicates

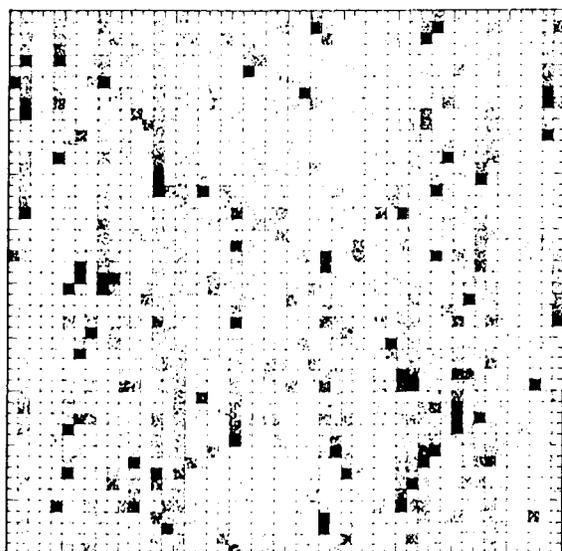
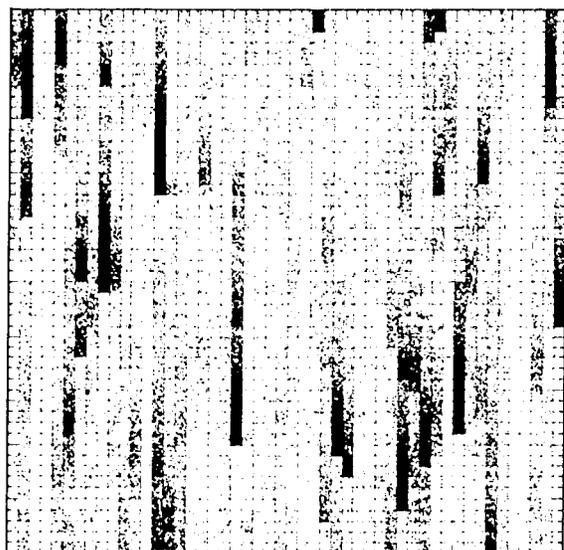


Figure 5a Two dark spike images generated at two different frame rates. The top image exhibits deferred charge tails whereas the bottom image does not. Comparing the images suggests that CTE performance is better in the lower image.

that deferred charge has spread over more pixels as the rate increases making it more difficult to detect because of the noise floor.

Figure 5c shows the true amplitude of the dark spike by measuring CTE characteristics using the CCD's upper on-chip amplifier. Clocking the sensor in this manner minimizes the number of vertical transfers. Comparing the dark spike amplitude in Figure 5b to Figure 5c shows that approximately 2/3 of the charge generated by the dark spike is deferred and is independent of vertical clock rate. CTE performance is very poor at all clocks rates investigated, a conclusion that would not be drawn by only examining the deferred tail.

when transferring charge towards the

stopping with almost no CTE degradation,

2/3 of the charge generated by the dark

spike is deferred and is independent of vertical clock rate.

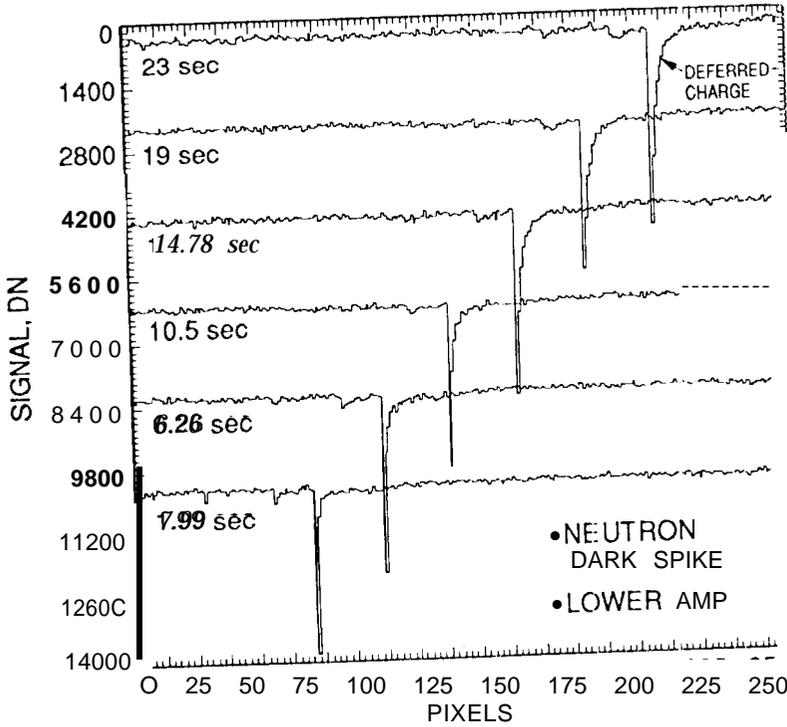
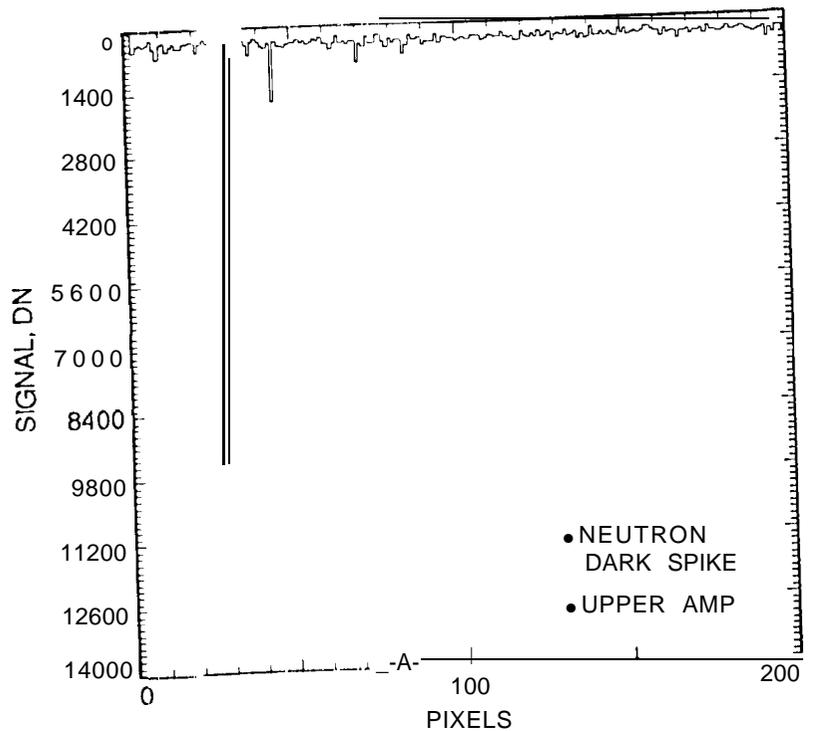


Figure 5b. A single dark spike characterized showing a deferred charge tail. Note when the CCD is clocked faster that the tail disappears implying that CTE improves. However, the dark spike amplitude remains essentially the same indicating that charge is spread over more trailing pixels with rate increase. Hence, speed has no significant effect on absolute CTE performance for the sensor.

Figure 5c. The same dark spike readout using the upper amplifier to minimize the number of vertical transfers. No deferred tail is seen. Also the amplitude of the spike increases by a factor of two compared to lower amplifier readout. Also two small spikes emerge barely seen in Figure 5 b.



The apparent CTE loss, as measured by x-rays (or point sources like stars), is also dependent on the separation between events. If the population of x-ray events on the array is low then the events must go through the array alone. However, if their density is relatively high then events will aid each other in the transfer process. This effect is especially pronounced when no background charge is present. Charge separation effects are demonstrated in Figure 6 where two x-ray column stacking responses are shown. The 1024 x 1024 CCD tested is partially damaged with protons. Half of the array is shielded and not damaged. The CCD is exposed to x-rays and then quickly clocked vertically (600 micro-sec/line) reading out approximately 512 lines. On the average there are 100 x-ray events per line. The data associated with these pixels is discarded by the computer. The remaining half of the array is then clocked slowly (20 ms/line) and saved by the computer. Vertical stacking plots are then generated for the damaged and shielded regions as displayed in Figure 6a. Note that the damaged region (the tilted response) begins at the ideal level for the shielded region (the flat response). This indicates that during high speed clocking that most x-ray events are not trapped because separation between events decreases compared to slow-scan readout which exhibits a tilt. Figure 6b shows the results of a similar experiment where the separation between events is reduced by a factor of 100 (i.e., 1 event/line). Note that the response for the damaged region does not begin at the ideal level indicating that charge is trapped more often during high speed readout because events are widely separated.

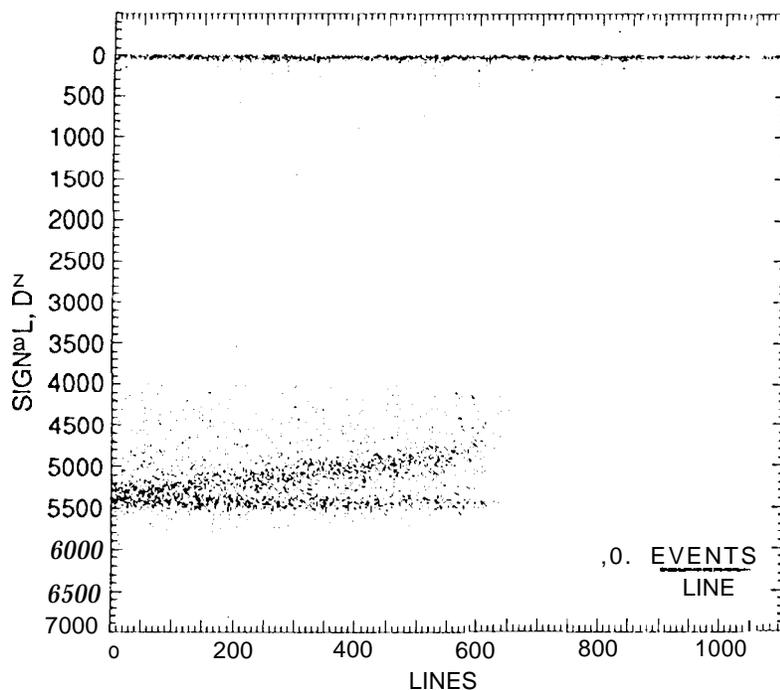


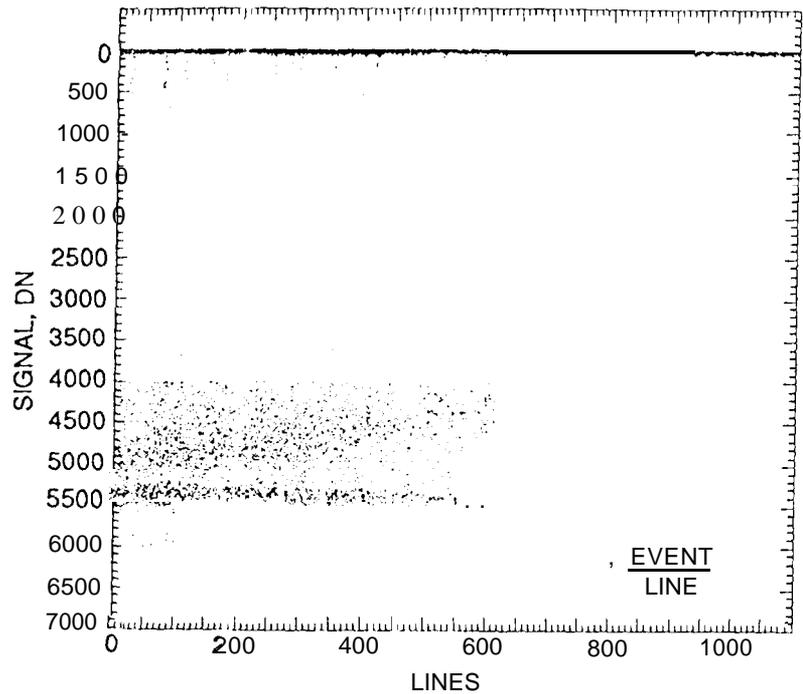
Figure 6a. VCTE responses taken from two subarrays - proton damaged and shielded regions. The damaged region exhibits good CTE when clocked at a fast rate (600 micro-sec./line). The single pixel event line for the region begins at the ideal level. Under these conditions the average time between x-ray events during readout is $< T_c$, hence events aid each other in the transfer process. Reading the CCD slow-scan (20 ins/line) causes the CTE to degrade in the damaged region resulting in the tilted response shown. The average time between events in this case is $> T_c$ and most events must go through the array alone. The shielded region shows good CTE.

The capture time constant (T_c) associated with deep traps also influences CTE results. Theory claims that T_c is very short (less than 1 micro-sec) and electrons are trapped instantaneously when transferred into a potential well. Therefore, it is generally assumed that $T_c \ll T_e$. This is true for the most part, however, electrons at the bottom of a well can be thermally agitated forcing them to move up the sides of a potential well and find new traps. The more time given to the electron the greater the probability it will find a trap. This effectively increases T_c for some traps. Hence, for this reason it is best to clock the CCD as fast as possible to minimize this trapping effect. This requirement only applies to deep traps.

For some CCDs charge trapping can become so severe that the device must be light flooded to fill in the traps and then erased quickly before an image is taken (the Galileo CCD - a 800 x 800 CCD in route to Jupiter, and the Cassini CCD are used in this manner because of radiation induced bulk traps). However, for this technique to work properly the operating temperature must be sufficiently low to keep the traps filled during integration and readout (e.g., Galileo operates at -120 C),

Therefore, T_c , T_e , operating temperature, clock overlap, clock rate, background charge, charge distribution, and charge packet size are important factors that influence CTE when bulk states exist (there are others). Ideally, CCDs should be built on quality silicon to avoid CTE and dark current problems discussed above. However, no matter how good the material some bulk states

Figure 6b. VCTE response when the x-ray event density is reduced by a factor of 100. This effectively increases the time between events. Both fast-scan and slow-scan exhibit degraded CTE in the damaged region.



will always exist. As CCDs become larger (such as the 4096x4096 Sandbox CCDs) and performance requirements get tighter, these variables must be completely understood and controlled by the user if optimum CTE performance is to be realized.

Unfortunately no method has been devised to determine the quality of silicon before a lot of CCDs is run. The only successful approach has been to purchase many silicon wafers and include some of them in ongoing lot runs to be evaluated later over a wide temperature and clocking range (to cover all applications intended). If the silicon tests good then the wafers can be used in future lots.

The technique of "pocket pumping" is one method often used in our lab to characterize silicon material once a CCD has been fabricated. This method allows one to locate and count the number of active bulk traps that influence CTE performance. For example, Figure 7a shows a pocket pumping map generated for quality silicon material. The density of traps measured is 0.002 single electron active traps per pixel based on a 1600 e- flat field signal and an operating temperature of -100 C (trap density changes when these variables are changed for reasons given above). CTE for this CCD is exceptionally high yielding a CTE > 0.999999 under the conditions tested here. Figures 7b and c show raw pocket pumping responses. Figure 7b was taken at an operating temperature of -90 C whereas Figure 7c was generated at -120 C. Note that some traps freeze-out at -120 C (i.e., T_c for these traps become longer than the clock overlap employed in the pocket pumping experiment).

From the discussion above dark current generation and CTE performance can be a hit and miss game. Fortunately the Sandbox CCDs have selected quality silicon based on previous lot builds. Therefore, low dark current (< 1 nA/cm² noninverted and < 20 pA/cm² MPP) and well behaved CTE performance are expected. However, some operational tricks, such as those demonstrated above, may be required.

3.3 Well capacity

Full well is an important characteristic to the Sandbox CCDS especially for the 9-micron pixel devices where dynamic range is at a premium. This section discusses how both the user and manufacturer optimize full well performance for small pixel devices.

3.3.1 Surface and bloomed full well operation

The gates of CCD can be clocked in three different ways. We refer to these clocking modes as noninverted (NI), partially

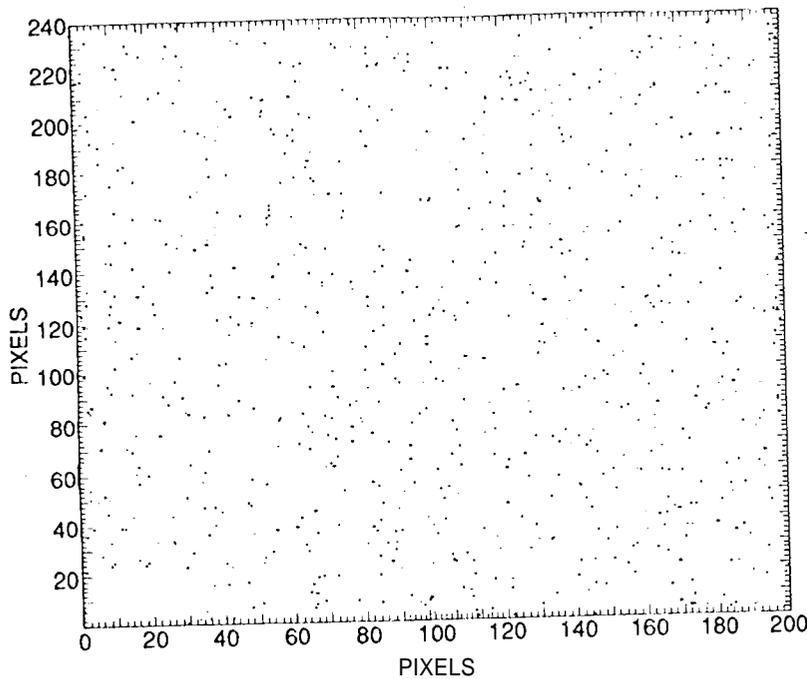
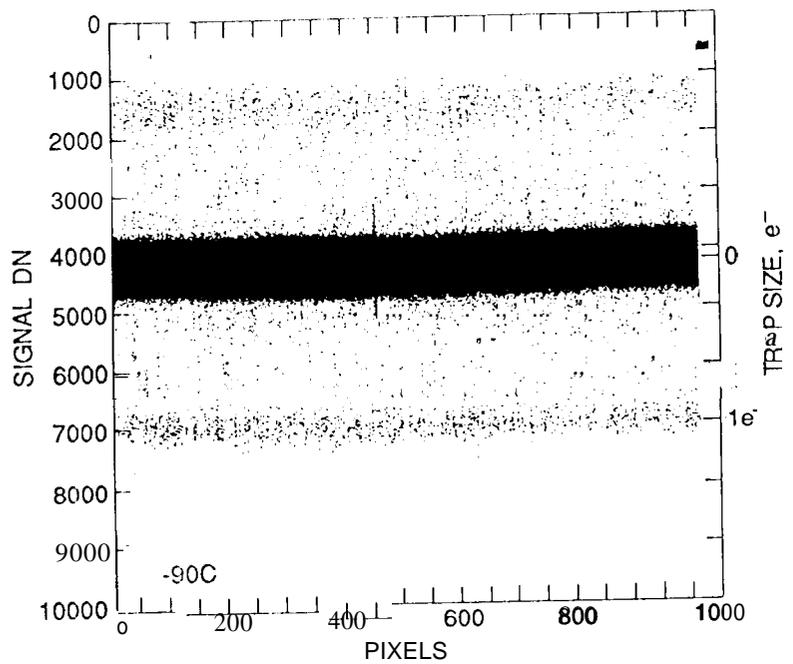


Figure 7a. Array pocket pumping trap map showing individual 1 e- array traps. A 240 x 200 pixel region is shown. A trap density of 0.002 traps/pixel is measured for the operating temperature (-90 C), vertical clock-overlap (60 micro-see), and signal level (4000 e-) employed. CTE for the CCD is exceptional, >0.999999 as measured by x-rays. Decreasing operating temperature or clocking the CCD faster effectively reduces trap count further improving CTE. Increasing the signal level increases trap density because the charge packets occupy more volume in the channel.

Figure 7b. A raw pocket pumping response showing individual 1 e- traps at an operating temperature of -90 C. Traps less than 1 e- are statistical, trapping and releasing charge randomly.



inverted (PI), and multi-pinned phase (MPP). The user can select the best mode for the application. However, it is often best to design a camera system so that all three modes can be utilized on command. In operation implies that the clocks to the CCD never swing low enough to invert the signal channel (e.g., -3 to +5 V). PI means that clocks invert as they switch (e.g., -8 to +5 V). For a three phase CCD one phase must be high at all times to keep charge confined to a pixel (hence the name partially inverted). MPP operation is where all clocks are normally inverted most of the time except during line transfer (e.g., -8 V). Each mode of operation has a profound effect on CCD performance. Well Capacity, dark current generation, residual image, anti-blooming, radiation damage tolerance, charge transfer, and pixel nonuniformity are some CCD parameters influenced by these clocking modes. We only examine well capacity here.

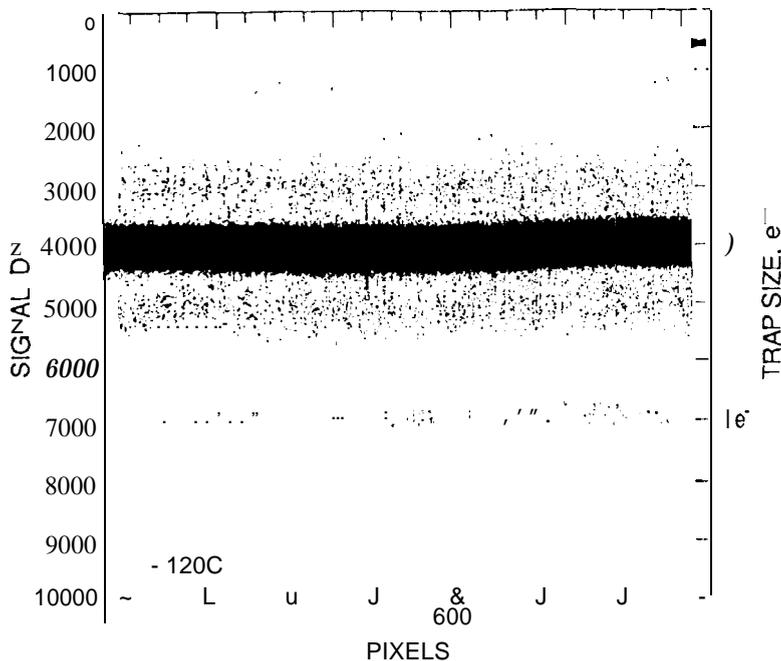


Figure 7c. Pocket pumping response taken at an operating temperature of -120 C . Note that some traps begin to freeze-out at this temperature (i.e., traps trap and hold charge over pocket pumping cycle). Other shallower traps are not affected by the temperature change indicating that at least two different bulk states are involved (possibly phosphorus and oxygen vacancies). X-ray measurement show that CTE improves when the temperature is lowered.

Optimum full well is achieved when the CCD is clocked into inversion. The increase in well capacity under inverted clocking can be significant compared to noninverted operation. For example, full well for the first generation Texas Instruments Space Telescope CCDS (WF/PC 1) could have been increased by a factor of three over what was originally flown if clocked PI. Unfortunately the flight units were clocked NI (from 0 to 7 V) yielding only 30,000 e^- well capacity. One year after these CCDs were placed into orbit flight spare units were clocked into inversion for the first time (approximately -8 V) resulting in a full well of 90,000 e^- . Additional capacity was achieved when the collecting phases were driven to $+4\text{ V}$ yielding 100,000 e^- overall. The apparent full well increase was not clear when the tests were performed for results were obtained by trail and error methods. We now, several years later, understand how to optimize well capacity for the CCD. A brief discussion on full well theory follows.

Well capacity for a pixel is defined when charge either blooms over a barrier phase into adjacent pixels or when charge in a potential well begins to interact with the surface at the Si-SiO₂ interface. Blooming is reduced by biasing barrier phases to the lowest channel potential possible (i.e., inversion). This condition allows for maximum charge collection and the greatest potential difference between the collecting and barrier phases.

A potential well collapses when charge is collected, Blooming will result if the channel potential for the collecting phase equals the potential of the barrier phase. We refer to this condition as "bloomed full well" (BFW). Also as charge collects the potential maximum also moves towards the surface. Therefore, it is possible for the potential maximum to first reach the surface before the onset of blooming. If this happens we say the CCD has reached the "surface full well" (SFW) state. Which comes first, BFW or SFW, depends solely upon the positive clock level of the collecting phase. Optimum capacity occurs when BFW and SFW occur simultaneously, a very important bias state that user must find for optimum performance.

Figure 8 plots full well as a function of positive drive for a three-phase CCD. BFW and SFW regimes are indicated in the figure. Data was generated in the following manner. A 100×100 pixel region on the array is saturated with light. If the CCD is biased in the BFW regime then charge will run up and down columns from the exposed region. After the shutter is closed extra time (a few seconds) is given to allow this process to reach equilibrium (blooming is a time dependent process). The resultant signal level is measured in the area representing a BFW data point. To detect SFW another procedure is used. After integration, with the shutter closed, we clock phases 2 and 3 while leaving phase 3 inverted as a barrier preventing charge from transferring. If the CCD is SFW limited charge will get trapped at the Si-SiO₂ interface under phases 1 and 2. Each time these phases are switched into inversion holes recombine with these trapped electrons. Eventually, if the device is clocked long enough (a couple of seconds at 2000 Hz is satisfactory), the charge level will reach equilibrium at SFW (this same technique is also

used to prevent blooming when the shutter is open). Signal is measured in the region representing a SFW data point. These two measurement techniques are performed in series to generate the full well curve shown in Figure 8.

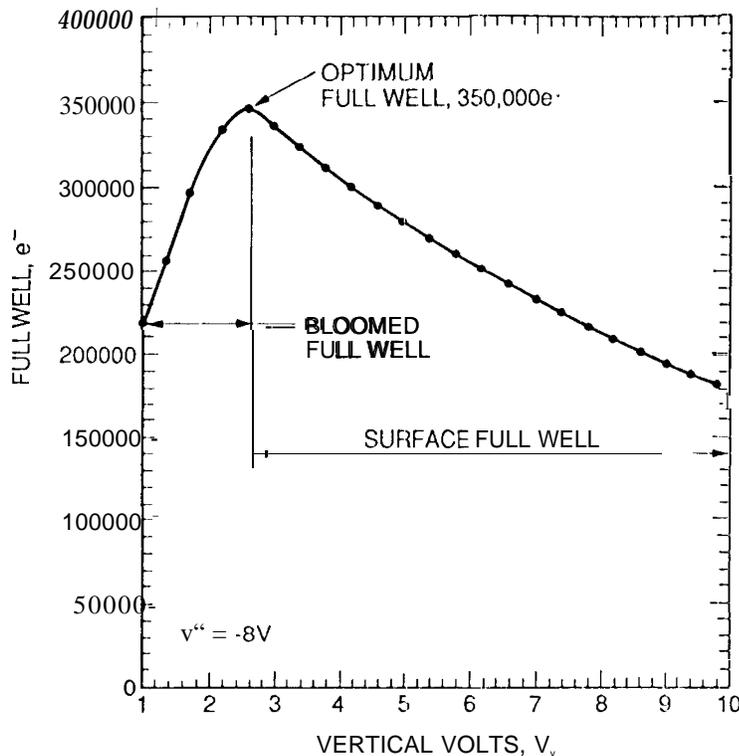


Figure 8. Full well characteristics as a function of positive drive using PI clocking. BFW and SFW regimes are indicated. Optimum full well occurs where charge interacts at the surface simultaneously when charge blooms over barrier phases. Data was generated by a 1024 x 1024, 18-micron pixel CCD. Optimum charge capacity for the CCD is 350,000 e^- .

Note in Figure 8 that optimum well capacity occurs when the collecting phase is driven to 2.5 V yielding 350,000 e^- . At this point $BFW = SFW$. Increasing the gate voltage above optimum moves the channel potential closer to the surface reducing SFW. At some very high gate voltage (not shown on plot) the potential maximum reaches the surface at which point $SFW = 0$. BFW is extraordinarily high under this clocked condition since the potential difference between the collecting and barrier phases is several volts. When clocked in the BFW regime the sensor will never run surface channel. Instead charge will bloom up and down the channel. BFW is reduced to zero when the potential of collecting and barrier phases are equivalent (i.e., when all are driven into inversion).

3.3.2 Full well process and design considerations

The discussion above demonstrates how the user optimizes full well performance by the manner in which the CCD is clocked (additional discussions are given below). The CCD manufacturer also plays an important role in maximizing well capacity (Ref. 3). Different design and process methods are employed to accomplish this. The depth and doping concentration of the n-channel are the two main process methods used to control full well. SFW and BFW both increase with channel doping. The amount of charge that can be collected in a potential well is proportional to the number of ionized phosphorus atoms in the n-layer. If the channel is lightly doped then the potential well will collapse faster as electrons are collected (limiting BFW). Also the rate at which the potential maximum moves towards the surface is faster for lightly doped channels (limiting SFW).

CCD manufacturers attempt to use maximum channel doping to increase charge capacity. However, there is a practical limit to the doping concentration that can be employed. For example, as the doping level increases higher gate clocks are required to control the collecting and barrier phases (both that stress the gate insulator). Channel depletion also requires higher bias to the channel (i.e., V_{REF}). However, the main limitation is associated with the electric fields generated in the middle of the channel near the surface where the fields are strongest. If the doping is excessive, high fields will generate dark spikes. In fact, fields can be fabricated where the CCD avalanches, saturating the CCD permanently. High internal fields also make the CCD vulnerable to radiation damage problems. For example, dark spikes are generated when the silicon lattice is damaged and high fields are present (i.e., field assisted dark current emission). Radiation sources, such as protons, induce lattice damage which

in turn leads to dark spike problems (refer to Figure 5).

Channel doping also influences characteristics of the on-chip amplifier. The performance of this transistor will degrade if channel doping is too heavy. This in turn results in higher read noise and nonlinearity for the device. To circumvent this problem manufacturers dope the amplifier and array independently using different reticles. The Sand Box CCDs are fabricated in this fashion where doping concentration of the array will be heavier than the amplifier to optimize charge capacity ($1.9 \times 10^{16} \text{ cm}^{-3}$ and $1.6 \times 10^{16} \text{ cm}^{-3}$ total dose respectively).

Although not as influential as channel doping, SFW conditions improve when the n-channel is made deeper. This is accomplished by an extended, high temperature cycle that drives phosphorus into the epitaxial layer. A deeper channel moves signal charge away from surface improving CTE (suppresses traps) and SFW characteristics.

Channel doping for three-phase buried channel CCDs is limited to about $2.5 \times 10^{16} \text{ cm}^{-3}$ (assuming box-like distribution - surface doping is approximately 2x higher) before dark spikes and clock drive become uncontrolled. The WF/PC 11 and Cassini CCDs employed channel doping of $1.6 \times 10^{16} \text{ cm}^{-3}$ and a 45 minute/1075 C channel drive. Well capacity for the CCD, when clocked PI, is approximately 4200 e- per square micron of active channel (i.e., less channel stops). Both the Cassini and WF/PC II CCDs were designed with 2-micron channel stops which encroach into the channel approximately 4-microns after processing. The Cassini CCD is a 12-micron pixel and the Space Telescope a 15-micron pixel. Hence, full well for the Cassini and WF/PC 11 CCDs achieve a full well of 134,000 and 231,000 e- respectively.

It is interesting to compare full well performance for the original WF/PC I CCD to the new WF/PC II CCD fabricated 15 years later. Recall from above discussions that well capacity for the WF/PC I was only 30,000 e-, a factor of 7.7 times smaller than WF/PC II for the same size pixel. The full well increase has come from design, process and clocking improvements made over the years.

3.3.3 MPP full well

When the first MPP CCDs were fabricated full well performance capacity was far from optimum. For maximum well capacity the doping concentration (usually boron) beneath the MPP phase (typically phase 3 for a 3-phase CCD) must be carefully selected. Without the MPP implant full well is zero since the channel potentials for all three phases are equivalent when inverted. Adding boron compensates phosphorus atoms that define the n-buried channel. Boron causes the potential under phase 3 to decrease relative to phases 1 and 2 allowing charge to collect. Well capacity for a MPP CCD therefore initially increases with boron concentration. However, doping phase 3 compensates the phosphorus atoms that define the buried channel. This in turn causes the potential maximum of the channel to move closer towards the surface lowering SFW capacity under this phase. Optimum full well is realized when the charge capacity under phases 1 and 2 equals the charge capacity of phase 3. Eventually if all phosphorus atoms are compensated phase 3 operates completely surface channel yielding $\text{SFW} = 0$ (indicated in figure).

Figure 9a illustrates, with two curves, the characteristics described above by plotting full well as a function of boron concentration. The first curve plots BFW characteristics for phases 1-2 and the second curve for SFW for phase 3. Charge capacity for the CCD is determined by the lowest full well curve shown. Optimum full well occurs when SFW for phase 3 equals BFW for phases 1 and 2, a condition that manufacturers attempt to achieve when fabricating MPP CCDs. Channel doping and drive also influence the optimum MPP implant employed, subjects discussed in considerable detail in Reference 2.

Figure 9b plots full well as a function of gate voltage (phase 3) for five MPP CCDs (shown dashed in Figure 9a). Consider sensor #1 first. When $V_g = -2 \text{ V}$ the full well is zero because the channel potentials are equivalent for all phases (i.e., MPP phase 3 is high at -2 V and phases 1-2 are low and pinned at -8 V). This clocking condition will occur when readout commences. Increasing the gate voltage results in greater charge capacity for phase 3 again during readout. At $V_g = 0 \text{ V}$ phase 3 holds more charge during readout than phases 1-2 during integration. Full well becomes limited by these phases exhibiting the flat response with increasing V_g as shown. SFW for phase 3 will eventually occur at $V_g = 8 \text{ V}$. At this point full well decreases as phase 3 is driven deeper into the SFW regime.

Now consider device #2 which employs more MPP implant. First note that full well = 0 when $V_g = -1 \text{ V}$, a shift of 1 V compared to device #1 because of the additional boron implant. Increasing the doping increases full well for phases 1-2 because

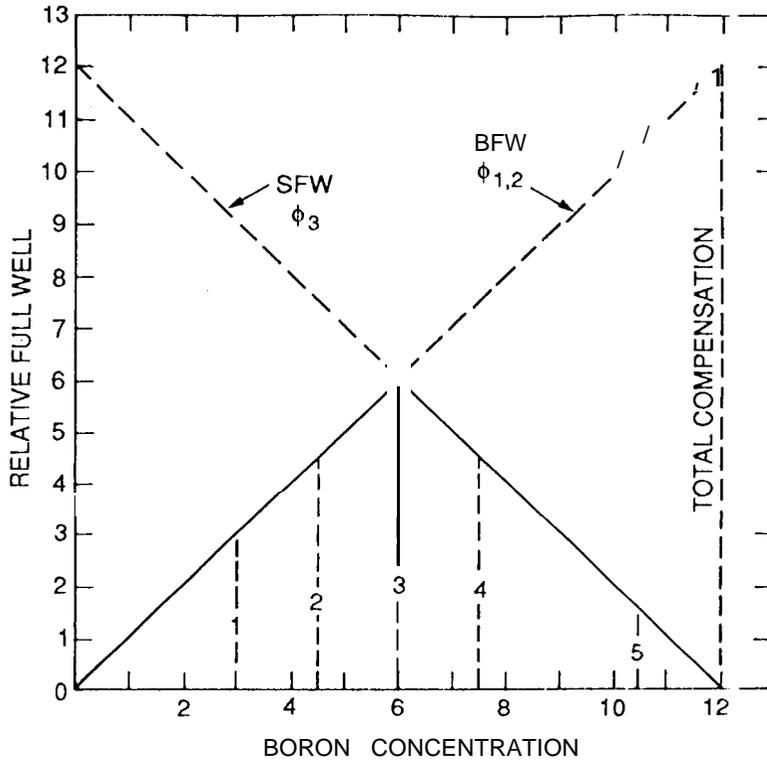
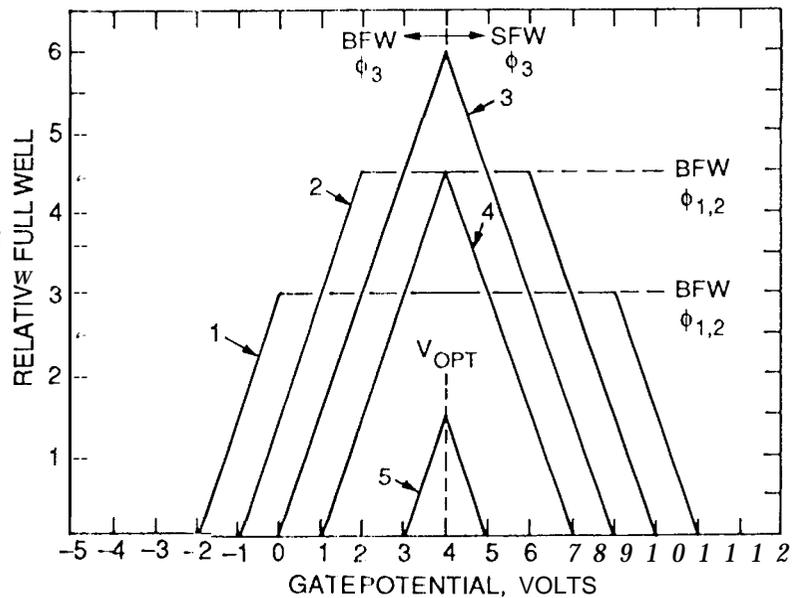


Figure 9a. Full well for a MPP CCD as a function of boron implant when clocked MPP. Optimum doping is achieved when the charge capacity under phases 1 and 2 during integration equals the charge capacity under phase 3 during readout. Doping beyond optimum results in surface channel operation for phase 3 and lower full well performance.

Figure 9b. Charge capacity as a function of gate voltage for phase 3 for five different MPP implants. The MPP implant for device 3 has been optimized to yield the greatest full well possible. Devices 1 and 2 are limited by the amount of charge that can be stored in phases 1 and 2 during integration. Devices 4 and 5, which have an implant greater than optimum, are limited by phase 3 and SFW during readout.



the barrier height increases under integration. SFW for phase 3 is offset by 1 V since more boron reduces SFW characteristics. Therefore, both phase 3 BFW and SFW curves shift towards V_{opt} by the same amount. The implant used for device #3 is optimum since $BFW = -SFW$ for phase 3. Devices #4 and #5 employ an implant dose that yields a full well level less than optimum (limited by SFW for phase 3).

3.3.4 MPP and PI clocking

Early MPP Cassini CCDs used a boron implant less than optimum, approximately $4.5 \times 10^{15} \text{ cm}^{-3}$ (optimum is $6 \times 10^{15} \text{ cm}^{-3}$ at 60 keV). MPP full well characteristics were therefore modest achieving only 30,000 e⁻ (compared to 80,000 e⁻ for an

optimum implant). However, when the CCD is clocked PI a significant increase in full well is measured, approximately 110,000 e⁻. However, this full well is less than a non MPP CCD clocked PI where 134,000 e⁻ is achieved. This behavior is typical for MPP CCDs. MPP well capacity is always less than non MPP devices when clocked PI. This is because the boron implant reduces SFW and BFW characteristics for phase 3.

Figure 10 illustrates full well characteristics for a non MPP CCD (sensor # 1) and three MPP CCDs (sensors #2, #3, and #4). Sensor #2 is a MPP CCD that incorporates an implant less than optimum. As discussed above, full well for the CCD is limited by the amount of charge that can be stored under phases 1-2 during integration when all phases are inverted. However, when clocked PI these phases are biased high allowing for much greater charge capacity. Under these conditions full well is determined by SFW and BFW characteristics for phase 3. The increase in full well is significant if the MPP boron dose is low (dotted line in Figure 10). The MPP implant for sensor #3 is optimum. PI and MPP clocking yield equivalent full wells. Sensor #4 dose is greater than optimum. Full well is dependent on SFW characteristics for phase 3. Hence, there is no advantage to implanting a CCD beyond optimum.

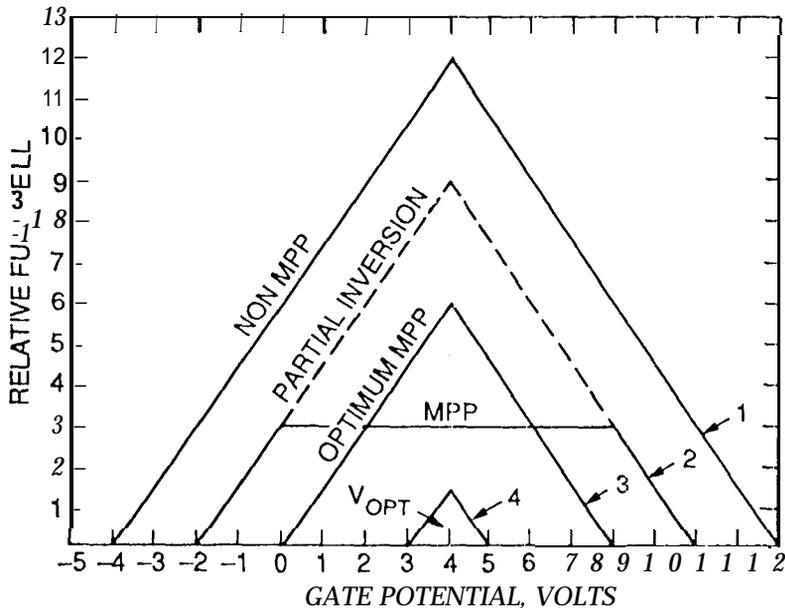


Figure 10. Well capacity as function of clock potential for a non MPP clocked PI (device #1) and three MPP CCDs (devices #2-4). Early MPP CCDs were processed similar to device #2 where well capacity is greater when clocked PI than when clocked MPP as shown. For the optimum MPP implant, PI and MPP clocking yield the same well capacity and full well curve. An implant greater than optimum also produces the same full well response but at a much reduced level. Note that all curves peak at V_{OPT} . This is because the MPP implant shifts the potential for BFW and SFW characteristics by the same amount.

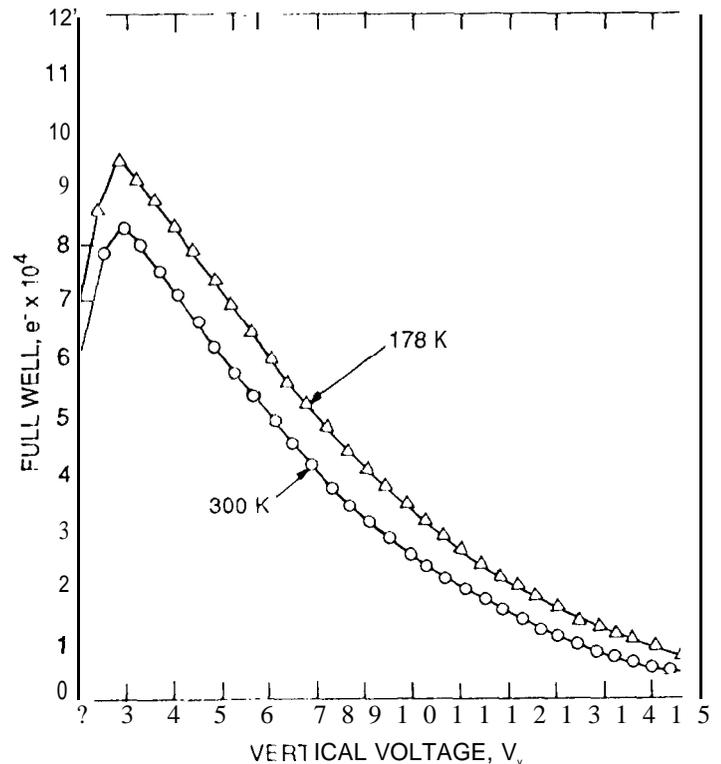
The Cassini MPP CCL exhibits optimum MPP full well performance, Figure 11 plots full well characteristics for the device as a function of gate voltage for two operating temperatures. Data was generated using MPP clocking, however, the same curves are generated when PI clocking is used for reasons given above. Note that full well increases when operating temperature is reduced. Full well in general is a temperature dependent variable. Strictly speaking, the onset of full well actually occurs before the channel potential equals that of the surface (SFW) or barrier phase (BFW). As charge collects in a potential well it naturally wants to come out. Two primary mechanisms are responsible for this action. First a repulsion force is generated between electrons that are collected. This field attempts to force carriers out of the well. Second, electrons also gain energy thermally (i.e., lattice vibration). The energy acquired is not the same for each electron but is described by Boltzmann's statistics. If the energy kick is large enough the electron can bloom over a barrier field. Electrons can acquire as much as 100 kT (2.5 eV) if sufficient time is given to acquire such energy statistically (hence full well is also time dependent). A similar process occurs when a CCD goes SFW. Here charge that collects near the surface (approximately 1000 Å) can thermally hop into the Si-SiO₂ interface region where the first signs of SFW appear.

For some applications it may be desirable to only introduce a small MPP implant barrier to preserve full well performance but still achieve the advantages of full inversion (although MPP full well will be modest). The user can command the camera to clock the CCD either MPP or PI. For low dark current generation and low signal levels MPP clocking would be advantageous. For high signals, requiring greater dynamic range, PI clocking could then be commanded.

The Sandbox CCDs will not include the MPP option for four reasons. First, dark current will not be an important factor since the CCDs will either be sufficiently cooled (e.g., -90 C operation for the Advanced Camera CCD) or readout quickly (e.g.,

30 frames/see for the Cinema CCD), both methods that suppress dark current to acceptable levels. Second, dynamic range is important especially for the 9-micron pixel devices. All CCDs will be clocked PI to achieve maximum well capacity. As described above, full well is sacrificed when MPP is implemented. Third, although low dark current generation is desirable for Advanced Camera and Pluto Flyby CCDs we anticipate (based on WF/PCII experiences) that radiation dark spikes will be generated when these CCDS go into space. Dark spikes will therefore limit dark current generation requiring cooling below -90 C. Fourth, MPP operation can severely limit how fast a CCD can be readout, an effect described below. This last factor is important to most Sandbox CCDS because they will be clocked at very fast rates in order to perform the frame transfer operation.

Figure 11. Full characteristics for the Cassini MPP CCD. This sensor was processed with an optimum MPP implant. Full well characteristics are the same whether the sensor is PI or MPP clocked. Well capacity is dependent on operating temperature as explained in text. At room temperature full well is 82,000 e- for the 12-micron, 3-phase pixel.



3.3.4 ESD protection networks

The discussion above shows the importance of driving the CCD with bipolar drivers to achieve optimum full well performance. Commercial CCDS often use protection diodes in parallel with clock lines to prevent electro-static damage (ESD). However, driving these diodes negative (relative to substrate) causes them to conduct resulting in a short circuit condition. This results in severe luminescence on the array (LED effect), not to mention the potential harm to the drivers and diodes. Also flight CCDS must pass a DC probe short test. For example, JPL flight CCDs require that poly to poly or substrate shorts <1 M ohm (ideally <10 M). This impedance test cannot be performed if diodes are present because the impedance of the diode would limit such measurements. Hence, for these two reasons ESD diodes are not employed for the Sandbox CCDs.

It has been often observed that when an ESD short does occur it is located at the edge of the array where poly lines drop from the field oxide region down into the active region (i.e., the interface of the p⁺ moat). It is this region where oxide fields are greatest when a high voltage spike is applied. An ESD short is typically not a dead short but a relatively high impedance leakage path where free carriers can be injected into the array. A bright column blemish or luminescence are signatures of a ESD short if the problem is associated with the vertical registers. Clock drivers normally can drive shorts of this type allowing the rest of the array to be readout normally.

The gates of the Sandbox CCDS are somewhat protected. The protection network consists of a small p⁺ moat in series with the aluminum bus line located near the bond pad. If a high voltage spike does appear damage will likely be induced in the network and not on the array. Hence, charge injection and luminescence will be minimized. Diffusions (e.g., V_{RFF} and V_{dd}) are nOT

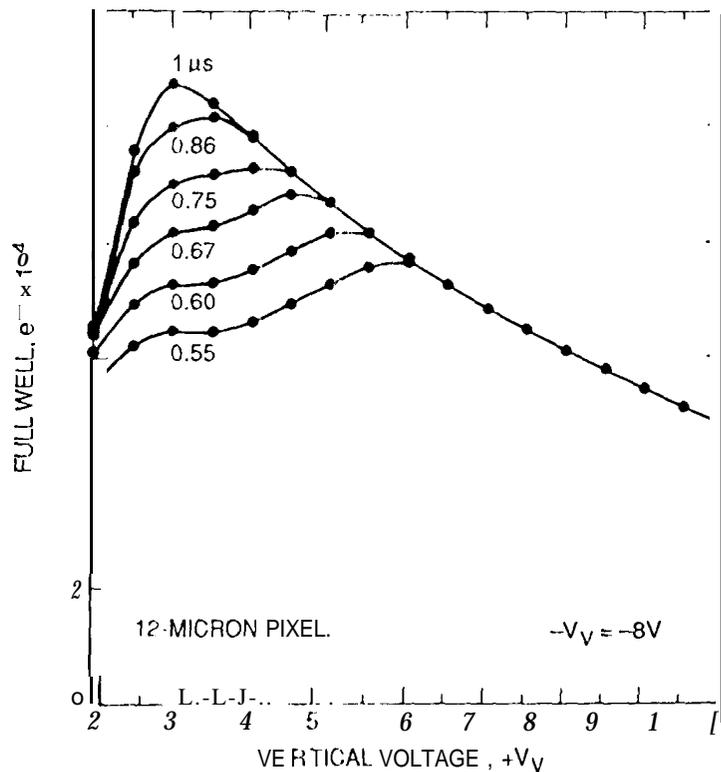
protected since they are not ESD sensitive (relatively speaking).

4. HIGHSPEED CLOCKING

The Pluto Flyby, Adapt 11 and Cinema CCDs will be clocked at a very high scan rate to perform frame transfer. The transfer time into the storage section will be performed 100 times faster than the longest integration time to suppress smearing. For example, the integration time for the Cinema CCD is approximately 1/30 of a second. Therefore, a frame transfer time on the order of 0.33 ms is required, a line transfer rate of 0.32 micro-sec to transfer 1024 lines.

A number of interesting limitations develop in the CCD when lines are transferred at this rate. First, well capacity decreases as transfer rate increases. Figure 12 plots well capacity for a 1024 x 1024 Cassini CCD as a function of clock potential ($+V_V$) with P1 clocking employed. A family of curves are presented for different line transfer periods (the shortest equal to 0.55 micro-sec). Data is collected in the following manner. The CCD is first erased of all charge. Then a 100 x 100 pixel region is illuminated at the top of the array (coordinates approximately 750 x 750). The illumination level is slightly greater than optimum full well. The CCD is clocked vertically 512 times with the line time indicated and data discarded. The remaining 512 lines, still in the array, are then clocked out slow-scan (20 ins/line at 50 kpixels/sec). The average signal level is then measured with a computer and plotted. As seen in the figure, well capacity is optimum for line transfer periods >1 micro-sec. This occurs at $+V_V = 3$ V and is where $BFW = SFW$. For shorter periods full well degrades and the optimum point moves to a higher clock potential.

Figure 12. Well capacity as a function of clock voltage and line transfer time for the Cassini imaging CCD. When line rates become faster than 1-micro-sec the full well curve begins to change shape as demonstrated here. Clocked too fast causes charge to bloom backwards from transfer direction. Optimum full well occurs at a higher clock voltage at a reduced level. Charge packets less than full well can be transferred at the speeds indicated without difficulty.



Degradation of full well observed in Figure 12 is attributed to fringing fields between phases (refer to top illustration in Figure 13). Fringing fields play an important role in transferring charge. Without these fields charge only moves by thermal diffusion aided by self repulsion. Fringing fields are greatest when the potential wells are empty. As charge collects the potential difference between phases decreases resulting in smaller fringing fields. It is for this reason why it is easier for the CCD to transfer a smaller charge packet than a large one. As full well is approached fringing fields essentially disappear. Under full well conditions extra time must be given to allow charge to thermally diffuse from phase to phase. If the clocking rate is too fast charge will bloom backwards as illustrated in the lower illustration of Figure 13. Figure 14 presents three column traces for the CCD characterized in Figure 12 demonstrating that charge always blooms opposite to transfer direction when the CCD is clocked too fast. Charge moves from right to left in figure.

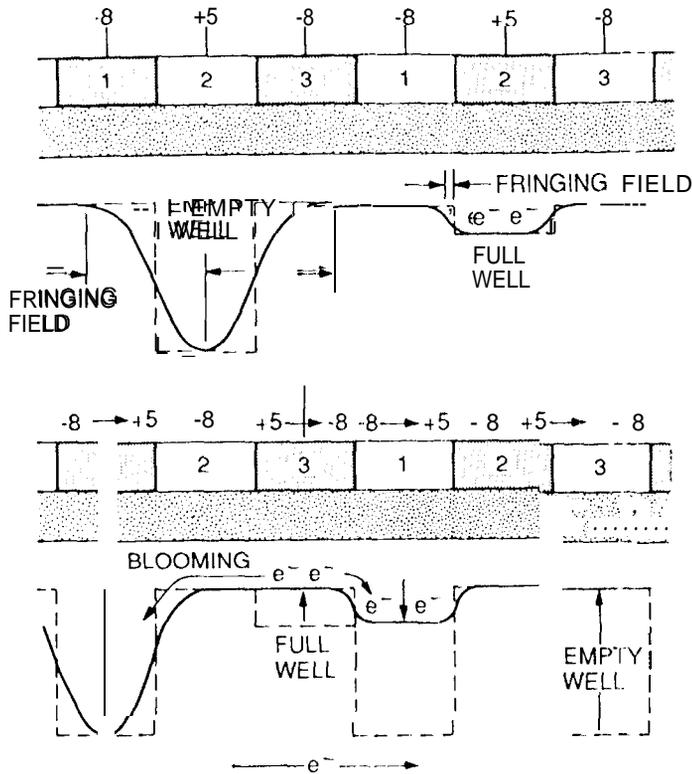
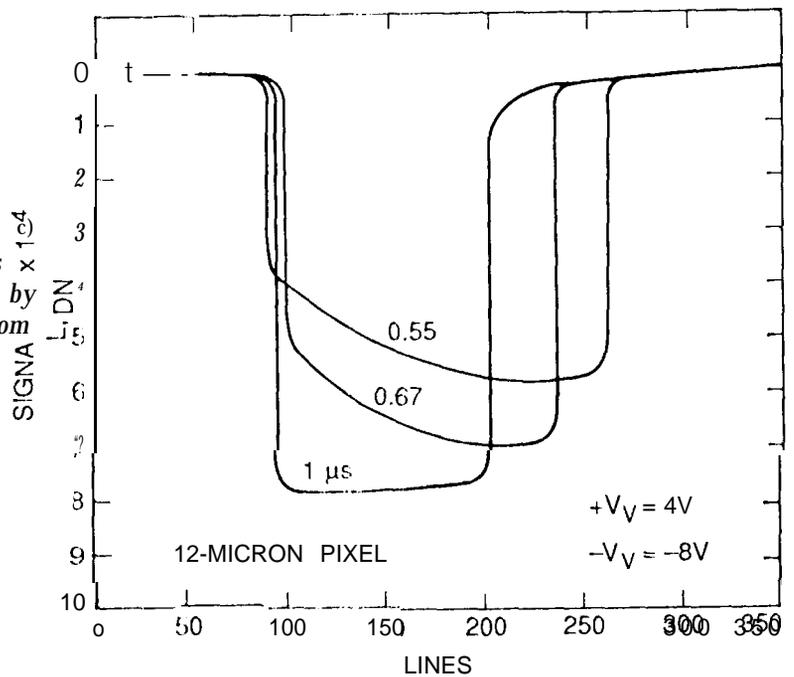


Figure 13. Top illustration shows relative fringing field strength for an empty and a full potential well. When a well is filled with charge the potential difference between the collecting phase and barrier phase is much smaller compared to when it is empty. This reduces the electric fields between them. Charge that remains in a collapsing phase that was full must primarily transfer by thermal diffusion and cannot rely on fringing field. Smaller charge packets receive the benefits of fringing fields, the reason why they can be transferred much faster. The bottom illustration shows why blooming occurs if the CCD is clocked too fast. Charge that remains in a collapsing phase blooms backwards.

Figure 14. Data taken from the same CCD as Figure 12 showing that blooming caused by high speed clocking is always backwards from transfer direction. Vertical clocks switch from -8 V (inverted) to +4 V.



Fringing fields can be increased by elevating the clock potential (i.e., V_V). Full well will increase initially until SFW is reached at which point it then decreases. This effect is observed in Figure 12. Note also full well characteristics are independent of clock rate when SFW limited.

Figure 15a is an x-ray response exhibiting perfect CTE for a line transfer rate of only 200 ns. The charge packets transferred are very small (1620 e-). As Figure 12 shows CTE should be well behaved when charge packets this size are transferred. PISCES modeling programs predict that CTE will become limited for line times of a few nano-seconds for the CCL) tested. Unfortunately it is very difficult to generate three phase clocks this narrow to verify this prediction. For signals of this magnitude CTE is not limited by the CCL) but by the clock drivers.

Figure 15b shows an x-ray response when the horizontal clocks are only switched from -0.5 V to + 0.5 V. Fringing fields under these clocking conditions are very small. CTE is well behaved as long as the clocks are slow (less than 1 M pixel/sec).

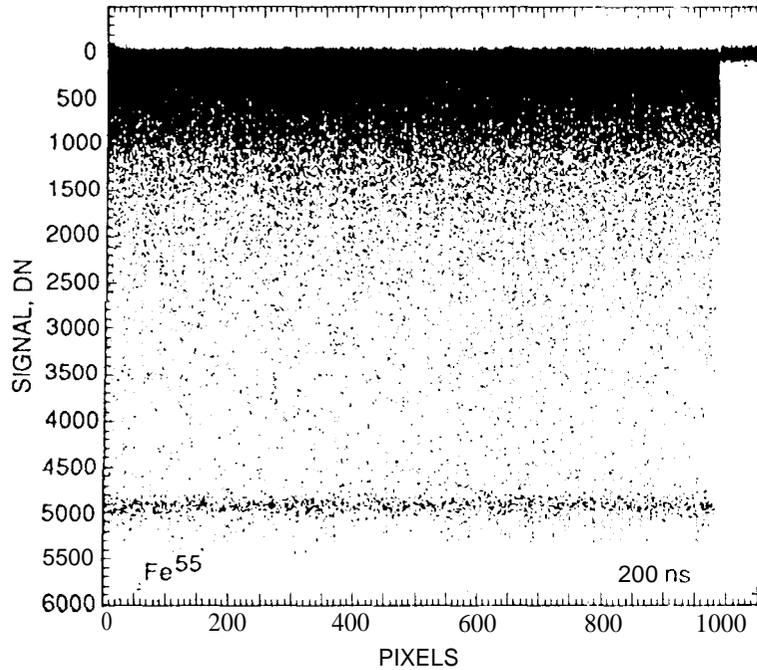
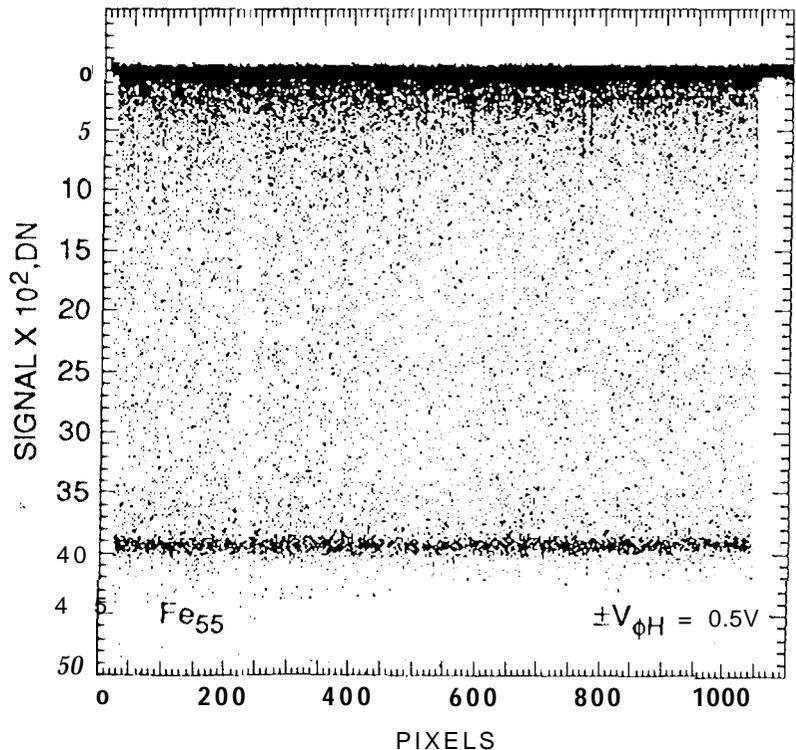


Figure 15a. HCTE Fe-55 x-ray response for the Cassini CCD. Ideal VCTE is demonstrated. Lines are transferred at 200 ns, much faster than the rates tested in Figure 12. In that the maximum charge level is only 1620 e- fringing fields are primarily responsible for transferring charge. Theory indicates that line times ten times faster than this are possible in transferring x-ray events this small.

Figure 15b. HCTE Fe-55 x-ray response for the Cassini CCD. In this test the horizontal clocks only swing 1 volt. This effectively reduces the fringing fields and transfer speed. Data was collected at 50 kpixels/sec using 8 micro-see to make a pixel transfer. Rates faster than 0.1 M pixels/sec will result in degraded CTE performance. Increasing the clock swing amplitude allows faster transfer rates.



The data shown in Figure 12 was generated for a three-phase 12-micron pixel allocating 4 microns/phase. It is more difficult to transfer charge when pixel dimensions increase in size since fringing fields are less influential in the center of a phase (for an empty well a fringing field may extend a couple microns into an adjacent phase). Figure 16a plots well capacity for a 15-micron pixel CCD (1024 x 1024, 3-phase CCD). Note that full well begins to degrade for a longer line transfer period compared to a 12-micron pixel. Figure 16b shows full well characteristics for a 7.5-micron pixel (800 x 800, 3-phase). Charge transfer for this CCD is much faster. Full well reduction does not take place until the line time is shorter than 300 ns. Figures 12, 15 and 16 show that CCD speed is limited by pixel size and charge level transferred.

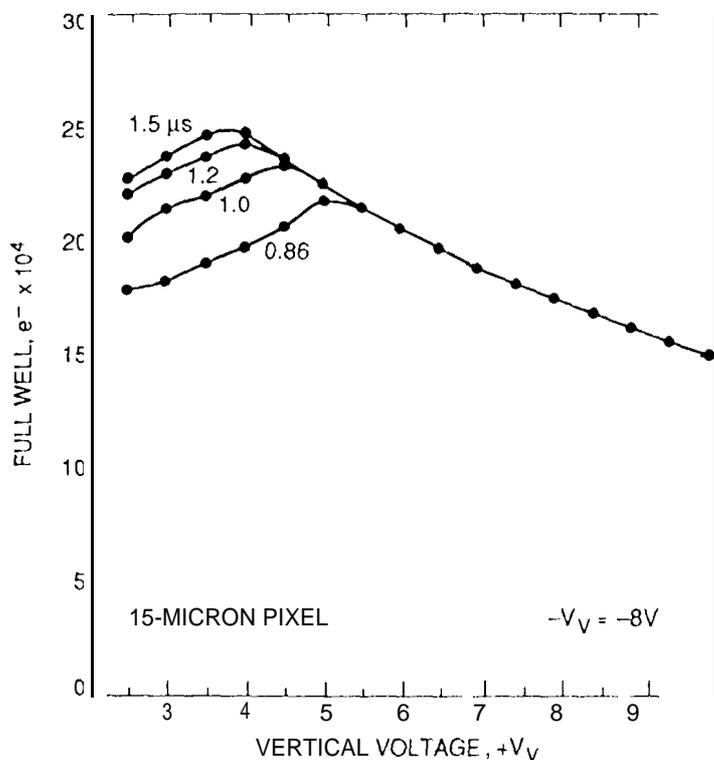
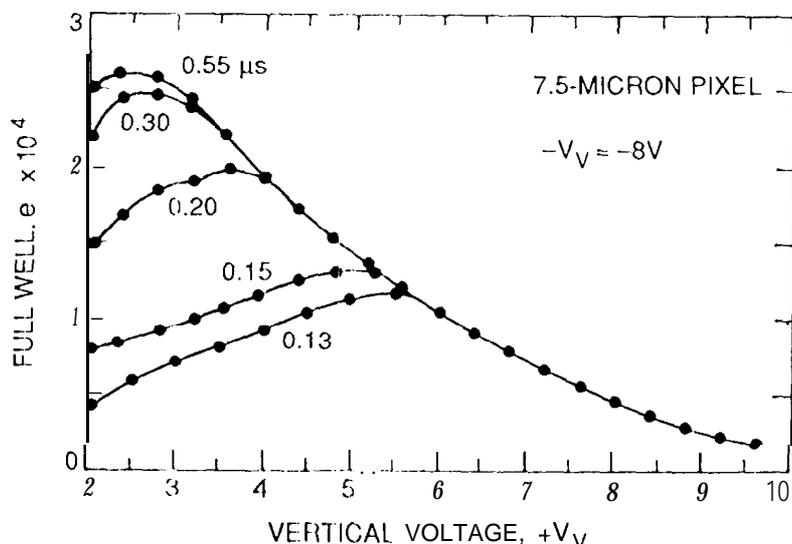


Figure 16a, High speed full well curves generated by a 800 x 800, 15-micron pixel WF/PC II CCD. Note that full well degrades for a longer line time compared to Figure 12 (generated for a 12-micron pixel device). Fringing fields only extend into a neighboring phase by a couple microns when the phase is empty. When the gate length is increased the fringing field strength at the center of the phase is reduced, Charge there must transfer by diffusion increasing line time requirements.

Figure 16b. High speed full well curves generated by a 7.5-micron pixel WF/PC II CCD. Note that the full well curve does not begin to change shape until line times shorter than 0.55 micro-see are tested. The gate length for this CCD is small (2.5-microns) resulting in strong fringing fields at the center of a phase resulting in greater speed. High speed CCDs are typically small pixels devices unless multiple phases are used to shorten gate length.

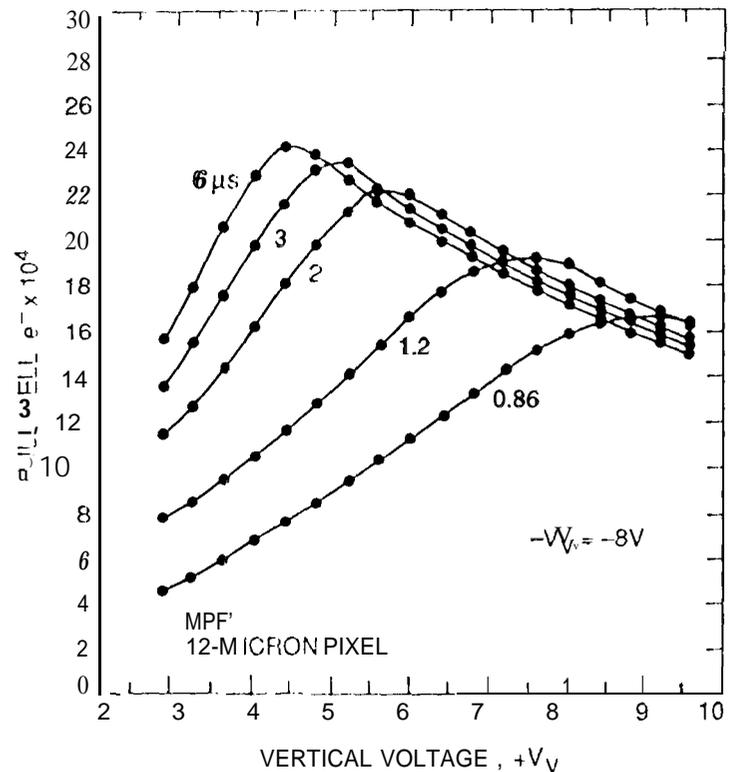


MPP CCDs clocked fast-scan typically exhibit CTE problems. The difficulty has been traced to the MPP implant itself. During high temperature processing the MPP implant encroaches under adjacent phases (i.e., phases 1 and 2). This effect decreases the potential at the edges of these phases generating a small but influential potential barrier to electrons. When phase 3 is empty

these barriers are overwhelmed by fringing fields and charge transfer is well behaved. However, as signal electrons are collected the fringing fields collapse and the barriers become apparent making it more difficult to transfer charge. Therefore, the full effect of this problem becomes present at full well conditions where fringing fields are smallest. Charge can only escape over the barriers by thermal diffusion. Since the potential associated with the barriers are probably many times greater than kT/q , significantly more transfer time is required compared to CCDs without MPP.

Figure 17 shows full well characteristics for a 12-micron pixel MPP Cassini CCD. Note that transfer speed is significantly reduced compared to the Cassini CCD characterized in Figure 12 without MPP (for the same pixel size). In fact, optimum full well is never achieved for the longest transfer times tested. For this reason alone MPP technology is not incorporated in the Sandbox CCDs because transfer times less than 1 micro-sec are required.

Figure 17. High speed full well curves generated by a Cassini MPP CCD (12-micron pixel). Note that the curves are considerably different than the full well curves shown in Figure 12 for a non MPP CCD. As the text explains, the MPP implant slows down transfer time. Line transfer periods > 10 micro-sec are required before full well characteristics stabilize. Vertical pixel summing in the horizontal register is used to readout the CCD yielding full well figures approximately three times shown in Figure 11 (data collected at 300 K).



The responses presented in Figures 12-17 were generated by relatively small CCD arrays (i.e., $< 1024 \times 1024$). When larger arrays are characterized another high speed effect comes into play. Using the same testing sequence as described above, Figure 18 plots full well characteristics for a Loral Fairchild 2048×2048 , 1 f-micron pixel MPP CCD tested at two line times (30, and 6 micro-sec). Also two regions of the CCD are interrogated, the center and edges of the array (indicated by "C" and "E"). Note that full well characteristics for the center of the CCD are worse than the edges. This is because the narrow clocks applied do not make it to the center of the array properly. The poly resistance of the gate electrodes and associated capacitance reshapes the clock reducing its amplitude (specifically the positive level since the negative side is driven deep into inversion). Although one can increase the clock voltage to reoptimize the center region of the CCD the edges would be driven into SFW. Each column of the CCD therefore has a different full well signature and optimization curve.

Figure 19 is a horizontal line plot for the same CCD characterized in Figure 18. The device is stimulated with a slant bar target in the region covering $1850 (H) \times 2048 (V)$ pixels and driving it at 10 nline-sec/line (again using the same testing sequence described above but using a slant bar target). Ideally a flat response should be observed at the full well level indicated. However, as we move towards the center of the device full well decreases because of the poly resistance effect. Curiously there is an "extra dip" in full well at the left side of the chip, in this location there is a high impedance gate short associated with a single pixel. This short effectively lowers that gate voltage at the site and surrounding regions (the CCD is driven from both sides of the array). At slow-scan rates this problem is not apparent but becomes obvious for line rates < 30 micro-sec/line.

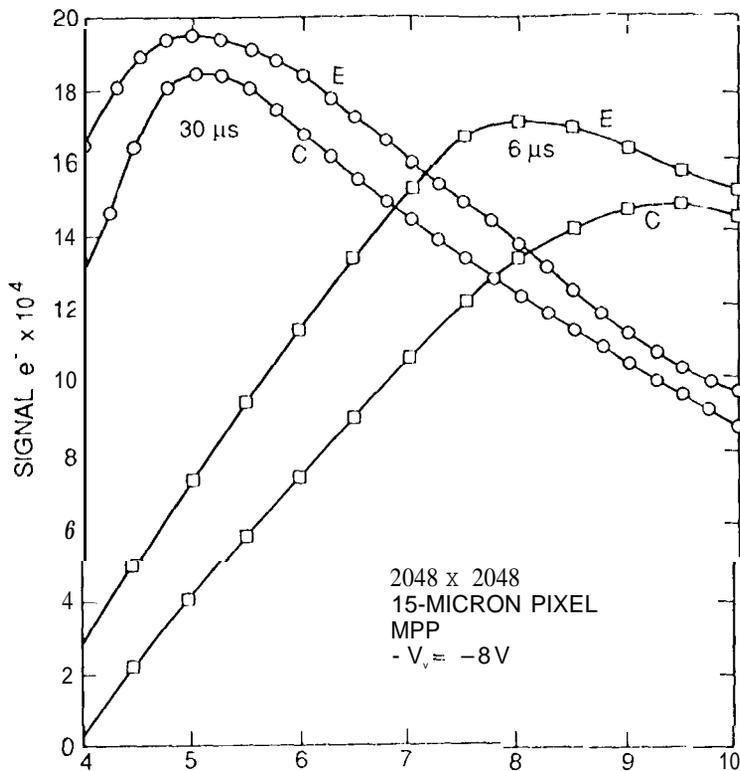
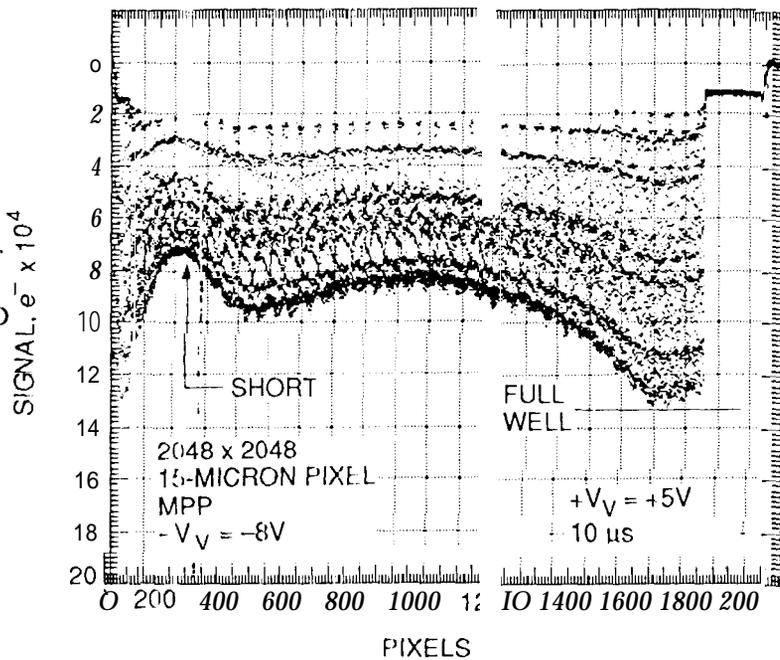


Figure 18. High speed full well curves generated by a 2048 x 2048, 15-micron pixel MPP CCD. Data is taken at the edge of the array (labeled "E") and the center of the array (labeled "C"). The edge is primarily limited in speed because of the MPP implant and the relatively large gate lengths employed (5-microns). Line transfer periods greater than 30 micro-see arc required to deliver optimum performance. The center of the array exhibits an additional problem caused by the long gate electrodes that feed the array. The poly resistance and capacitance associated with the gates results in a distributed R-C filtering effect that reduces clock amplitude and full well performance.

Figure 19. A slant-bar stacking response generated by the CCD tested in Figure 18. The vertical clocks swing from -8 V (inverted) to +5 V using a 10 micro-sec line time. These set of conditions limit full well performance over the array (refer to Figure 18). Note that full well decreases towards the center of the CCD because of the R-C clock filtering effect. In addition, a high impedance short is found on the left hand side of the array which perturbs the clock amplitude limiting speed in this location,



In summary, the CCD characterized in Figures 18 and 19 exhibits four high speed difficulties: (1) the fringing field problem; (2) the MPP barrier problem; (3) the poly resistance/capacitance problem and; (4) a high impedance gate short problem. The first difficulty results in blooming over the entire array and depends on pixel size. The second effect also causes similar blooming characteristics but is only associated with MPP devices. The third difficulty causes a shift in the full well curve towards a higher gate voltage when moving towards the center of the chip. The fourth difficulty is a localized problem and depends on the severity of the short.

The Sandbox CCDs were designed and will be processed to minimize these problems as much as possible. First, as mentioned above, MPP technology will not be employed. Second, either small pixels (e.g., 9-micron pixels for the Cinema CCD) or multiple phases (e.g., six phases for the Adapt 11 and Mach 11 CCDs) are used to increase fringing field strength. Third, aluminum bus lines are designed into the array to reduce the poly resistance/capacitance problem. For example, the Cinema CCD uses aluminum bus lines that are brought into the array every 256 columns and are strapped to the poly lines to reduce poly resistance. The fourth problem will be screened through testing.

S. QUANTUM EFFICIENCY

5.1 Introduction

To achieve the highest sensitivity possible, the Advanced Camera and Big-CIT CCDs will be thinned and illuminated from the backside. This technique avoids the problem of photons being absorbed and lost in the frontside gate structure. Thinning also improves sub-pixel QE uniformity.

5.2 Advanced Camera CCD

Thinning will be performed by EG&G Reticon by standard techniques of chemical etching. Prior to thinning, the CCDs will be bonded to, and supported by, a glass substrate that covers and extends slightly beyond the pixel array. An unthinned border outside the pixel array will allow bonding of wires to the bond pads. The supporting substrate is necessary to strengthen the CCD to avoid damage during ground handling and launch, and to ensure flatness.

Thinning leaves a free silicon surface that oxidizes on the backside, leaving an accumulation of positive charge at the Si-SiO₂ interface. This charge creates a potential well at the back surface which traps photo-electrons, preventing them from reaching the frontside potential wells. This effect significantly reduces QE performance for photons that do not penetrate deeply into the silicon (i.e., short wavelength photons). Also the QE varies (i.e., hysteresis) when signal charge is collected in the backside well. This highly undesirable characteristic can be alleviated by a number of different passivation methods (e.g., backside charging, flash gate, biased flash gate, ion-implantation). For the Sandbox CCDs we will accumulate the backside using molecular beam epitaxy (MBE) delta-doping (Ref. 4).

The delta-doping method utilizes MBE to form a uniform and stable 1/3 monolayer of passivating boron atoms, on a 1-nm thick MBE grown silicon lattice both residing on the backside surface of the CCD. A thin layer of silicon is then grown on top of the boron layer. Advantages of the MBE approach are: (1) the boron layer can be precisely targeted to lie at a depth such that very strong electric fields are generated at the immediate surface that accelerates signal electrons to the frontside; (2) passivation over the area of the CCD is highly uniform; and (3) the boron atoms replace silicon atoms without distorting or damaging the silicon crystalline structure, so that annealing is unnecessary (required for ion-implantation). This technology achieves the "QE pinned" condition achieving 100 % internal QE. More-over the QE is uniform and stable over periods of many years (likely indefinitely).

An AR coating of SiO will be applied to the silicon surface to reduce reflection loss in the visible spectrum. The AR coating is expected to increase the overall QE of the device by a factor of about 1.4 in the visible wavelength range compared to noncoated CCDs.

High sensitivity for the Advanced Camera CCD must extend over a broad wavelength range (100-11,000 Å). Unfortunately an efficient AR coating to cover this range has not been developed into the far UV. Therefore, a phosphor (lumogen) coating is used, the same coating that is used on the WF/PC 11 and Cassini CCDs. The phosphor works by absorbing short wavelength photons (<4800 Å) and re-emitting them at visible wavelengths (5400 Å for lumogen). The phosphor and AR coatings work together to enhance performance across the entire wavelength range and permits the CCD to be optimized for visible wavelength sensitivity. At visible wavelengths, where the phosphor is transparent, the AR coating enhances QE in the conventional way. In the UV and EUV, the phosphor absorbs photons and re-emits them at a wavelength where the AR coating is optimized (i.e., 5400 Å).

The photon re-emission for the phosphor is geometrically isotropic, so that half the re-emitted photons are directed away from the CCD. Thus, at best the QE in the region where photons are absorbed by the phosphor (100-4800 Å) is one-half the QE where the photons are re-emitted (5400 Å).

Figure 20a presents an experimental QE plot generated by a backside illuminated WF/PC 11 CCD using the thinning and accumulation recipe described above. The CCD was thinned to approximately 8-microns which essentially thins the backside to the frontside depletion edge (the sensor is fabricated on 30-50 ohm-cm silicon). Note that the sensitivity below 4800 Å is essentially flat and is approximately half the QE achieved at 5400 Å. Also plotted in Figure 20a is a theoretical QE curve generated with an AR coating but without a lumogen layer. The parameters used best describe the WF/PC 11 CCD (7-microns of depleted material, 1-micron of field free material, QE-pinned, and 550 Å of SiO₂). Note that sensitivity for the experimental CCD is lower than theory between 3000-6500 Å primarily due to the lumogen layer and associated isotropic problem discussed above. However, below 3000 Å sensitivity is greater because of reflective and absorption loss related to the AR coating. Lumogen remains high (down to approximately a wavelength of 500 Å at which point the phosphor becomes transparent).

Also note that theory and experiment differ in the near IR. There are two possible explanations for this observation. First, the device may be slightly thicker than 7-microns resulting in slightly higher QE longward of 7000 Å. Second, the QE model employed (Ref. 5) does not include a reflection component at the frontside surface. That is, when near IR photons pass through the CCL some photons are reflected back from the front and make a second pass through the membrane again. This effect would increase sensitivity. In fact multiple passes result in fringing for the device always seen in the near IR for rear-illuminated CCDs.

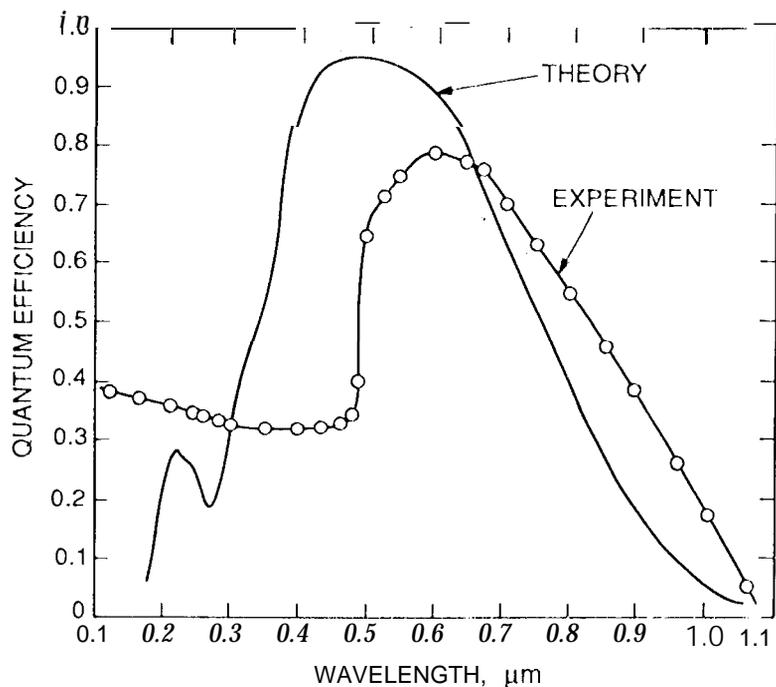


Figure 20a. QE curve generated by an experimental backside illuminated, MBE accumulated, SiO₂ AR coated, lumogen phosphor coated, WF/PC 11 CCD. The AR coating thickness was adjusted to yield the highest QE possible at 5400 Å, the wavelength where lumogen fluoresces. The sensitivity in the UV (< 4600 Å) is approximately half of the QE achieved at 5400 Å. The theoretical QE curve shown uses parameters that best describe the CCD without a phosphor coating. Note the sensitivity is very poor shortward of 3000 Å where the AR coating becomes opaque. For this reason a phosphor coating is used on some Sandbox CCDs for extended response into the far UV. Lumogen responds to 500 Å where at this wavelength becomes transparent.

It is important that the Advanced Camera be thinned and backside illuminated because of the 9-micron pixel size employed. Figure 20b shows frontside QE responses for the Cassini and WF/PC 11 CCDs in the far UV (both CCDs are coated with 6000 Å of lumogen). The response for the Cassini CCD drops at 1800 Å where the quartz window above the CCD becomes opaque. Similarly the WF/PC 11 response degrades below 1500 Å where a MgF₂ window becomes absorbing. Note the QE for the Cassini CCD is lower than the WF/PC 11 device. The difference is because the WF/PC 11 pixel is 15-microns whereas the Cassini CCD is 12-microns. As the pixel dimensions shrink in size the gate overlaps become a greater portion of the pixel decreasing sensitivity. A gate overlap of 1-micron is used for all CCDs. Projected frontside UV QE for a 9-micron pixel is only 6% considerably lower than the WF/PC 11 CCD (14%). Hence, thinning is required if the Advanced Camera CCD is to outperform the WF/PC 11 CCD. Figure 20a shows that QE will be in excess of 30%.

5.3 CIT CCD

The Big CIT will be thinned and processed in the same fashion as the Advanced Camera CCD except that the lumogen layer will not be deposited. The CCD will be used in ground-based astronomical applications, and therefore, UV sensitivity only needs to be high to 3000 Å (the wavelength where the atmosphere cuts off). The expected QE for the CCD will follow close to the theoretical curve shown in Figure 20a (the AR coating will be slightly thinner to boost UVQE performance with some sacrifice in the visible).

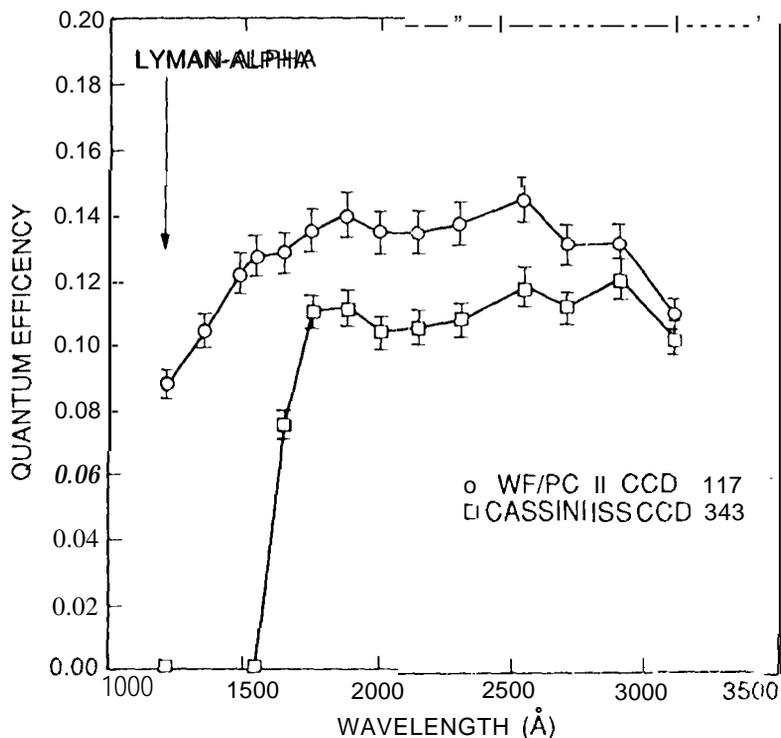


Figure 20b. Experimental QE plots generated by a WF/PC II and Cassini frontside illuminated lumogen coated CCDs. The WF/PC II response is higher because the pixel is larger than the Cassini CCD (15-microns compared to 12-microns). Gate overlap (approximately 1-micron) between phases becomes a greater percentage of pixel area for smaller pixel devices reducing QE at 5400 Å. For small pixel (<12-microns) devices that are coated with a phosphor this effect becomes important requiring thinning and backside illumination.

6. READ NOISE

Curiously, read noise for the CCD is still limited to more than $1e^-$ rms for slow-scan operation. Some CCDs exhibit noise floors as low as $1.5e^-$ slightly better than the first lightly doped drain (LDD) CCDs fabricated several years ago. Flicker ($1/f$) noise generated by the on-chip amplifier limits read noise. Many theories have been presented to explain where $1/f$ noise is actually generated in the output MOSFET. One popular theory is that carriers that make up the drain current tunnel between the buried channel and surface states primarily near the source of the MOSFET. Presumably, the trapping and detrapping of charge at the interface is the noise voltage associated with $1/f$ noise. Although this theory may be correct a solution to eliminate $1/f$ noise is not forthcoming. Nevertheless, $1/f$ noise has been reduced compared to MOSFETs fabricated in the past by improved surface passivation techniques (the corner frequency for $1/f$ noise is approximately 50 kHz at room temperature). It now appears that a $1/f$ limit has been reached, and therefore, we must live with $1/f$ noise and remain slightly above $1e^-$.

Floating gate technology has allowed the CCD to circumvent the $1/f$ noise problem by reading pixels nondestructively (amplifiers of this type are called Skipper amplifiers). Multiple samples of a pixel are averaged together to improve noise performance (noise is reduced by the square-root of the number of samples taken). The technique is very effective and has allowed noise levels of $0.3e^-$ rms to be achieved thus breaking the $1e^-$ barrier. For best results the CCD video signal is processed using the technique of correlated double sampling (CDS). An optimum sample-to-sample time is found for best S/N depending on spectral noise characteristics of the output amplifier (i.e., white and $1/f$). We generally find for today's CCDs that when sample times > 4 -micro sec that correlation $1/f$ noise frequencies begins to be lost. At this point read noise does not decrease by the square-root of sample-to-sample time because of $1/f$ noise skirt. Therefore, multiple samples are taken using

a sample period of 4-micro sec.

The general trend for reducing read noise at the manufacturer has been to increase the sensitivity of the output amplifier (i.e., e^-/V) without significantly increasing white and $1/f$ noise. This has been accomplished by primarily reducing gate capacitance of the output amplifier. This is accomplished by reducing its size and using LDD technology. Although $1/f$ and white noise has increased slightly in the optimization process the net noise (in rms e^-) has been reduced due to the sensitivity increase. Sensitivity is approximately 4 micro- V/e^- for 2-3 e^- amplifiers, about a factor of 10 times higher compared to the WF/PC 1 CCD which exhibited a read noise of 13 e^- rms. Increasing the sensitivity any more than this results in a significant $1/f$ and white noise increase and a corresponding increase in read noise.

As mentioned above, read noise for high performance floating diffusion CCD amplifiers is about 2 to 3 e^- rms. Skipper amplifiers typically require between four to nine samples/pixel before a 1 e^- noise floor is achieved. Two Sandbox CCDs (Adaptive Optics and Advanced Camera) will utilize Skipper amplifiers. The current WF/PC 11 CCD is achieving 4-5 e^- (about 3 times better than the WF/PC 1 CCD). The Advanced Camera CCD employs two floating diffusion amplifiers for single sampling that should yield 2-3 e^- improving noise by a factor of 1.5 or more. The device also employs two Skipper amplifiers for improved noise performance if desired.

The sensitivity improvement has resulted in a side problem related to linearity. As the sensitivity increases the voltage swing on the gate of the output MOSFET increases. This swing can be quite large if the CCD is used over its full dynamic range. For example, the Cassini CCD exhibits a sensitivity approximately 4 micro- V/e^- and a well capacity of 134,000 e^- thus swinging the gate by -0.54 V. This voltage variation results in a nonlinearity because the gate bias point for the amplifier shifts slightly to a new gain level. The Cassini CCD is limited to approximately 130,000 e^- before a nonlinearity of 1 % sets in. The on-chip amplifier therefore exhibits a dynamic range of its own bounded by a linearity requirement (the dynamic range for the Cassini output amplifier is approximately 26,000 assuming a read noise of 5 e^-). Nonlinearity is not a problem for the 9-micron pixel Sandbox CCDS because full well is less than the Cassini CCD (approximately 60,000 e^-). The amplifiers are nearly identical in size and input capacitance.

The Cinema CCD uses a three-stage output amplifier for high speed operation (Figure 1 a). The first stage MOSFET is extremely small in size and will exhibit high sensitivity (> 8 micro- V/e^-). Because of its size the amplifier will exhibit a high $1/f$ noise cut-off frequency. However, the horizontal register will be read out a approximately 8 Mpixels/sec requiring a sample-to-sample time < 50 ns. Therefore, $1/f$ noise will be correlated and removed by CDS. The second and third stages are used to increase bandwidth and drive characteristics.

7. 10 NIZINC; RADIATION DAMAGE

7.1 Introduction

This section briefly discusses some new concerns in reference to ionizing radiation damage for the CCD. Much could be said about this field of study because it is still unfolding. Discussions given in this section are important to the Advanced Camera and Pluto Flyby CCDS because they will be used in space where high energy radiation sources are found.

7.2 Full Well

Figure 21 shows a full well plot generated by a Cassini MPP CCD before and after being irradiated with 6 krad of CO-60 gamma-rays. A significant full well loss is observed considering the device was exposed to such a small amount of radiation. Also note that the optimum full well point shifts towards a higher gate voltage (2.2 V to 3.8 V), opposite to the expected direction. Flat-band shift is always negative for CCDS because radiation induces positive charge in the gate oxide. For example, a flat-band shift of -0.6 V was measured for this CCL). These peculiar results are now explained.

Figure 22 shows a cross-section view for the Cassini MPP CCD looking up the signal channel. The region where the channel stop and signal channel converge is referred to as the "birds beak" region. The field oxide over the channel stop region is approximately 20 times thicker than the gate oxide. During irradiation the field oxide absorbs more radiation than the gate oxide. In turn the flat-band shift in the field oxide region is greater than compared to the middle of the channel.

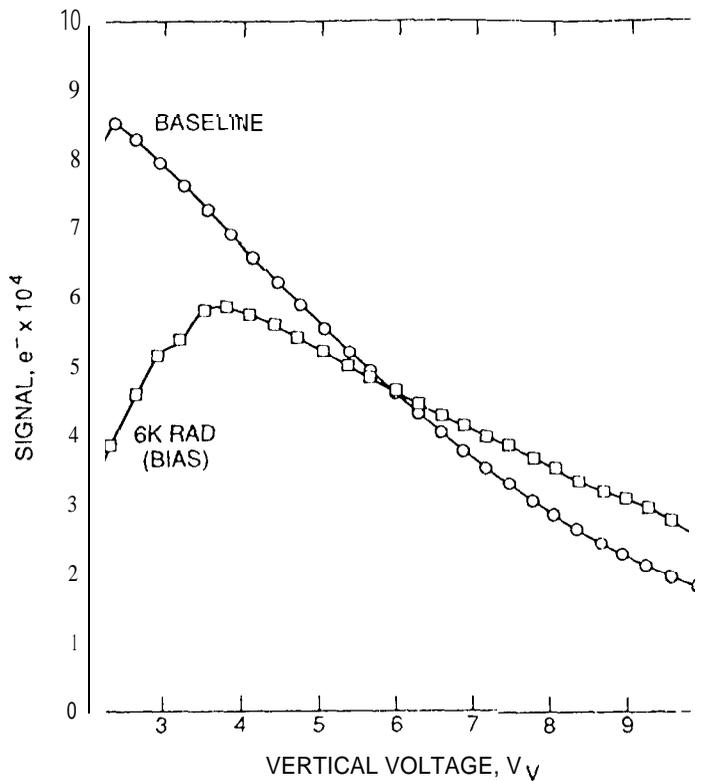


Figure 21. Full well characteristics for a MPP Cassini CCD before and after being irradiated with 6 krad of 2 MeV gamma-rays. Full well degrades because of a significant flat-band shift that develops near the channel stop region as discussed in the text. The device was biased during irradiation which intensifies the problem.

Figure 22. Cross-sectional view of signal channel and "birds beak" region. Field oxide above the channel stop captures more incident radiation resulting in more damage in the region. As a result, the flat-band shift is greater causing the potential to change more relative to the center of the channel. This effect significantly influences BFW and inversion characteristics for the CCD.

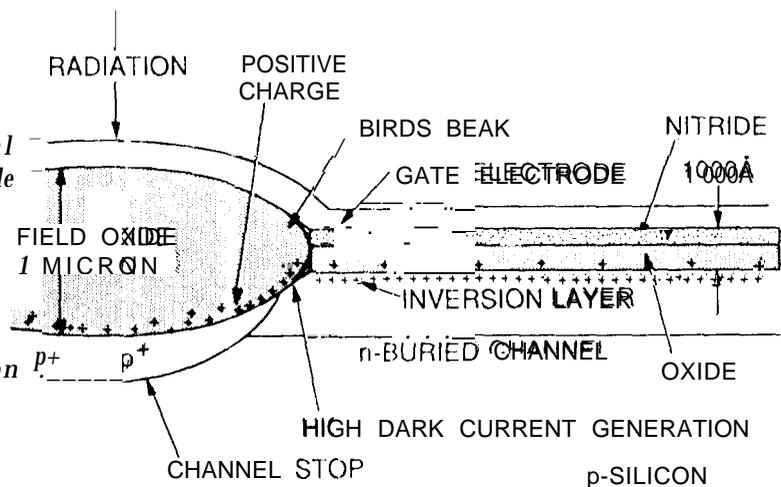


Figure 23 demonstrates the magnitude of shift that occurs in the birds beak region after the CCD is exposed to a small amount of radiation. Figure 23a plots dark current as a function of $-V_v$ when the gates to the upper half of the array are grounded during irradiation. Figure 23b is a similar plot except that the lower half of the array is biased at -9 V (the CCD is designed as a frame transfer device so split bias during irradiation is possible). A baseline response is shown in both figures before irradiation. These responses show that the inversion point occurs approximately at $V_v = -6.0$ V. After irradiation the inversion point shifts due to positive charge build-up in the oxide. The shift is significant for the hissed portion of the CCD (for reasons explained below). The shift in both cases is much greater than the flat-band shift related to the channel itself (-0.6 V).

Knowing these effects we return to the full well issue presented in Figure 21. Figure 24 presents PISCES potential diagrams for the Cassini MPP CCD. The top diagram plots the channel potential for a non MPP phase beginning in the center of the channel (labeled $x=2.6$ microns) and moving towards the birds beak region ($x=0$). The analysis assumes a flat-band voltage of zero volts (i.e., pre-irradiation) and a gate potential of -8 V. Note the channel potential is maximum in the center and collapses

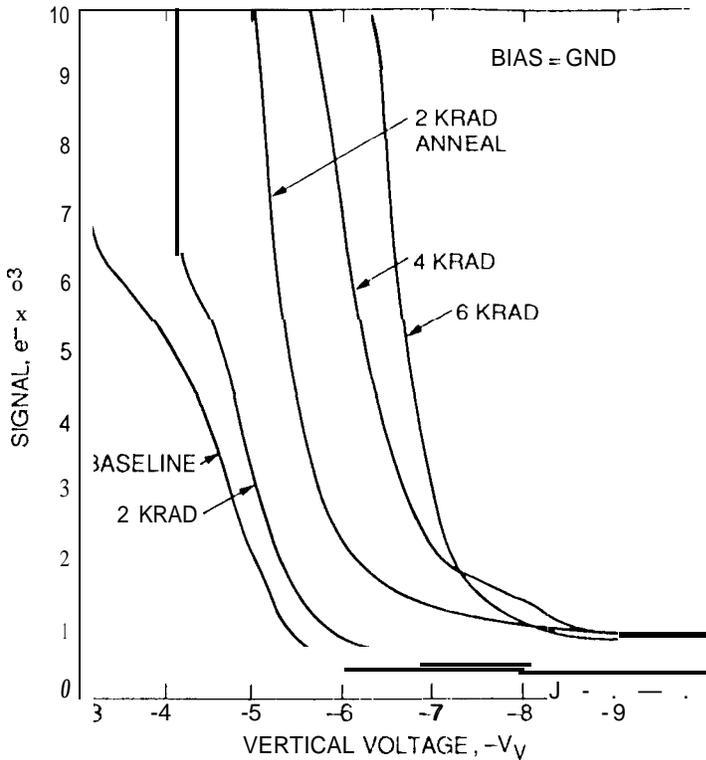
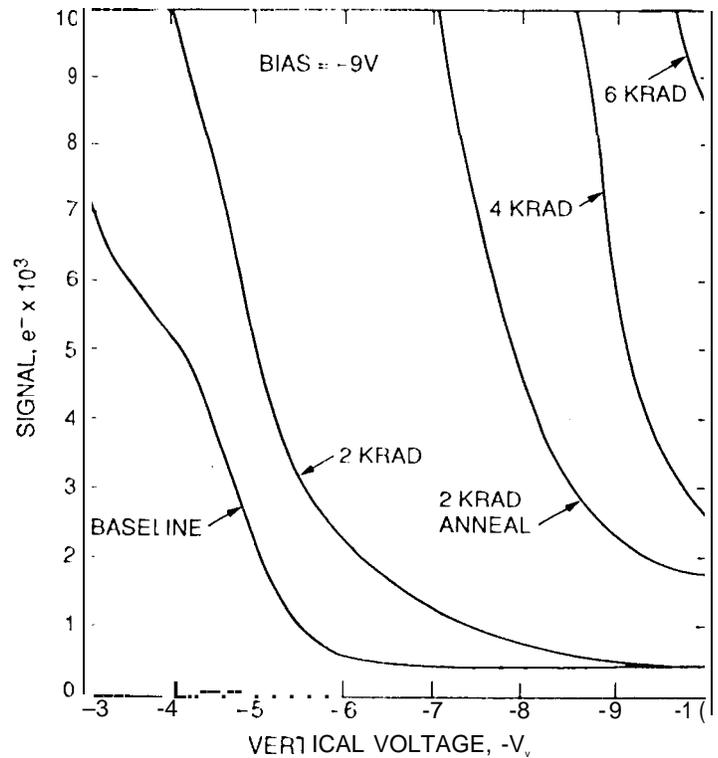


Figure 23a. Dark current plots as a function of negative clock drive for three CO-60 irradiation levels. Note that onset of inversion requires additional drive for increasing amounts of radiation. At 6 krad the shift is 2.5 V, greater than the a 0.2 V shift measured in the center channel. A short high temperature anneal is performed after 2 krad which increases dark current for reasons explained in text (i.e., reverse annealing).

Figure 23b. The same data plots as Figure 23a except the gates are biased at -9 V during irradiation as opposed to ground potential. Bias to the CCD separates electron-hole pairs generated in the gate insulator during irradiation resulting in less pair recombination and more damage. The resultant damage is considerably more than the unbiased case shown in Figure 23a. The 6 krad curve shows that the flat-band shift is significant possibly as high as 15 V in the region. Flat-band shift in the center of the channel is only 0.6 V.



to zero at the channel stop region. The lower diagram plots potential for the MPP phase with oxide charge added thereby simulating radiation induced charge. Note that the potential now increases as we approach the birds beak because the pinned condition cannot be maintained due to positive charge build-up (gate potentials as high as -24 V are required to pin the region). As discussed above, full well is determined by the potential difference between the MPP phase (phase 3) and non MPP phases

(phases 1 and 2). As indicated in the figures after irradiation only a 0.7 V barrier is left (compared to a 2 V difference). Hence, BFW is reduced considerably near the birds beak compared to the center of the channel (refer back to Figure 21). Since BFW is reduced the optimum full well point shifts towards SFW.

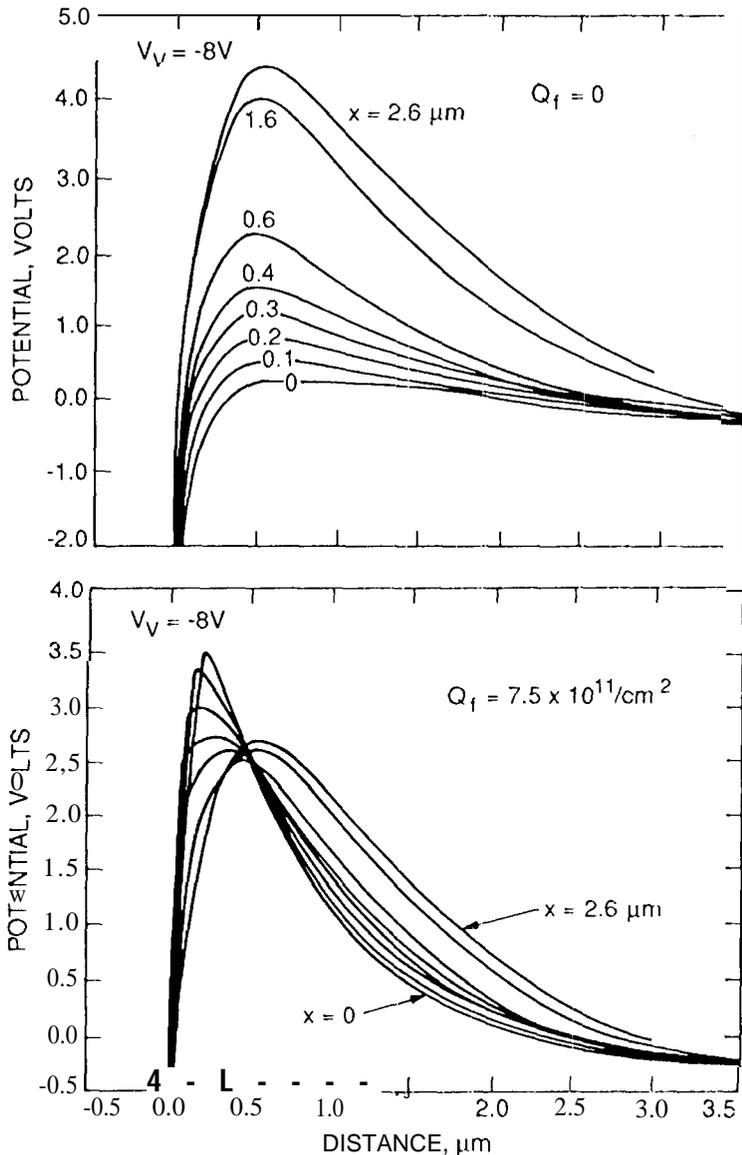


Figure 24. PISCES modeling data showing potential plots for the signal channel and the birds beak region. The top potential plots are for a non MPP phase without oxide charge. The potential at the center of the channel ($x=2.6$) is 4.3 V and the channel stop region ($x=0$) is 0 V. The lower plot shows the potential distribution after oxide charge, Q_f , is added simulating radiation induced charge. Note that the potential in the birds beak region is now much greater because of positive charge build-up in the region (the region becomes unpinned for the gate voltage applied). Flat-band shift in the center of the channel is small and negligible. The potential difference between phase 3 and phases 1 and 2 is therefore reduced considerably. premature blooming occurs along the edge of the channel stop region reducing overall full well performance. (Figure 21).

The inversion and full well problems caused by radiation can be reduced by employing a super notch structure as shown in Figure 25 (the "notch" structure indicated is employed to reduce bulk trapping - an effective technology). Super notch effectively isolates the birds beak region from the signal channel. For example, Figure 26 plots dark current as a function of negative drive for different super notch widths ranging from 2-15 microns (pixel pitch is 18-microns based on a 4-micron channel stop before processing). The test CCD was only slightly damaged with radiation to demonstrate flat-band shift at the birds beak region. Note when the channel butts up to the channel stop (i.e., 15-micron super notch) that it is difficult to invert the CCD requiring a negative drive voltage of -10 V. However, when the channel is pushed back by 4-microns from the center of the channel stop inversion is controlled (requiring -6.5 V).

The penalty paid in implementing super notch is a reduction in full well because the width of the signal channel is reduced. Figure 27 plots well capacity for the same CCD. Full well is reduced from 270,000 e- to 195,000 e- when a 10-micron super notch is employed. The Sandbox CCDS will not employ super notch because of full well reasons. However, the studies above

(and below) have guided us around the birds beak flat-band shift problem by *the manner in which the CCD is clocked as discussed in the next section.*

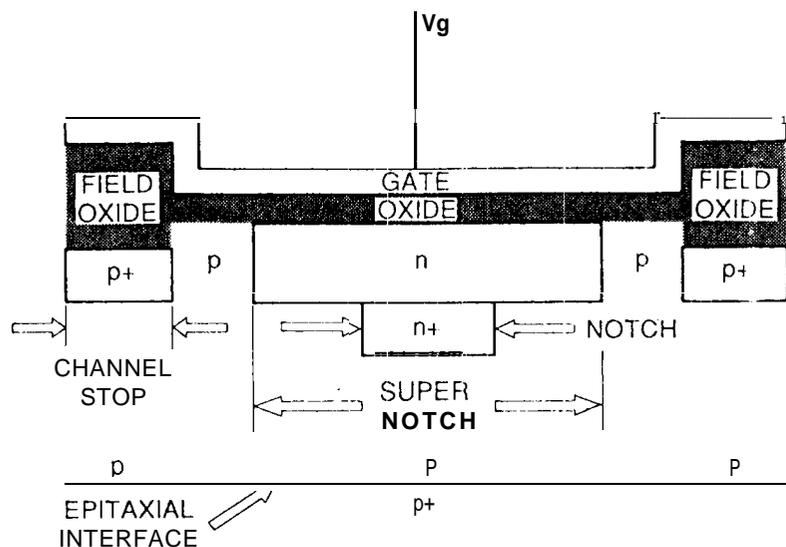
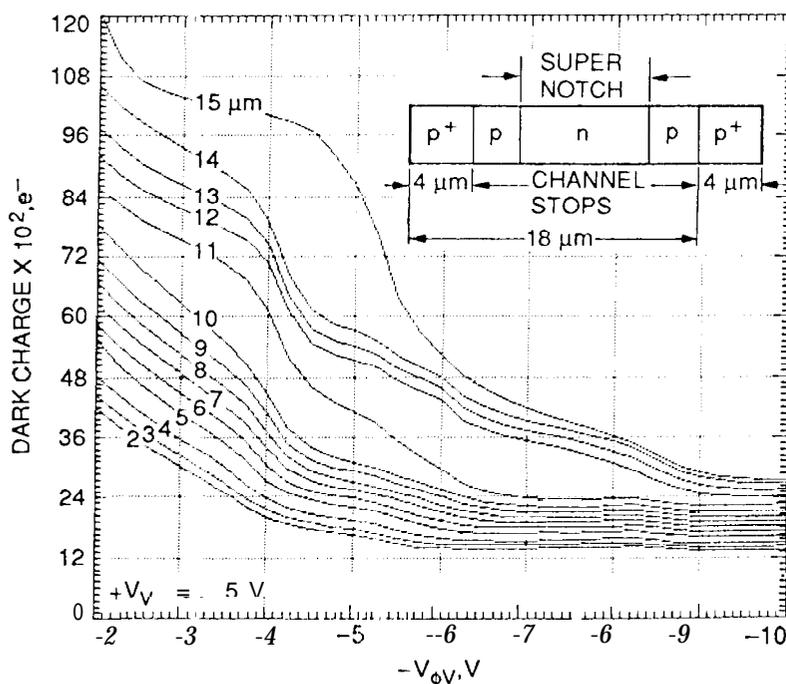


Figure 25. Super notch structure used to isolate birds beak and signal channel. The technology reduces flat-band and inversion problems induced by radiation. The buried channel is defined by a separate mask leaving sufficient p material between the p⁺-channel stop and n-buried channel regions. The "notch" structure also shown is another mask used to implant the *signal channel deeper* and provide a smaller channel to transfer *small charge packets*. The notch is often used to reduce CTE trapping problems for ultra-large CCD arrays or devices used in radiation environments.

Figure 26. Dark current plots demonstrating the benefits of super notch after the device is exposed to a small amount of ionizing radiation. Various super notch channels are investigated on this test CCD that gradually show the isolation effect as the width is varied. A 15-micron super notch overlaps the channel stop and provides no isolation. In this case it is difficult to control inversion requiring a clock drive > -9 V. However, as the super notch width is made smaller isolation is achieved. A width of 10-microns *provides good isolation*, approximately 1-micron removed from the channel stop after processing.



7.3 Reverse Annealing

Dark current results for the 4 krad and 6 krad curves presented in Figure 23 are actually much worse than shown because of an interesting effect referred to as reverse annealing. Note that a significant shift occurs for the 2 krad curve after the CCD was annealed at +50 C for 2 hours. Annealing was not performed after the 4k and 6 krad doses but given time they would shift significantly also.

Reverse annealing is a radiation effect that has been recently studied in detail for the Cassini and Space Telescope projects. It appears to be a very complex, long term chemical reaction associated that takes place in the gate insulator immediately after

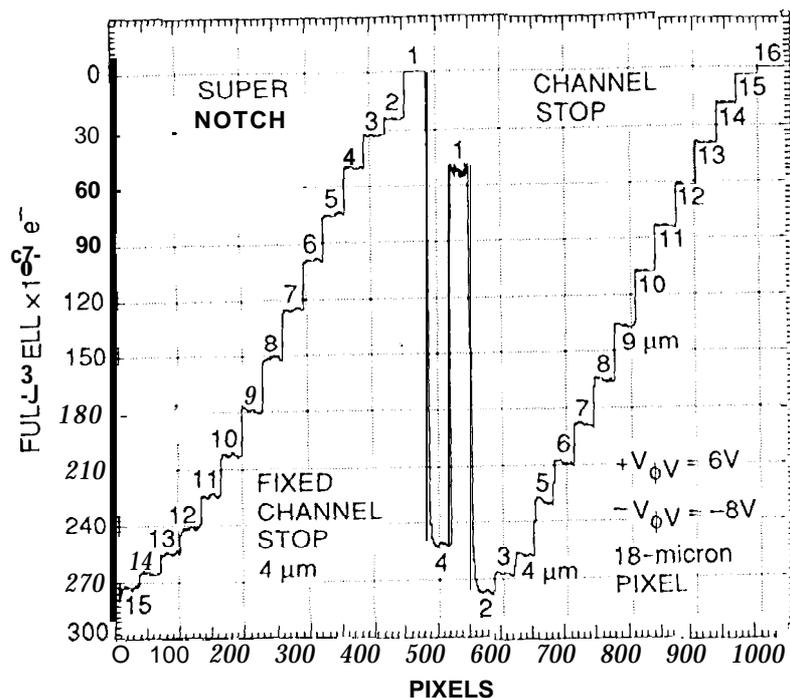


Figure 27. Full well line trace generated by the same test device as Figure 26 designed with different super notch widths in columns 0-500. Note as the width of the notch decreases a corresponding decrease in full well is experienced. Good channel stop isolation requires a 10-micron super notch. Full well is reduced from 270,000 e- to 195,000 e- when this super notch is employed. Super notch is not used in the 500-1000 column region. In this area the channel stop width is varied from 1-micron to 16-microns and is used to find the minimum channel stop width. For the CCD process used 2-micron channel stops are sufficient

irradiation. Similar effects have been observed in other types of MOS devices and various models presented (Ref. 6). We briefly present one of these models here that appears to fit our observations.

The process begins when radiation induces electron-hole pairs in the gate insulator (wavelengths shortward of 1800 Å where oxide absorbs incoming photons). Most of these carriers recombine, however, some holes remain and slowly diffuse in the insulator. Through several chemical steps the free holes generate H⁺ ions in the layer. These ions diffuse towards the Si-SiO₂ interface and attack it with the following reaction taking place:



where 3H-Si-H is a hydrogen passivated trap (after device fabrication the CCD is passivated with hydrogen gas at a high temperature to reduce interface state density). The free electron in the equation comes from the silicon substrate via tunneling. Note the end result of this process is a dangling bond or interface state.

The hydrogen ion diffusion process takes time and is exponentially dependent on operating temperature. For example, We project that 4k and 6krad dark current curves shown in Figure 23 would require several years to stabilize at room temperature. However, warming the CCD to +50 C reduces this time to a couple of hours. Once formed, the new states increase dark current generation.

It is not too surprising that the amount of reverse annealing measured is also dependent on bias conditions to the CCD because holes and ions are both charged. For example, when a negative bias (relative to substrate) is applied an electric field is generated that attracts the H⁺ ions to the gate instead of to the interface stopping the reverse annealing effect. However, biasing the CCD positively repels the ions to the interface accelerating the reaction. Figure 28 shows how reverse annealing is controlled by the bias applied to the CCD during annealing after the sensor is irradiated. In this experiment the CCD is first irradiated with 2 I-a-ads of 5.9 keV x-rays, The CCD is then heated to 60 C and the dark current monitored (top plot). A region that is shielded from the x-rays and not damaged (bottom curve) is also measured to correct for temperature differences that occur in experiment as the CCD is thermally cycled. Note when the gates of the CCD are grounded (0 V) that dark current increases as positive ions make it to the interface. Biasing the CCD to +15 increases the dark rate. However, applying -5 V stops the process completely as theory would predict. Returning the bias to +15 V causes the dark current to increase once again. The effect can

be completely controlled by the user

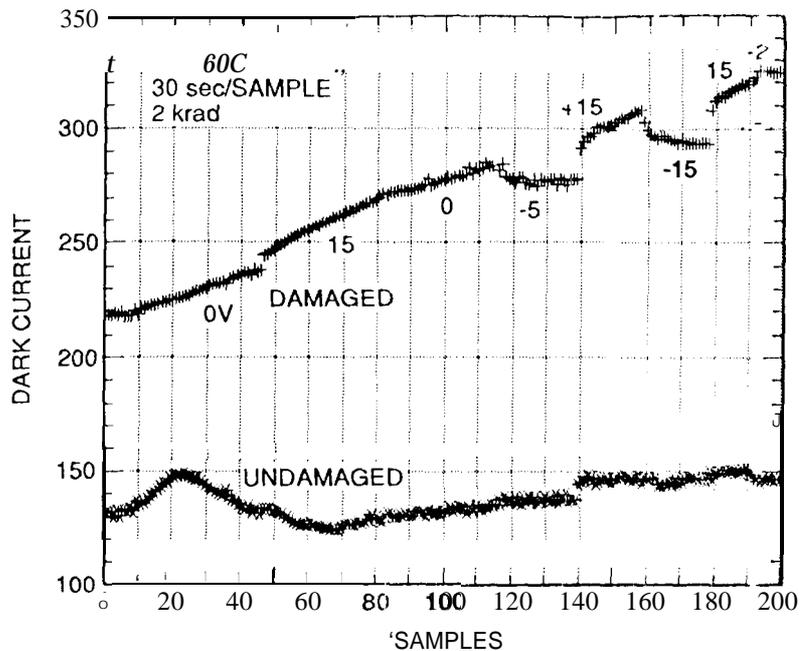


Figure 28. Dark current buildup as a function of time during a high temperature anneal cycle demonstrating the reverse annealing phenomenon. The CCD is irradiated and then annealed at 60 C as dark current increase is monitored. Note that the dark rate can be controlled by how the CCD is biased. The process can be turned off by biasing the CCD with a negative voltage (attracting positive ions to the gate). The lower plot is used to monitor operating temperature by measuring dark current in an undamaged region of the CCD.

We should also mention that flat-band also exhibits *reverse annealing behavior*. This is because the new interface states are electrically active and contribute to flat-band shift. Figure 29 plots SFW characteristics for a non MPP CCD during and after the sensor is irradiated with 5.9 keV x-rays. The baseline response before irradiation is indicated. Every 13 hours, while the device is being constantly irradiated with x-rays (with +15 V bias), a new full well plot is taken at room temperature as shown. Note that the full well curve slowly shifts towards the left indicating that new positive states are being created. After exposing the CCD to 46.5 krad it is annealed at +50 C for 2 hours and a new full well curve taken (triangles). A net flat-band shift of approximately 2 V is measured, half which comes from the high temperature anneal cycle.

Understanding the physical effects behind reverse annealing, and many other ionizing processes that occur in the CCD, one can minimize the amount of radiation damage induced. The improvement can be significant if carefully studied and planned (a factor of 20 was gained for the Cassini project simply by understanding the physics involved). For example, Figure 23 shows a dramatic difference in flat-band shift induced by how the CCD is biased. When biased during irradiation e-h pairs are separated leaving more holes to damage the interface. The unbiased condition allows carriers to recombine. Figure 30 shows the dark current increase for a Cassini CCD as a function of bias during irradiation. Minimum dark current generation occurs for zero bias because more recombination occurs. Note that damage is independent of polarity and is less for colder operating temperatures (carrier diffusion is less which promotes recombination). After irradiation it is important to keep the positive ions away from the Si-SiO₂ interface. This is accomplished by biasing the CCD negatively (normal clocking provides this condition automatically).

The CCDs characterized above were either damaged with gamma-rays or x-rays to a specified rad level (a rad is equal to 100 ergs of energy deposited per gram of material). Exposing the sensor to a differentiation source, such as protons, would give an entirely different result (for the same ionizing rad dose). The stopping power exhibited by protons is typically much greater than energetic photons. Hence, the density of e-h pairs generated by protons in the gate insulator is greater, and therefore, more recombination occurs. Hence, ionization damage for protons is significantly less than gamma-rays, a fact verified by experiment. This knowledge effectively reduces the rad level.

one concluding remark. The reverse annealing effect discussed above may not be observed for all CCD families. Ionization damage is very dependent on the CCD process employed (unlike bulk damage effects which for the most part are process independent). For example, it appears that reverse annealing naturally occurs in certain devices with Si₃N₄ (or similar) encapsulation layers. Devices that use an all oxide insulator, for example, may not experience the problem.

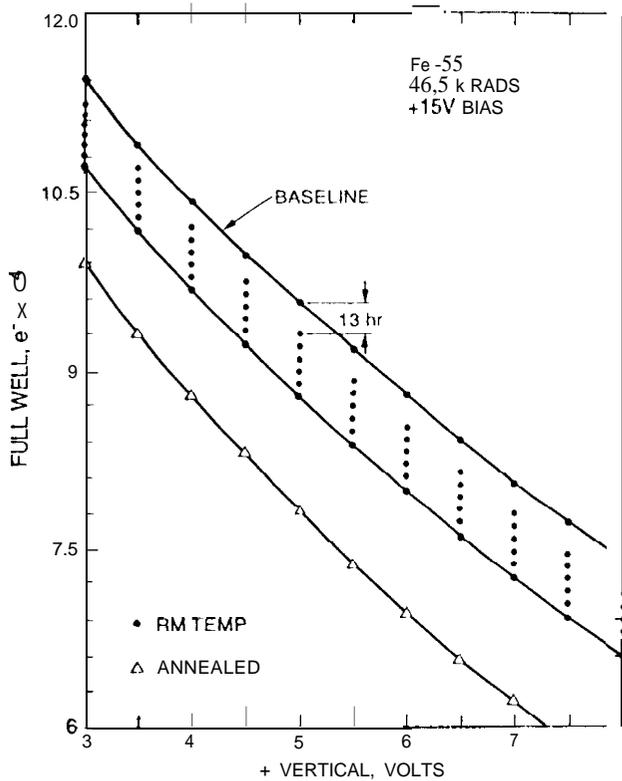
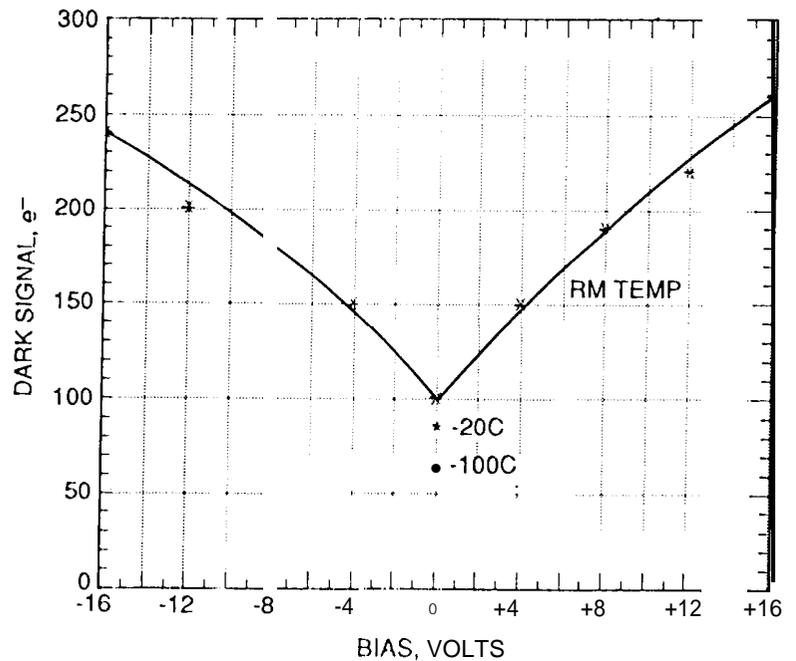


Figure 29. Full well characteristics before and after a CCD is irradiated with Fe-55 x-rays demonstrating that flat-band is also associated with reverse annealing. The plot labeled with triangles was generated after the CCD was annealed. As shown, a large shift in the full well curve was observed. The curve only plots SFW characteristics to avoid blooming problems that develop during irradiation.

Figure 30. Dark current as a function of CCD bias during irradiation. Carrier recombination is minimized in the gate insulator when bias is applied by forcing radiation induced electron-hole pairs apart. Note that damage is independent of polarity as long as an electric field across the insulator exists. Irradiation polarity should not be confused with annealing polarity where different mechanisms are at work. For reverse annealing we require a negative polarity to delay or stop this process.



8. Summary

CTE and dark current generation are two critical performance parameters that remain uncertain for the Sandbox CCDs. These characteristics have varied dramatically in the past depending on the quality of the silicon wafers used. The concern is important and most manufacturers have experienced the difficulty. CCDs require the best silicon that can be grown and efforts in this area have been given top priority. Curiously silicon material was not a major concern to CCD performance in the past. Other CCD problems related to process and design difficulties were often dominating. Now that the CCD has matured in these areas silicon material has become the limiting factor for many performance parameters. Unfortunately, no method has been devised to test silicon wafers before CCDs are fabricated. Finding a technique, equally as sensitive as the CCD, is a major challenge for CCD workers. For now we can partially deal with the silicon problem, if it arises, by how the CCD is operated. This paper, for example, has discussed several operational techniques to improve CTE by the way the CCD is cooled and clocked. However, to be effective, the user must perform a series of tests to understand the CTE mechanisms involved (i.e., characterize bulk states).

The silicon problem will likely become more critical in the near future because of four reasons. First, as CCD arrays get bigger CTE performance will need to keep pace. Second, dark current will be important because cooling requirements for large arrays will be demanding. Third, 4-inch material, which many CCD manufacturers now use, will eventually become obsolete (3-inch wafers have gone through a similar history). Quality silicon will come from 5-, 6-inch or larger wafer sizes. Four inch manufacturers are already realizing this fact. Many CCD manufacturers in the states are moving to larger CCD lines which will relax the problem. (e.g., the Reticon CCD group is changing over to a 6-inch line). Fourth, new scientific applications will demand improved performance which in turn will push CCD technology and silicon requirements.

Three of the 4096 x 4096 Sandbox CCDs are some of the largest CCDs made today. Currently the CCD is going through a growth period where prototype arrays larger than this have been fabricated. As long as yield figures continue to improve for the CCD larger arrays can be fabricated. An ultra-clean process facility in conjunction with large silicon wafers are key requirements in fabricating large CCDs. For example, the Philips CCD group in the Netherlands has an ideal laboratory to fabricate ultra-large scientific CCD arrays. Their CCD lab is based on a Class-1, 6-inch wafer line. The scientific community may take advantage of this opportunity later this year and fabricate a 9k x 7k, 12-micron pixel CCD, the largest monolithic chip fabricated. Other CCD groups have similar plans. It will be interesting to see just how big the CCD will become in the next few years. Currently it is difficult to predict the theoretical size limitation as things improve.

Competition among CCD manufacturers is currently intense. This has not always been the case. Several years ago scientific CCD production was in jeopardy forcing some good groups out of business. CCD technology has finally matured and has generated an explosion of applications making it now profitable for many groups. However, cost for a custom CCD remains to be a problem for the scientific community in general. The price for a lot run is approximately \$100K to \$140K and continues to rise rapidly. Additional funds are required to perform testing and packaging tasks. Thinning and backside illumination requirements typically doubles the price. The Sandbox method described in this paper attempts to reduce costs by sharing lot expenses among several customers. Cost for Sandbox customers depends on array size and quantity of devices that occupy the wafer.

An exciting area to watch in the future is high speed CCD advancements. This paper briefly addresses some high speed limitations for the CCD. Knowing these problems allows the CCD to be designed and tailored to perform amazing high speed feats. How far the CCD advances in this area depends significantly on computer technology which has advanced at the same pace as the CCD. The Cinema CCD, for example, challenges this market because storage requirements are very demanding. A ten minute movie scene, for example, will generate 900 gigs-bytes of information (2 bytes/pixel). A tera-byte computer system is therefore required to run the Cinema CCD. Although building a camera and computer system is technically possible, it remains to be seen if profits can be made on such a camera system.

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10. REFERENCES

Many Scientific CCD topics examined in this paper are discussed in considerable depth in a collection of CCD publications written or co-authored by the CCD Advanced Development Group at JPL. These articles and papers can be obtained on request by telephone or letter. Several CCD publications were collected and published in three CCD special issues by Optical Engineering: (1) Charge Coupled Device Characterization, Modeling and Application, Volume 26 Number 8, August 1987; (2) Charge Coupled Device Manufacturer and Application, Volume 26 Number 9, Sept. 1987; (3) Charge Coupled Device and Charge Injection Device Theory and Application, Volume 26 Number 10, Oct. 1987.

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