Submitted for presentation at the IEEE Nuclear and Space Radiation Effects Conference (July 1995)

MULTI-SHIELDED p-FET DOSIMETER

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ABSTRACT

A compact device was developed for dose measurements where each of four p-FETs has a different shield. Radiation data from the STRV-1 b shows that p-FETs can be used to map the radiation inside a spacecraft.

INTRODUCTION

The detailed knowledge of radiation levels within a spacecraft are . important in verifying the radiation codes [1] and in understanding the more complex phenomena of spacecraft charging [2]. This paper describes a microchip consisting of four individually shielded p-FETs accessed using a multiplexer. In addition a new set of equations were developed for dose calibration.

DISCUSSION

The microchip layout developed on this effort is shown in Fig. 1, It consists of seven components listed in Table 1 including p-FETs PO, Pl, P2, and P7 each with different shields. These shields were fabricated in the kovar lid by chemical etching. The microchip, shown in Fig. 1, was fabricated in 1.2-pm CMOS rad-soft process. The chip was packaged in a 16-pin flat pack.

The equivalent circuit for the chip, shown in Fig. 2, has a multiplexer and decoder used to place each component selectively in the feedback loop of the operational amplifier circuit shown in Fig. 3. The circuitry was designed to force a current at the temperature independent point through the p-FET during measurement. When not operating, the p-FETs are unbiased,

The calibration of the p-FETs must account for both dose and temperature effects. The analog voltage, VA, shown in Fig. 3 is:

$$VA = VA_{oo} + VAT(T - To) + VO_D \cdot G \cdot D \quad (1)$$

where VA_{oo} is the initial output voltage determined from spacecraft ground tests, VAT is the temperature coefficient determined from flight data, VO_D is the dose coefficient determined from Cobalt 60 ground tests, G = Gain = Rl 3/R1 2, and To = 27°C. The dose is calculated from:

$$D = [VA - VA_{oo} \cdot VA_T(T - T_o)] / (VO_D \cdot G) \quad (2)$$

The output voltage, VO, for the p-FET follows from the square law behavior of the FET operating in saturation [3]:

$$VO = VT - \sqrt{(2 \cdot ID/\beta)} \quad (3)$$

where VT is the threshold voltage, β is the tranconductance, and ID is the current chosen at the temperature independent point. This expression is used to determine the VO-dose calibration curve given VT, β, and ID as discussed below.

The temperature-dose expression for the VT is:

$$VT=VT_{oo}+VT_T\cdot(T-T_o)+\Delta VT[1-\exp(-D/D_o)] \quad (4)$$

where VT_o is the threshold voltage at To and D =8, VT_T is the threshold voltage temperature coefficient, Do is the VT dose coefficient, and AVT is the maximum change in VT when the radiation reaches infinity. When D = Do, the VT increases by he.

The expression for VT indicates that VT is rate limited which depends on the filling of a firrite supply of gate oxide hole traps [4]. The VT equation was solved using the least squares method to determine VT_{oo}, VTT, and AVT. The parameter, Do, was found using an optimization technique that maximized the least squares correlation coefficient.

The dose-temperature expression for/? is:

$$\beta = \beta_{oo}(T/T_o)^{-n}/[1 + (D/D_m)(T/T_o)^{-n}] \quad (5)$$

where /?$_{oo}$ is/3 evaluated at To and D = O, n is the β temperature coefficient and D_m is the β or mobility dose coefficient, When D = D_m at T = To, then #? is reduced by 50 percent. This equation was formulated by combining the β temperature and dose dependencies as the sum of reciprocals.

The operating point for the p-FET drain current at the temperature independent operating point is found by differentiating the VO expression with respect to temperature. Setting the result to zero at the measurement temperature, T_m and D = O leads to [3]:

$$ID_{mo} = 2\beta_{mo}{}^3(-VT_T/\beta_{Tmo})^2 \quad (6)$$

where $\beta_{Tmo}=(-n/T_m)\beta_{mo}$, $\beta_{mo}=(T_m/T_o)^{-n}$.

The VT, β, and VO results are presented graphically in Figs. 4 to 6. The curves were obtained by fitting the data shown in Fig. 4 to Eq. 4 and the data shown in Fig, 5 to Eq. 5. Thus, the p-FET results can be characterized by seven parameters, namely VT_{oo}, VTT, AVT, D_o, β_{oo}, D_m. These parameters are listed in Table 2 for PO. The device-to-device uniformity was excellent,

The VO values were obtained from Eq. 3 using Eq. 4 for VT, Eq 5 for/?, and Eq. 6 for ID_{mo}. The VO_{mo} values, listed in Table 5 for each of the four p-FETs, are within 0.1 percent of each other. The VO values are plotted in Fig. 6 for two different values of ID_{mo}. The curves for the PO design value of ID_{mo} = 88.4 µA show that VO is fully temperature compensated at D = O. The curves for the operating value ID_{mo} = 100 µA show that temperature compensation occurs near 100 krads and that VO_{mo} = 1.507 V. These parameters were used as the target design parameters, thus the 100 µA curve is designated as the calibration curve.

A similarly fabricated p-FET was flown on the STRV-1 b launched June 17, 1994 in to a 10.59-hr geosynchronous orbit. The p-FET temperature dependence was determined from the slope of the flight data as shown in Fig. 7. The dose for the STRV-1b is shown in Fig. 8. It shows the dose at different locations and behind different shields in the JPL experiment box. The results indicate that the dose is not uniform across the exposed portion of the box.

CONCLUSION

This paper describes the design, fabrication and calibration of a compact multiply-shielded p-FET dosimeter. The calibration included characterizing the p-FETs at four doses and three temperatures. Multiply-shielded p-FETs were used on the STRV-1 b where the dose was observed to vary across an experimental test box.

ACKNOWLEDGMENT

The research described in this paper was performed by the Center for Space Microelectronics Technology, Jet Propulsion Laboratory, California Institute of Technology, and was sponsored by the Martin Marietta Astro Space and the Ballistic Missile and Defense Organization, Innovative Science and Technology Office. The devices used in this study were fabricated through MOSIS, Information Sciences Institute, University of Southern California. File: NSRE5129.DOC

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Table 1. Microchip Devices

DEVICE	TYPE	SHIELD (mil)
Po	GATE OXIDE p-FET	6
PI	GATE OXIDE p-FET	0
P2	GATE OXIDE p-FET	2
P7	GATE OXIDE p-FET	10
N3	FIELD OXIDE n-FET	10
N5	GATE OXIDE n-FET	10
R4	METAL-1 RESISTOR	10
E6	EXTERNAL DEVICE	NA

able 2. p-FET Parameters(ICM#4926.XLS)

PARAMETER	UNITS	Po
VT_{oo}	v	-0.8598
VTT	mV/°C	1.7595
AVT	v	-0.4998
Do	krad	118.9166
B_{00}	μA/V²	474.7261
D_m	krad	588.5114
n	unitless	1.7169
ID_{mo}	μA	88.3632
VO_{mo}	v	-1.4701
ID_{mo}	μA	100
VOmo	v	-1.507
AVO_m	v	-0.7658
D_x	krad	142.8
VOD_{mo}	mV/krad	-4.732
DEV = 15	T_m(°C) = 10	T_o(°C) = 27

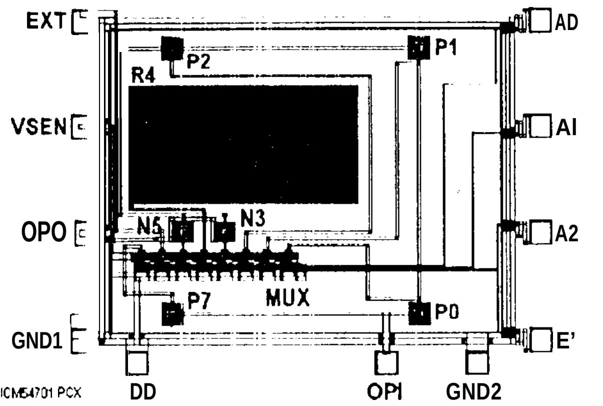

Figure 1. Microchip with four p-FETs, PO, P1, P2, and P7. Each p-FET is located behind a different shield whose thickness is listed in Table 1. The different shield thicknesses were obtained by selectively them-etching the Kovar lid.

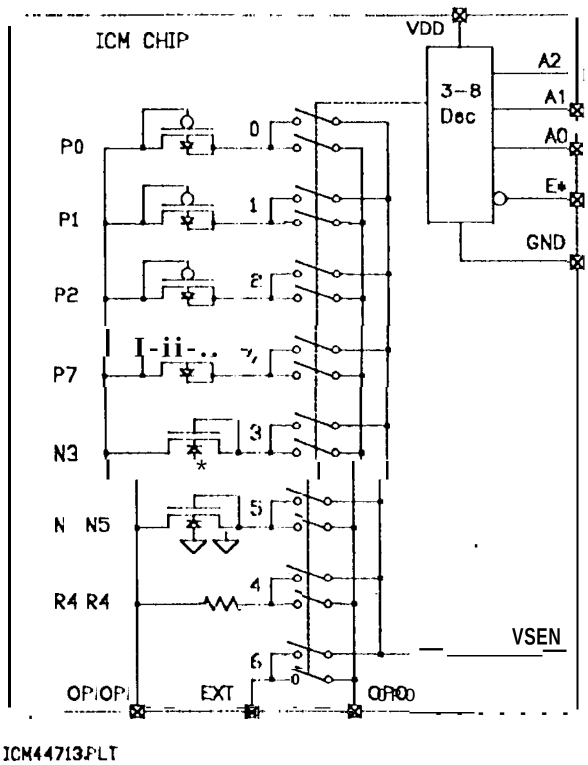

Figure 2. Microchip schematic.

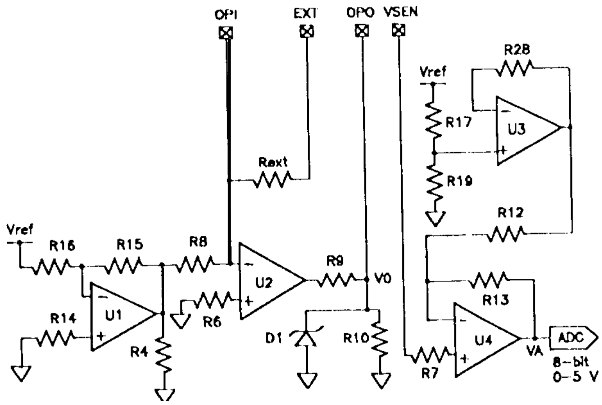

Figure 3. Microchip surround circuitry.

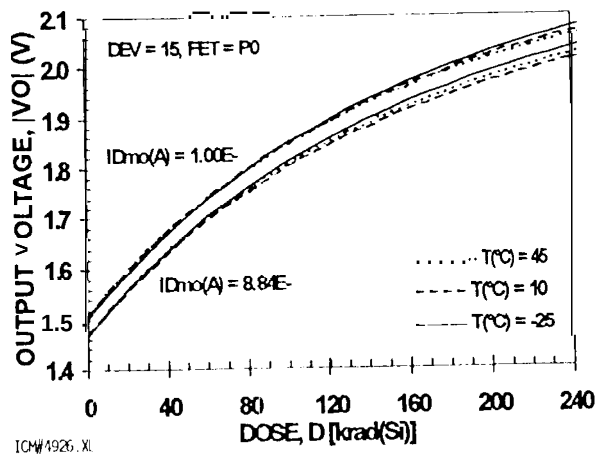

Figure 6. p-FET output voltage dose dependence.

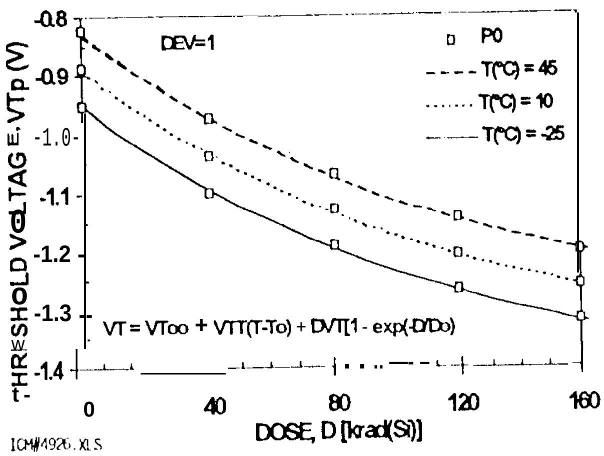

Figure 4. p-FET threshold voltage dose-temperature fit to Eq. 4.

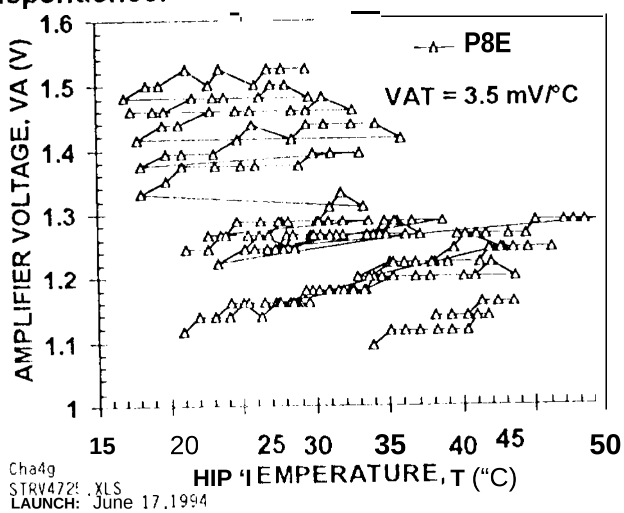

Figure 7. STRV-1b p-FET VA-temperature dependence, VAT = 3.5 mV/°C.

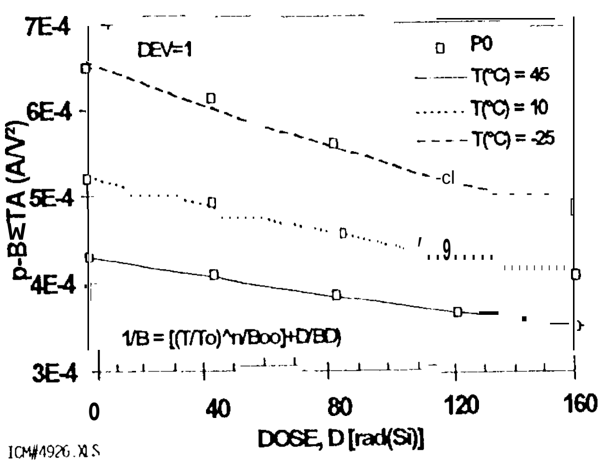

Figure 5. p-FET beta dose temperature fit to Eq. 5.

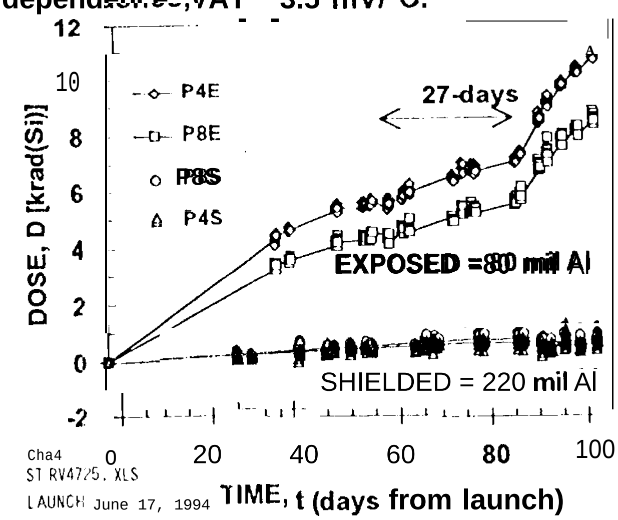

Figure 8. STRB-1b dose profile for devices behind 80-mm and 220-mm Al shields.