Advanced Failure Determination Measurement Techniques Used in Thermal Fatigue Life Testing Of Electronic Packaging

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Abstract:

Thermal fatigue life testing of various electronic packaging technologies is being performed by the Reliability Technology Group at the Jet Propulsion Laboratory. These testing efforts are in progress to improve understanding of the reliability issues associated with low volume packaging technologies for space applications and to develop qualification and acceptance approaches for these technologies. The work described here outlines the electrical failure detection techniques used during testing by documenting the circuits and components used to make these measurements, the sensitivity of the measurements, and the applicability of each specific measurement. These measurements have been applied to life testing of various SMT packages and also vias in polyimide-kevlar boards. Intermittent current detection combined with milliohm resistance tracking circuits were designed and fabricated to explore the onset of electrical failure in gullwing, j-lead, and leadless surface mount devices and vias for a variety of test conditions. In addition, time constant and frequency response measurements were used to measure resistance fluctuations in passive devices. This was done to generate fatigue data for capacitor, resistor and inductor packages, which often have different package designs than active surface mount devices. The following work presents all of the circuits designed and documents preliminary test results.

Keywords: fatigue, surface mount, measurement, testing, thermal cycling, intermittent detection

Introduction / Background:

The Reliability Assessment Technology Testing Laboratory at the Jet Propulsion Laboratory is dedicated to the qualification and reliability assessment of advanced technologies and designs for spaceflight application. In addition to other ongoing work, life testing of surface mount technology (SMT) and polyimide-kevlar boards is currently in progress. In both cases, stresses due to coefficient of thermal expansion (CTE) mismatches are induced by thermal cycling. Life testing of surface mount devices is not new, but the current effort explores the relationship between reliability and various parameters for ultra low volume applications. These parameters include: detailed workmanship inspection and visual correlation of defects to electrical measurements, rework, different cyclic temperature ranges, different cyclic mean temperatures, vacuum/atmosphere, and gullwing lead height. The Surface Mount Technology Qualification research effort (SMT RTOP) provides life testing results to other related RTOPs and explores testing methodologies and electrical failure definition. Sources in literature have often reported the importance of intermittent open detection as essential in assessing the electrical performance of solder joints under thermal cyclic loading [3,6]. However, this effort combines intermittent open detection with resistance tracking measurements in hopes of providing greater resolution into the onset of failure of surface mount devices. Furthermore, large value capacitors and inductors may have non-traditional package styles which may cloud reliability predictions for these devices. Therefore, additional techniques are required to electrically assess the life of these devices under thermal cyclic loading.

As a "piggy-back" effort for a JPL earth orbiting project, which is anticipating a strenuous thermal cycling environment, the resistance tracking and intermittent detection measurements were applied to life testing of a flight-like polyimide-kevlar board. The stresses on these vias is somewhat exacerbated by the large z-axis CTE of polyimide-kevlar.

Solder joint failure definitions vary between investigators, examples include: 50% peak load drop, 10% increase in electrical resistance, initiation of a visible crack, complete fracture of joint, 7 sequential intermittents, etc. Therefore, this work will attempt to enhance electrical failure determination techniques, and provide future test engineers a resource for building simple test circuits for technology qualification and life testing.

Test Articles:
The SMT RTOP board as shown in Figure 1 was designed specifically for SMT life testing, hence several steps were taken to isolate the solder joints as the driving life parameter. These design steps include: all connector pins are redundant, all signal traces are on the top or bottom layers, wire-bonds are all double-stitched, and all vias used to go from the top to bottom layer are triply redundant. Furthermore, the board backside allows electrical probing to each lead to determine exactly where the solder joint failure occurred (to one of two solder joints). The board is seven-layers to ensure copper balancing and provide a realistic composite CTE. The board material is polyimide. Each board contains numerous components as listed in Table 1. Thirty-five test boards are being subjected to various test environments as part of a complete design of experiments. Figure 2 is a schematic representation of the SMT RTOP board shown in Figure 1. Each resistor represents the daisy chained component(s) to be measured. Due to the large number of components and the relatively small number of pin connections some sacrifices in resolution were made. For instance, some of the automated resistance tracking measurements were made on multiple parts, although isolation to individual leads can be achieved manually. Four intermittent open measurements are made on the board, one per each chain. The RC and RLC circuits for passive device failure detection will be discussed later.

Figure 3 is a polyimide-kevlar board used for via thermal fatigue characterization. This board is similar to one which is to be used by a JPL project in an earth-orbiting mission, which will, therefore, be subjected to extensive thermal cycling. Numerous jumpers were placed on the boards to provide a series circuit of vias; a few gullwing surface mount devices were tested on these boards as well. Four "4 point" resistance measurements and two intermittent detection measurements were used during testing of these boards.

Resistance Tracking Circuit Description:
As shown in Figure 2, there are 16 resistors in the resistance network. Actually, each of these resistors is composed of board traces, wirebonds, internal part wire frames, and solder joints. At a particular temperature, the resistance of all these components is constant, with the exception of fatiguing solder joints.

The fundamental equation for analyzing the measured data is V = I*R. The voltage is measured on opposite sides of a resistance (a daisy-chained part), V1 and V2. Then, by dividing by a known current, the resistance in question is found. The 12 bit, 100 kHz data acquisition channels (DAQ) have very high input impedance; therefore, current flow to the DAQ is negligible. Furthermore, since some testing was done in vacuum, and vacuum electrical feedthroughs are extremely costly, external multiplexers (with a buffered amplifier) were used inside the vacuum system to increase the number of measurements possible (Figure 4). An unswitched multiplexer (MUX) line will draw negligible current from the input line and the switched line is buffered. Therefore, all lead and interconnect resistances (those not on the test board) are irrelevant.

A voltage supply was used to power all of the test articles simultaneously. Therefore, in order to measure the current going through each chain, a current sensing resistor was placed in series with the chain. By measuring the voltage, Vdiff, across the current sensing resistor, Rcur, the current can be calculated. The resistance of the daisy-chained component, Rcomp, is then calculated according to the following:

$$R_{comp} = \frac{(V_2 - V_1)}{V_{diff}} * R_{cur}$$

Since it is hoped to use this resistance measurement to correlate resistance changes with fatigue, as a means of predicting the onset of failure, estimating the uncertainty in the measurement is imperative. The three principal sources of measurement error are: the accuracy of the current sensing resistor, the accuracy of the A/D converter, and noise. In order to reduce noise, both signal averaging and shielded wires were implemented in the system construction. The sensitivity of the measurement is developed by the very basic error propagation equations. The overall error in the resistance measurement is calculated by the following:

$$\sigma_R^2 = \frac{\sigma_{V_1}^2}{I^2} + \frac{\sigma_{V_2}^2}{I^2} + \left(\frac{\sigma_{V_{diff}}^2}{R_{cur}^2} + \sigma_{R_{cur}}^2\left(\frac{V_{diff}}{R_{cur}^2}\right)^2\right)\left(\frac{V_2 - V_1}{I^2}\right)^2$$

Labview® was used as the data acquisition software package. The front panel for measuring resistance is shown in the bottom of Figure 7. All voltage measurements are an average of 1000 samples; all average voltage reads and the number of reads in the 2 and 3 sigma range are stored for future reference and will be evaluated for onset of failure trends. The measured resistance errors are on the order of milliohms.

Intermittent Current Detection:
The intermittent current flow detection circuit (Figure 5), interfaces with the resistance tracking measurements without drawing excessive current (buffered lines). Essentially, when a large resistance spike occurs in the chain of components, the voltage difference across the current sensing resistor will go to zero, since little current can flow through the circuit due to the large chain resistance. When the voltage across the current sensing resistor goes below 1.4V the opto isolator circuit will toggle its logic output state. When this toggle occurs, it latches a Set-Reset (SR) latch circuit. This remains latched until the logic state is read and then reset by the computer.

Sizing of the current sensing resistor (Rcur) has numerous factors which must be considered. First, the resistor serves as a current limiter to the daisy-chained components. The power dissipation due to large currents will cause corresponding large part to board temperature

gradients. This was an important factor for our application, since one of the goals is to correlate the results from vacuum and atmospheric thermal cycling tests. Due to the lack of convection in vacuum, large temperature gradients would make it difficult to correlate the results of the two tests. Testing showed the SMT board with 12 thermocouples had less than 3°C gradient (across board and between parts and board) during vacuum thermal cycling.

An additional Rcur sizing requirement is the voltage at either side of the differential voltage output (resistance tracking circuit) can not exceed 12 Volts to ensure proper operation of the data acquisition board. Also, R-cur sizing drives the sensitivity of the intermittent current detection circuit. Rcur must be sized for a differential voltage greater than the 1.4 V toggle voltage for three primary reasons: noise margin, resistance increases at high temperature, and for solder joint open resistance threshold control. In our condition, the voltage drop across Rcur at standard conditions was approximately 3.5 V. Table 2 summarizes the effects for various Rcur selection for particular resistive component chains.

The minimum period of solder joint open detection is dependent on several parameters. The closer the voltage across R-cur is to 1.4 at standard conditions, the faster it will respond. Furthermore, the voltage across the opto isolator must be below 1.4 V for a period greater than 100 ns due to opto isolator and SR-latch delay. However, the single driving factor for the sensitivity of the circuit is op-amp slew rate. When the resistance change goes above a particular threshold the voltage will drop below 1.4 V; however, the response of the op-amp will lag. The constant op-amp slew rate model predicts the worst case time response for a given circuit with a particular op-amp (Figure 6a).

However, the constant op-amp slew rate model is extremely conservative; in reality, op-amp slew rates are not constant and are dependent on bias voltage, input voltage, internal capacitance, and external impedance. Figure 6b displays the input and output voltage across a 741 op amp. The input was provided using a Tektronix pulse generator. The slew rate at the initial section of the pulse is larger than the .5 Volt/micro-sec as listed as a typical slew rate. The slew rate then begins to "knee" and it approaches the .5 V/micro sec value. However, in the intermittent detection circuit the opto-isolator triggers around the "knee voltage." The actual op-amp response for intermittent current detection circuit is therefore faster than that predicted by the typical slew rate calculation (due to the nature of the circuit and the event that is being looked for). To test this, the pulse generator was applied directly to the intermittent detection circuit. It was verified experimentally that the circuit would trigger in 2.8 micro-sec and 2.6 micro-sec for a 446 ohm and 1395 ohm spike, respectively. This is the worst case response of any Rchain and Rcur combination.

Substituting a 301 op-amp for the 741 op-amp (due to its larger slew rate) would yield resolutions into the 0.3 micro sec range. The 741 was used due to schedule and cost constraints. Furthermore, the circuit containing the 741 op amps was experimentally verified for minimum pulse widths in the range of intermittent measurements reported in literature [3,6].

Resistance Tracking in Passive Devices

The RC circuit is simply a resistor and capacitor in series. A voltage will be applied to the circuit and then the voltage across the resistor will be measured until the capacitor is fully charged. By monitoring variations of the circuit time constant, the resistance (and changes in resistance due to solder joint fatigue) may be calculated. This process is enabled by the high speed data acquisition equipment in use, and a current amplifier circuit used between the DAQ output and RC circuit input. A sample measurement is shown in Figure 7.

The RLC (resistor-inductor-capacitor) circuit is essentially three series RLC circuits in parallel, with C's sized to provide three separated measurements. The resistance is the real resistance of traces, inductor windings, and solder joints, while the L and C are primarily passive devices. At resonance the impedance of the circuit drops significantly, drawing more current from the power supply. This current goes through a transformer, which then enables the detector circuit. A "superdiode" circuit was used to enhance the performance of this detector [8,9]. With larger current, more voltage will be seen across the load resistor in the detector circuit. From this, measurements of the quality factor, Q, and the max peak at the resonant frequency give sufficient information to calculate circuit resistance and monitor resistance fluctuations. The three peaks seen are at the resonant frequency for each of the RLC circuits in parallel. A sample of the measurement is shown in Figure 7.

Preliminary Results:

For reference, the typical thermal cycles for the SMT life testing are depicted in Figure 8. Figures 9, 10, 11, 12, and 14 display combined intermittent detection and resistance measurements. All "Time" scales are in minutes and are in reference to a particular test number not the total amount of exposure in a test environment. Intermittents are plotted using a time vs. chain number scheme (where chain number is superimposed on the y-axis, ohms). Figures 11 and 14 have the intermittent markers circled. Figure 9 displays the evolution for a 28 leadless component from a steady resistance cycle with temperature cycling to relatively large resistance fluctuations. At time = 5000 in Figure 9, the 28 leadless components in question had undergone 727 thermal cycles (-55 to 25°C) and 764 by time = 8500, which is at the end of test 51. After some time in test number 52, shown in Figure 11, the first intermittent occurred in cycle number 787, which then begins to repeat somewhat sporadically until intermittents occur multiple times per cycle as shown in Figure 12 (cycles 823 - 836). The

largest resistance fluctuations (from the steady cycle) are at the hot portion of the temperature cycle (25°C), and particularly at the points of first reaching 25°C and then the initial ramp back down to cold.

The small resistance spikes at the bottom of the resistance cycles (Figure 10) are due to the temperature fluctuations (Figure 8) associated with our 2 stage atmosphere chamber during the -55 to 25°C cycle. However, at the top of the resistance cycle (Figure 10), at time = 5400, a slight shift in the high end resistance is seen. The high end temperatures were measured to be equal at the surrounding cycles; therefore, for a 28 leadless component, a resistance tracking measurement was able to detect damage related resistance fluctuations 57 cycles before an intermittent was detected for a -55 to 25 °C cycle.

Contrasting to this, for a larger temperature cycle of -25 to 95°C (Figure 12), a resistance tracking measurement found resistance fluctuations approximately 4 cycles before intermittent opens were detected.

Conclusions:

In tracking resistances fluctuations, measurements must be compared at like temperatures only. Preliminary test results have shown measurable resistance fluctuations a number of cycles before an intermittent open circuit was triggered. Only a sample of results available are shown for reference; a complete set of results will be presented at the conclusion of the testing program. However, current cumulative life plots are using 7 intermittent opens as the failure criteria. As data continues to be generated, the statistical significance of the results presented here will be investigated and reported. The advantages associated with resistance tracking techniques may prove to be more beneficial for different package types, for instance, fine pitch gullwing components, where local CTE mismatch is a primary driver, the damage may be measured over a much large time interval. Furthermore, in future work, the life data generated will be correlated to manufacturing defects and a number of reliability models (both internal and external to JPL). The resistance at particular temperatures will also be plotted over the life of the component, and the 3 sigma voltage reads (from the 1000 data points) will be examined for trends in identifying failure onset. The work presented here demonstrates relatively simple circuits that can be built with standard DAQ hardware and external circuits with under 2 dollars in component costs. Preliminary results have also shown a relatively close comparison between intermittent open and resistance tracking circuits for leadless devices.

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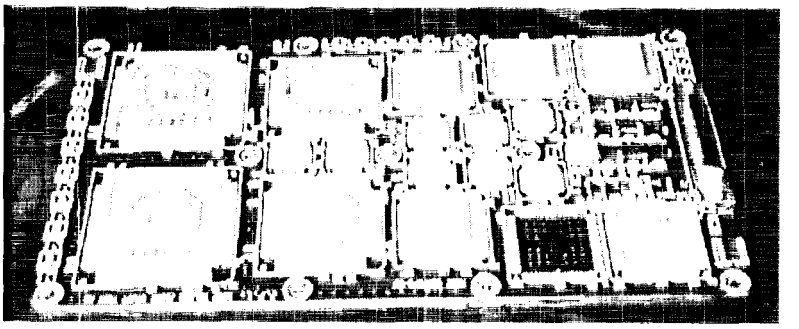

Figure 1: SMT RTOP Test Article

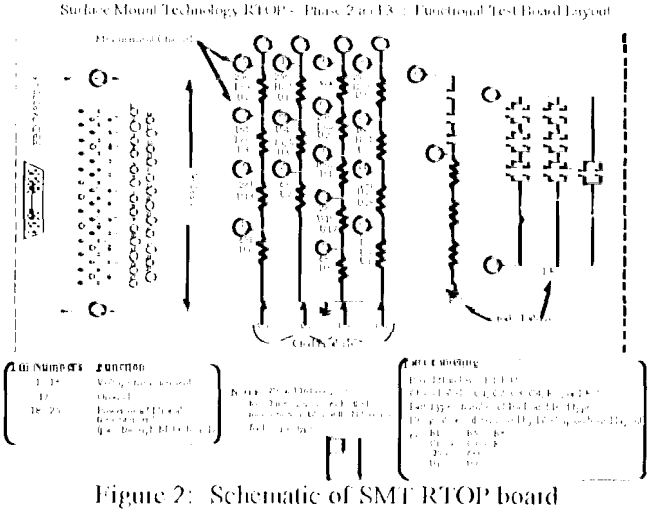

Figure 2: Schematic of SMT RTOP board

Table 1: Components and Respective Measurements On SMT RTOP Test Article
(All components are ceramic unless otherwise noted)

Reference #	Part Type	Lead Type	Package Area	Measurement
U1,2	256 Cerquad	Gullwing	1.46" * 1.'10'"	R / Int
U3,4	164Cerquad	Gullwing	1.15" * 1.15"	R / Int
(15. s.9.10	68 Cerquad	1 eadless	.95 0" * .950"	R I Int
U6,7	68 Cerquad	J1 ead	.950" * .950"	R / Int
U15,16,17,18	28 Cerquad	1 eadless	.450" * .450"	R / Int
(111.1 ?.13.1.1	28 Cerquad	J1 ead	.450" * .450"	R / Int
L1	Inductor-10mI I	Gullwing(4 leads)		RLC
1?. -{	Inductor--6. 8 mH	leadless(* ?)		RLC
C18,14	Cap-560pF	surface mount	805	RLC
C17	Cap-390pF	surface mount	805	RLC
('10.13	Cap-820pF	surface mount	805	RLC
C15	Cap-1000pF	surface mount	805	RLC
C23,20	Cap- 1500])1'	Sill face 111(111111	1206	RLC
C24	Cap-1800pF	Sill (ace' 111(1111	1206	RLC
('?2.10	Cap-2700pF	surface 111(111111	1206	RLC
C21	Cap-4700pF	surface mount	1206	RLC
C1,2,3,4,5,6, 7,8,9,10,11,12	Cap(Tantalum)-100micF	surface mount	.287" * .1'/3" (Size D)	RC/RLC
R4	Resistor-3ohm	surface mount	805	RC
R2	Resistor -5011111	Sill face mount	805	RC
R1	Resistor - 10 ohm	surface 111(111111	603	RC
R3	Resistor-20ohm	surface 111(111111	1206	RC

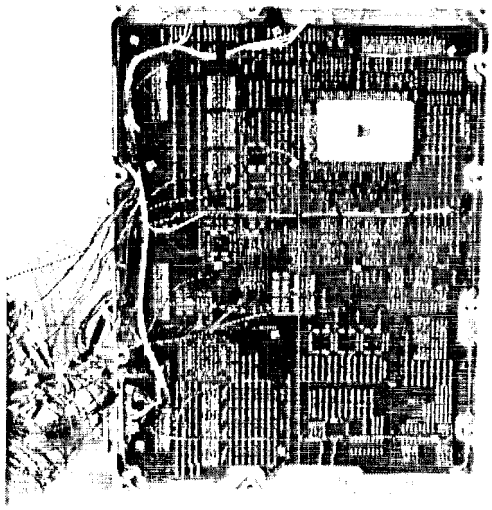

Figure 3: Polyimide-Kevlar Board Used In Via Thermal Fatigue Test

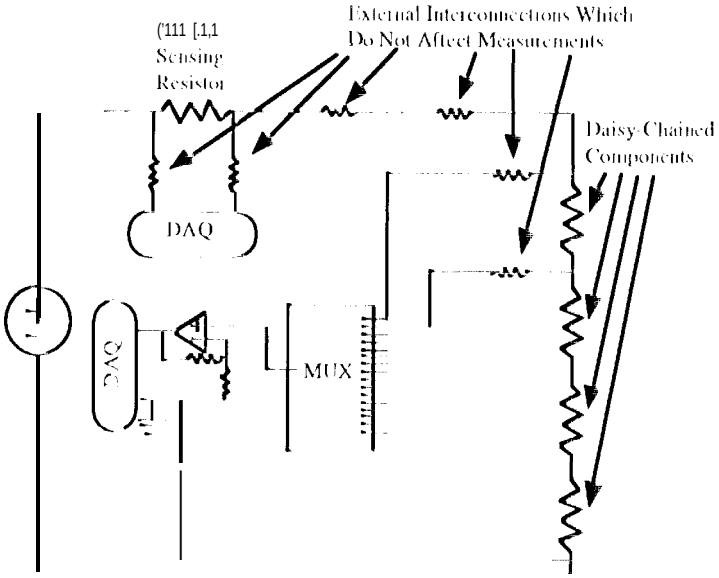

Figure 4: Resistance Measurement's Insensitivity to External Interconnect Fluctuations

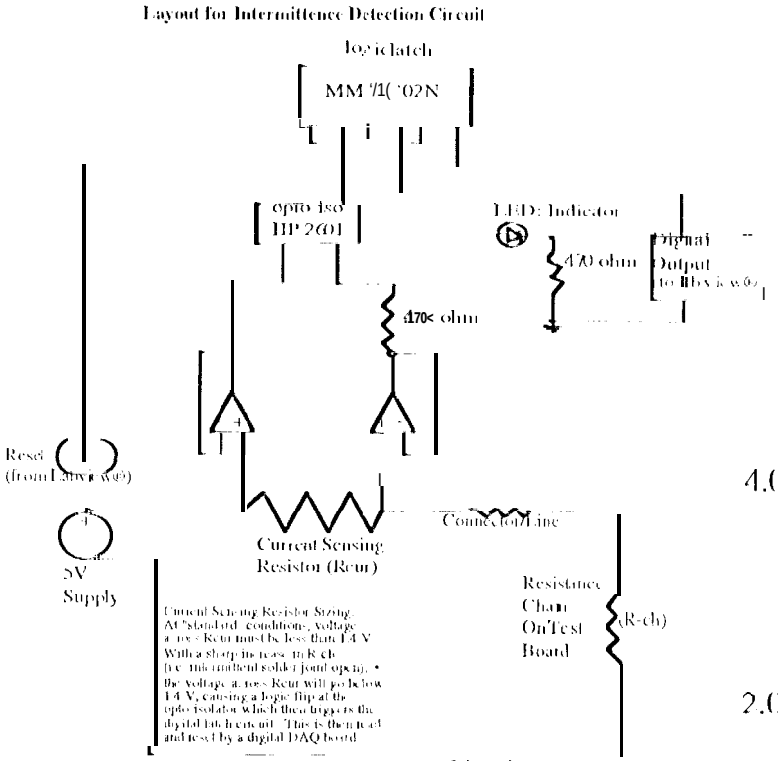

Figure 5: Intermittent Current Detection Circuit

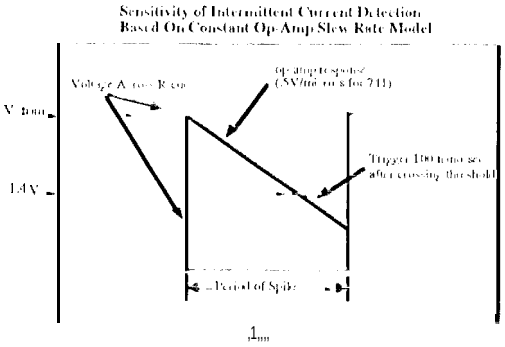

Figure 6a: Circuit Response Based On Constant Op-Amp Slew Rate Model

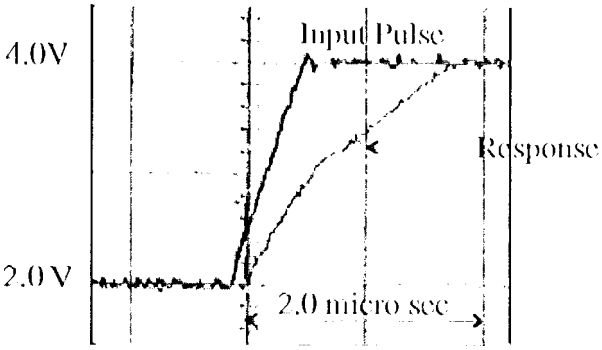

Figure 6b: Op Amp Actual Response To Pulse

Table 2: Current Sensing Resistor izing and Minimum Pulse Detection

R(Chain)	R(Cut)	Vinput	Vthreshold	V(Chain)	Vdiff	Vdiff Margin	Speed (micro sec.)
26	95.3	4.8	1.42	1.03	3.77	2.35	<2.6
38	95.3	4.8	1.42	1.37	3.43	2.01	<2.6
27	95.3	4.8	1.42	1.06	3.74	2.32	<2.0
66	66.5	4.8	1.42	2.39	2.41	0.99	<1.5

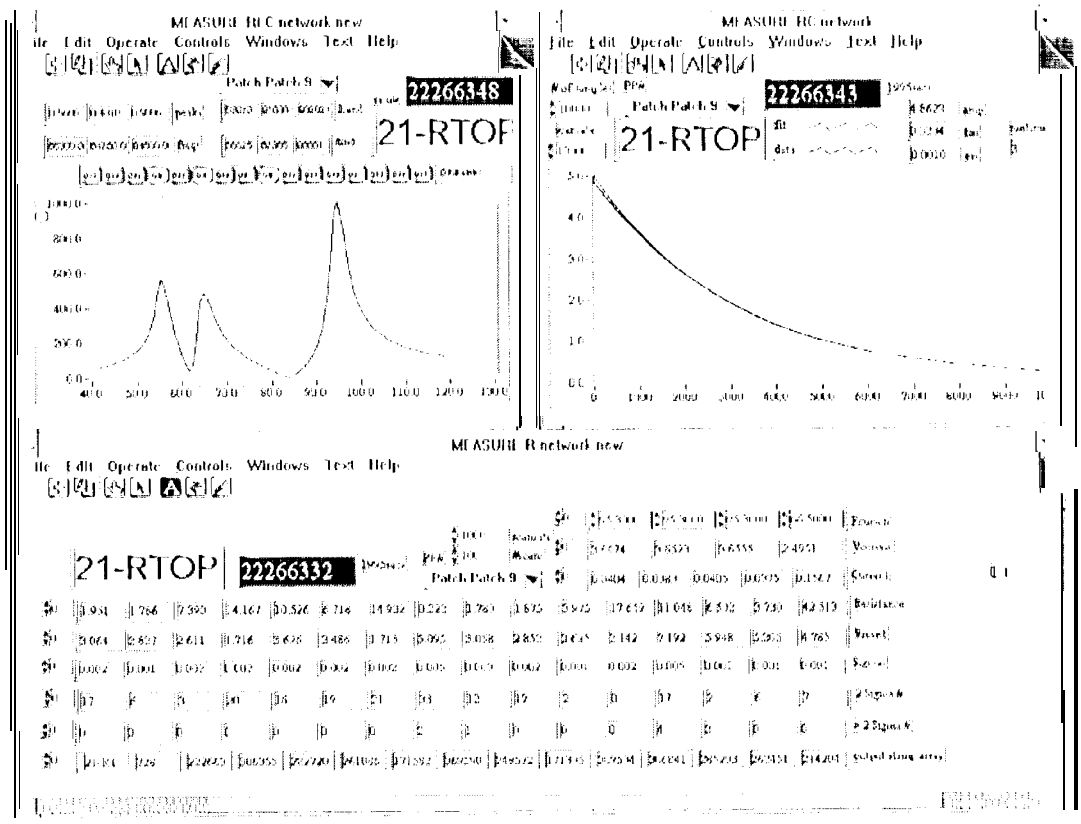

Figure 7: RLC, RC and Resistance Tracking Measurement Labview® Front Panels

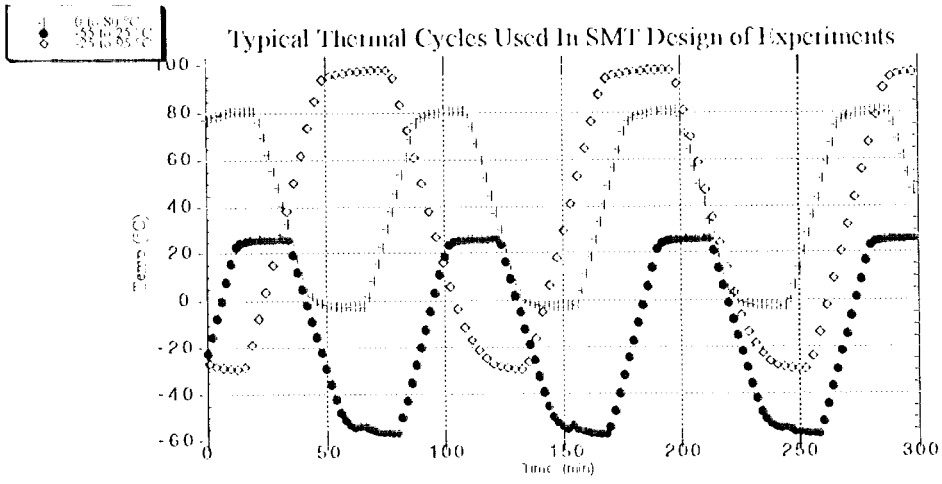

Figure 8: Typical Thermal Profiles for 0 to 80 °C, -55 to 25 "[· and -751095 "(' Cycles

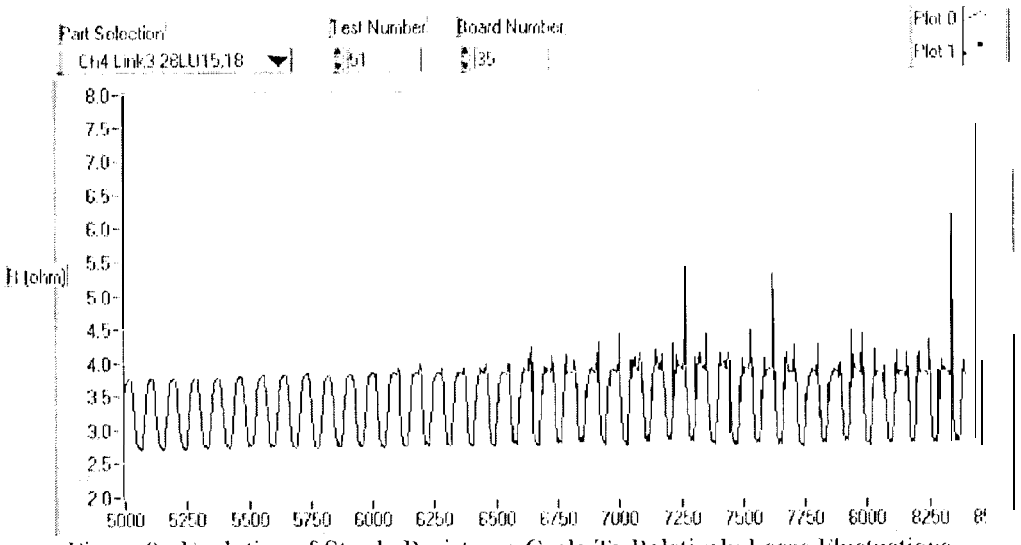

Figure 9: Evolution of Steady Resistance Cycle To Relatively Large Fluctuations

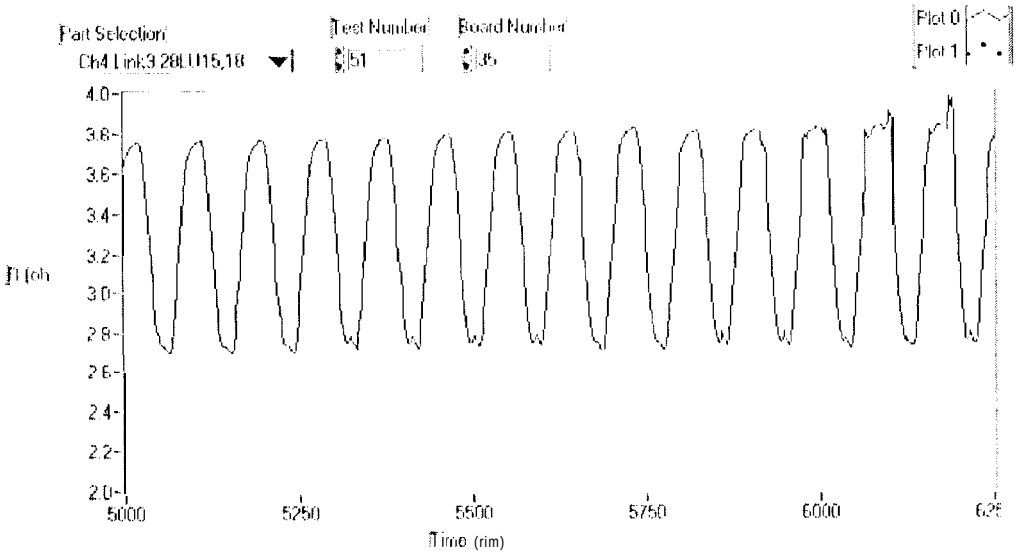

Figure 10: Zoom On Initial Resistance Damage

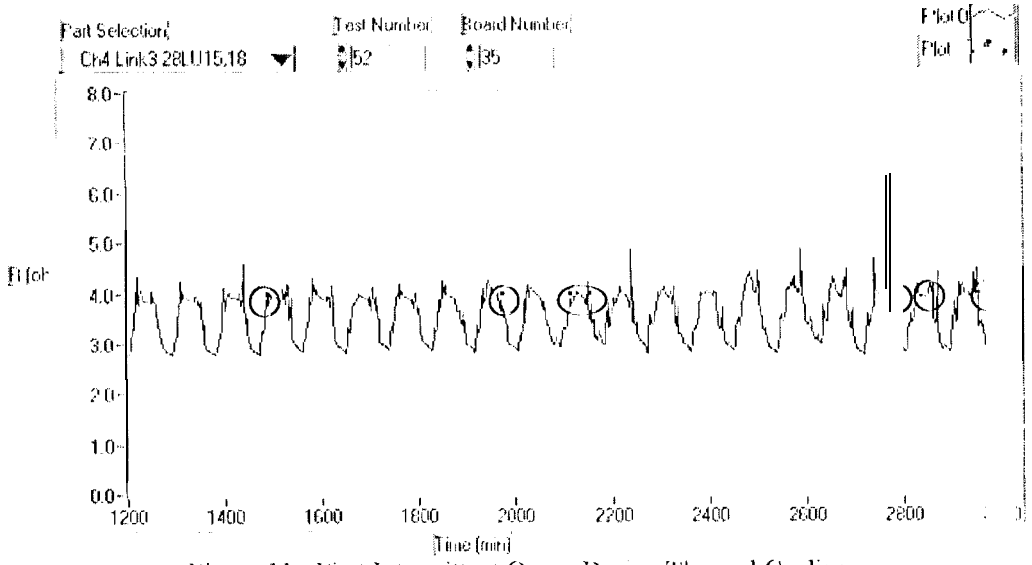

Figure 11: First Intermittent Opens During Thermal Cycling

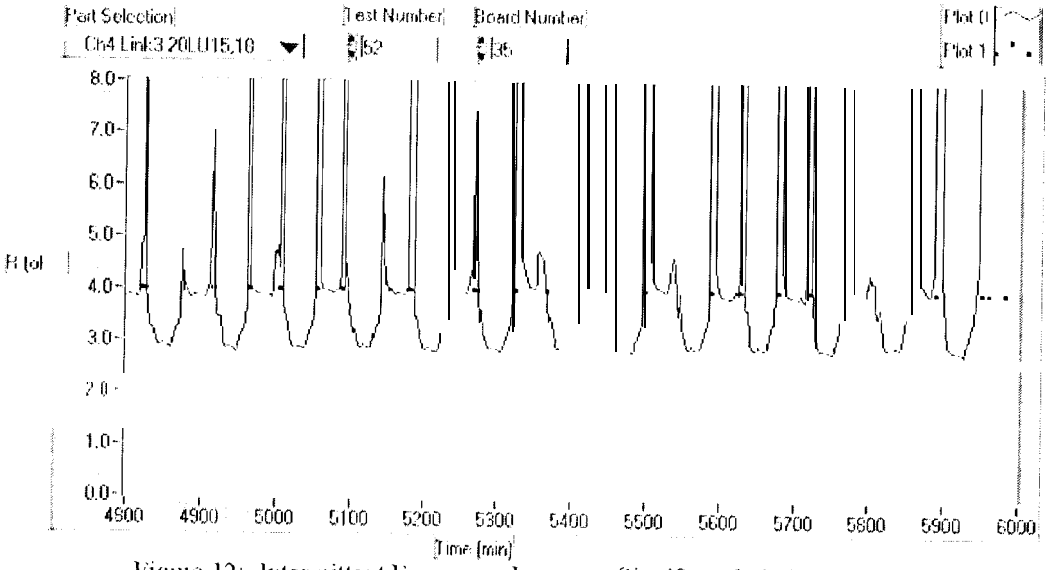

Figure 12: Intermittent Frequency Increases Significantly With Cycling

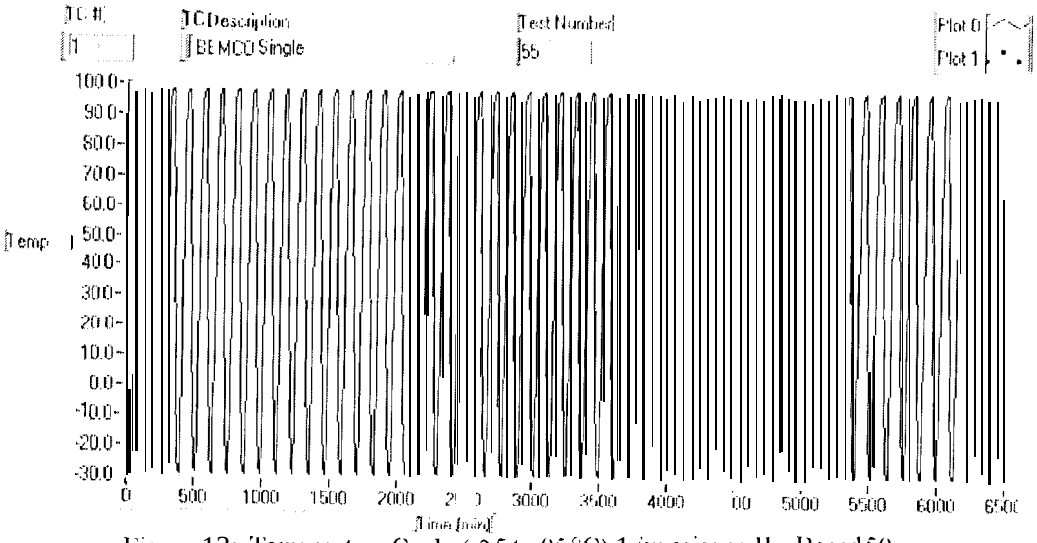

Figure 13: Temperature Cycle (-25 to 95 °C) Experienced by Board 59.

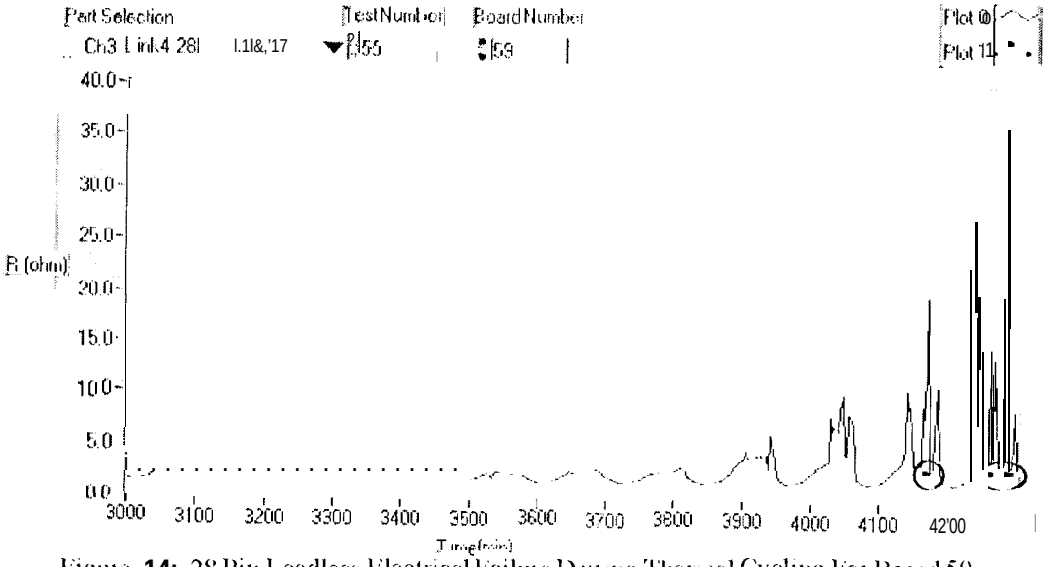

Figure **14:** 28 Pin Leadless Electrical Failure During Thermal Cycling For Board 59.