CBGA/PBGA FOR HIGHLY RELIABLE APPLICATIONS

by
Reza Ghaffarian, Ph.D.
Jet Propulsion Laboratory
California Institute of Technology

Abstract

The Jet Propulsion Laboratory (JPL) is currently assessing the use of Ball Grid Arrays (BGAs) for National Aeronautics and Space Administration (NASA) spaceflight applications, This work is being funded through NASA Headquarters, Code Q. The objectives are to demonstrate the robustness, quality and reliability of BGAs technology, and to assist in the development of the rapidly growing industrial infrastructure for this technology. JPL has solicited industrial, academic and other related consortia to work together to leverage the related efforts into a synergistic effort Initial results of these activities will be summarized and presented in this paper.

Objectives

NASA Headquarters, code Q, has established the Advanced Interconnect Program (AIP) to address the common needs of NASA programs in electronic packaging. One of these programs, funded during 1993-1995, focused on the use of Surface Mount Technology (SMT) for high reliability, Ultra Low Volume (ULV) spacecraft electronics. Another program funded during 1994-1996 concentrated on evaluation of the quality and reliability of BGAs.

Significant characteristics of SMT technology were determined by four projects at JPL. These projects were interdependent and were conducted concurrently. Each project concentrated its efforts on a particular aspect of the design, modeling, manufacturing, test, or deployment (aging) cycle. In the 1996 Nepcon West proceedings, the author referenced some relevant publications in these areas and presented the results of solder joint quality and reliability correlations for standard SMT assemblies.

Similarly to the SMT projects, many aspects of BGAs were investigated. The objectives of the BGA project were to demonstrate the robustness, quality, reliability, and to assist in the development of the rapidly growing industrial infrastructure for this technology. BGAs are electronic packages used for higher 1/0 (input/Output) counts that also provide improved electrical and thermal performance, as well as more effective manufacturing and ease of handling, compared to conventional Surface Mount (SMT) leaded parts.

To meet requirements of the NASA community, including JPL, for highly reliable assemblies in an Ultra-Low Volume (ULV) environment, an integrated system approach was used. The foci included identification of BGAs' critical manufacturing parameters, evaluation and development of inspection techniques, and determination of the effects of manufacturing defects on solder joint reliability, The Quality Assurance (QA) procedures developed will then be integrated into design and manufacturing so that critical parameters can be bounded and controlled.

JPL solicited industrial, academic and other related consortia to work together to leverage their resources and expertise into a synergistic effort. All participants furnished in-kind contributions. The wide industrial use of BGA technology will afford NASA as well as consortium industries inexpensive access to this technology and support miniaturization thrusts for their next generation applications.

The consortium objectives were to complete the characterization of BGAs in the following areas:

- Processing/assembling Printed Wiring Boards (PWBs) using BGAs. Variables included PWB material types and surface finishes, and use of ceramic and plastic packages with different ball populations and I/Os.
- Identifying inspection and Quality Assurance (QA) methods for ascertaining the process controls, acceptance methodologies, and final quality of BGA assemblies.
- Characterizing package properties such as coplanarity, inspection for solder joint quality, damage progress during environmental exposure, and defect/reliability correlation, as well as estimating solder joint life.
- Investigating the reliability of BGA assemblies in several different environments (thermal and dynamic).

Background

Introduction

The production of surface mount assemblies (SMAs) now surpasses assemblies using through hole technology (THT). In SMT, components are mounted and terminated directly onto PWB surface. One of the most important component parameters is the lead pitch, which is continuously decreasing to meet the need for higher I/O count,

The use of fine and ultra fine pitch (FP and UFP) components with less than 0.020 inch pitch is growing, often resulting in more than 200 leads for a single device. Typically, these components have gull wing leads. FP and UFP components, in addition to being extremely delicate and easily damaged during handling, are also difficult to process and rework, and are prone to misalignment with the associated reliability implications.

BGA is an important emerging technology for utilizing higher pin counts, without the attendant handling and processing problems of the peripheral array packages (PAP). Unlike PAPs, BGAs have balls, covering the entire area, or a large portion of the area on the bottom of the package.

BGAs offer several distinct advantages over FP and UFP SMCS that have gull wing leads, including:

- High pin counts, generally> 200.
- Larger lead pitches, which significantly reduces the manufacturing complexities for high I/O parts.
- Higher packaging densities, since the lead envelope for the gull wing leads does not apply to BGAs; hence, it is possible to mount more packages per board.
- Faster circuitry speed than gull wing SMCS because the terminations are much shorter.
- Better heat dissipation than gull wing leaded SMCS because of providing lower path from die to PWB for heat dissipation.

BGAs are also robust **in processing.** This stems from their higher pitch (0.050 inch typical), better lead rigidity, and self-alignment characteristics during reflow processing.

BGAs, however, are not compatible with multiple solder processing methods and individual solder joints cannot be inspected and reworked using conventional methods. In ultra low volume SMT assembly applications, e.g. NASA's, the ability to inspect the solder joints visually has been standard and is a key factor for providing confidence in solder joint reliability.

Consortium Team Members

At the start of the project, in January of 1995, a core of consortium team members was formed. Its members included Hughes, Boeing, and RIT. In weekly teleconferences, the consortium defined their needs, shared their experience and strengths, and knowledge gained on BGA technology through their independent literature searches. Consortium members visited companies with experience in BGAs to better understand the state of the technology and the areas that the consortium could address to add value to the advancement of technology.

JPL organized a workshop on 3 March 95 to have face-to-face information exchange among the core consortium team members and new participants. Participation by Interconnection Technology Research Institute (ITRI) and SEMATECH, a visionary organization in electronics technology, permitted further narrowing of the project focus activities, ITRI, a focal point for the collaboration among the industries, was key in facilitating future expansion of the consortium into the commercial sectors. The consortium shared invaluable information, and built further confidence in BGA technology. Variables for the test matrix definition were ranked based on the current and future needs of the consortium.

The test matrix went through many revisions as new members joined and was finalized by September '95 when Akron agreed to fabricate both FR-4 and polyimide PWBS and Celestica agreed to assemble most of the test vehicles. The organizations that have been an integral par-t of the consortium activities are as follows:

- **Military sectors-** Hughes Missile Systems Company (HMSC) designed the PWBS, Boeing Defense and Space Group performed environmental testing for military applications. Loral (Lockheed-Martin), Canada, offered to assemble and test validated the reliability of an additional 200 test vehicles using the consortium test matrix and test vehicle design.
- **Commercial facilities-** Amkor/Anam Electronics, Inc. provided more than 700 plastic packages, Altron Inc. fabricated 300 PWBS using FR-4 and polyimide materials, Celestica, Canada, assembled 200 test vehicles, Electronics Manufacturing Productivity Facility (EMPF) performed environmental testing, American Micro Devices (AMD) provided resistive die, IBM provided ceramic packages at a minimum charge, Nicolet assisted in X-ray, and View Engineering measured coplanarity and warpage of packages using their 3-D laser scanning equipment.
- **Infrastructure-** ITRI established by the Institute for Interconnecting and Packaging Electronic Circuits (I PC) has provided a vehicle for collaboration among the various sectors of electronic interconnection industries,

- Academia- Rochester Institute of Technology (RIT) assembled 35 test vehicles. More than 20 industrial advisors including people from JPL are helping to redirect the RIT metal manufacturing laboratory into a Computer Integrated Electronics Manufacturing (CIEM) facility to better meet the current national demand for electronics manufacturing engineers.

Technical Issues

ITRI's presented viewgraphs at the JPL Workshop depicting the relationship between pin count and cost/performance. It was apparent that peripheral leads will soon fall short of meeting advanced packaging requirements. Cost/performance requirements for QFPs to meet near term future requirements were even more disparate. However, for BGAs there was a wide range of 1/0, pitch, and sizes meeting both a near term demand and expected future long term requirements.

In reviewing packaging, technology trends, SEMATECH forecast different types of electronic packages for surface mount applications. These included plastic quad flat pack (QFP), plastic ball grid array (PBGA), ceramic ball grid array (CBGA), and thin tape carrier packages (TCP). Comparison of low, medium and high I/O counts were presented. There were QFP packages in the medium range while at high I/O count only BGAs and TCPS were cost/performance competitive.

Many other technical issues were discussed related to the selection of test matrix parameters for the investigation. Issues discussed included:

- Further definition of test vehicles based on the objectives and needs of industry.
- Pretesting before evaluation for test vehicle optimization.
- Need to leverage the work performed by others. Enough data were available that many manufacturing variables did not have to be considered.
- SEMATECH project data on cost/performance was used to better define test vehicles.
- Industry standard practices, or as close to them as possible, needed to be used for the test vehicle design and the manufacturing variables.
- Use of the JEDEC standard for pitch size. There were no standards for many component types. IBM and Motorola had their own standards.
- FR-4 was ranked high and then polyimide. FR-4 is widely used and also has larger differences in Coefficient of Thermal Expansion (CTE) with BGAs, compare to polyimide. FR-4 would provide the most conservatively reliability test results.
- The 300 I/O BGAs were considered to be norm where BGAs compete with leaded packages. The 600 I/O would be expected in the near future in BGA packages. Both plastic BGA and ceramic BGA packages needed to be evaluated.
- No interest at this time in evaluation of ceramic column grid array because it was not expected to be commonly used and there was no plastic column grid array for reliability comparison.
- Evaluate both full array and peripheral array because of concerns about the reliability of solder joints under the die.
- Characterization of solder paste is important.
- Solderability is important and must be evaluated. At the package level solderability is OK, but at the assembly level solderability needed to be tested.

- It was very important to use dies even though costly. Regarding power cycling, resistive die were used.
- Underfilling was generally done to promote thermal enhancement and vibration tolerance, but did not contribute to reliability,
- The JPL study indicated the importance of vibration and mechanical shock. The effect of vibration needed to be investigated further.
- Only edge balls could be detected visually and by SEM. The best way to monitor crack initiation and propagation needed to be defined.
- JPL previously used Anatech® to continuously monitor for electrical opens. New monitoring systems with less noise wereneeded. Cross-sectioning could also be done.
- It was the ball height after reflow, rather than the ball size that was thought to affect solder joint reliability.
- Solder volume was said to be more critical for some types of package than others. It was important to include solder volume as a variable in the Design of Experiment (DOE) test program.
- Surface finish plating, i.e., hot air leveling (HASL), or use of organic solder preservative (OSP) are important and should be considered.
- Solder mask was shown to be a factor affecting reliability.
- Need to look into underfilling and conformal coating as affecting reliability.

Subsequent to the Workshop and after extensive discussion and further ranking of the variables discussed, the following most critical issues were identified:

- Determine a suitable inspection technique for BGA packages, particularly after they have been attached to the substrate. Evaluate:
  - X-ray systems: Nicolet, Fein Focus, and Four Pi
  - Acoustic imaging systems; Sonoscan
  - Visual inspection for peripheral solder joints
- Decide the optimal package type array configuration.
  - Peripheral array versus full area array and depopulated packages
  - Overmolded plastic vs. metallic version (Super BGA)
- Characterize the reliability differences between ceramic and plastic BGAs.
  - Thermal cycling including a military version and power cycling
  - Vibration behavior
  - Robustness and reliability compared to fine pitch QFP
- Assess the **various techniques** for reworking AAP/BGA packages.

Ceramic and Plastic Package Dimensional Properties

Packages

Packages cover the range from OMPAC to SuperBGAs from Amkor/Anam. In SBGA, the IC die is directly attached to an oversize copper plate providing a better heat dissipation efficiency. The copper plate also acts as a stiffener and ground plane for the package. The solder balls for plastic packages are eutectic (63 Sn/37Pb).

Ceramic packages were from IBM, Ceramic solder balls have 0,035 inch diameters and have a high melting temperature (90Pb/10Sn). These balls are attached to the ceramic substrate with eutectic solder (63 Sn/37Pb) material. At reflow, substrate eutectic material and the PWB eutectic paste reflow to provide the electro-mechanical interconnects,

Figures 1 shows Scanning Electron Micrograph (SEM) photos of ceramic packages with 625 1/0s with straight and tilted solder balls.

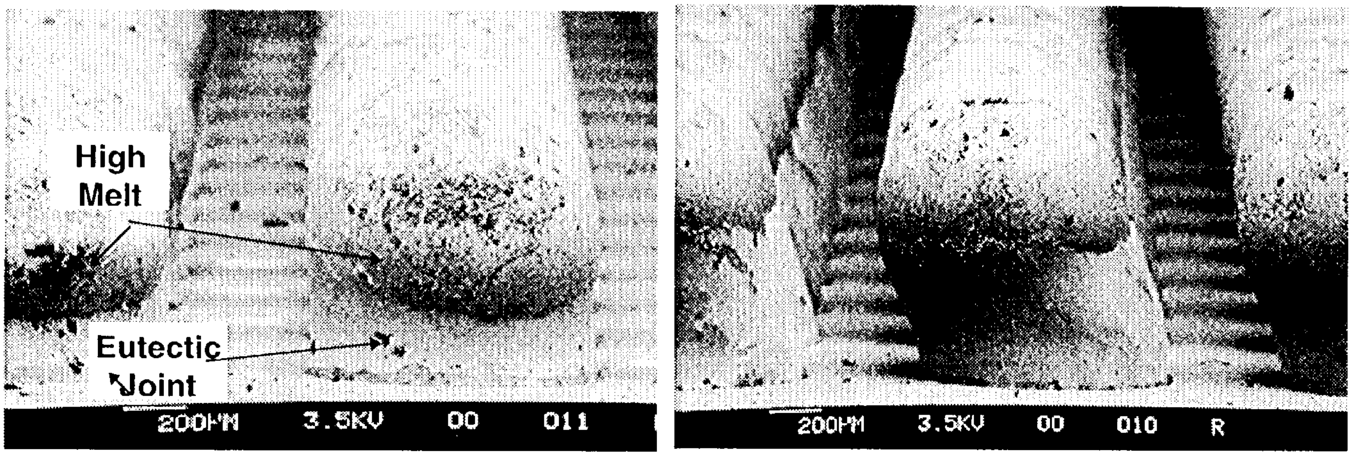


Figure 1 Solder Balls With no Tilting (left) and with tilting in 625 CBGA

Package Dimensional Characteristics

Package dimensional characteristics are among the key variables that affect solder joint reliability. Dimensional characteristics of all packages were measured using View Engineering 3-D laser scanning system. Output of measurements included solder ball diameter, package warpage, and coplanarity.

Package coplanarity is defined as the distance between the highest solder ball (lead for QFP) and the lowest solder ball. Coplanarity can contribute to the yield of surface mount manufacturing as well as long-term solder joint integrity. For leaded parts such as QFP, nonplanarity in excess of 0,003 inches is not acceptable. JEDEC specification for coplanarity requirement was 0,006 inch which increased to .008 inch.

In this paper, the results of package properties for 625 CBGA and 560 Super BGA will be given only. These data are being used to determine the influence of these parameters on the solder joint number of cycles to failure.

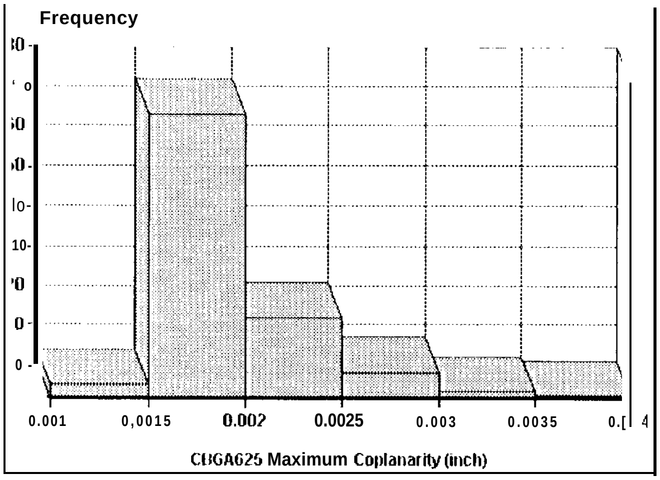
Dimensional Characteristics for CBGA 625

Figure 2 shows histogram plots of coplanarity and warpage distributions for 108 ceramics with 625 1/0s and coplanarity distribution for a package with the maximum coplanarity of 0.0042 inch. Results from these and similar plots are:

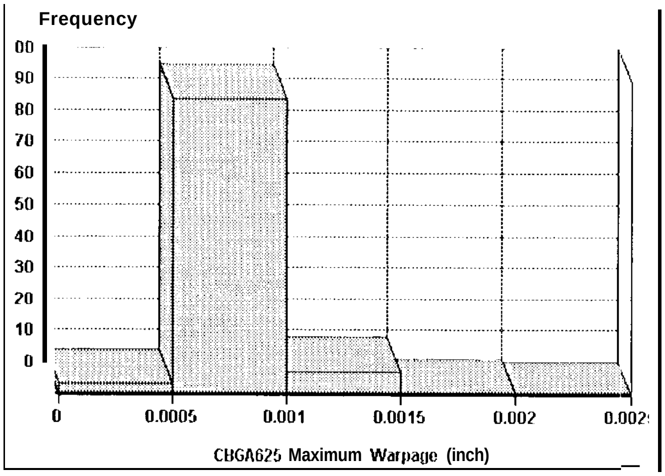
- The balls' coplanarities were 0.0015 to 0.002 inches for 104 parts and 0.003 to 0.0042 inches for 4 pads.
- Maximum solder ball diameters were 0,0315 to 0.0334 inches with minimums 0.028 to 0.029 inches. Diameters were measured only for 36 parts.

. Maximum warpages were 0005 to 0.0029 inches.

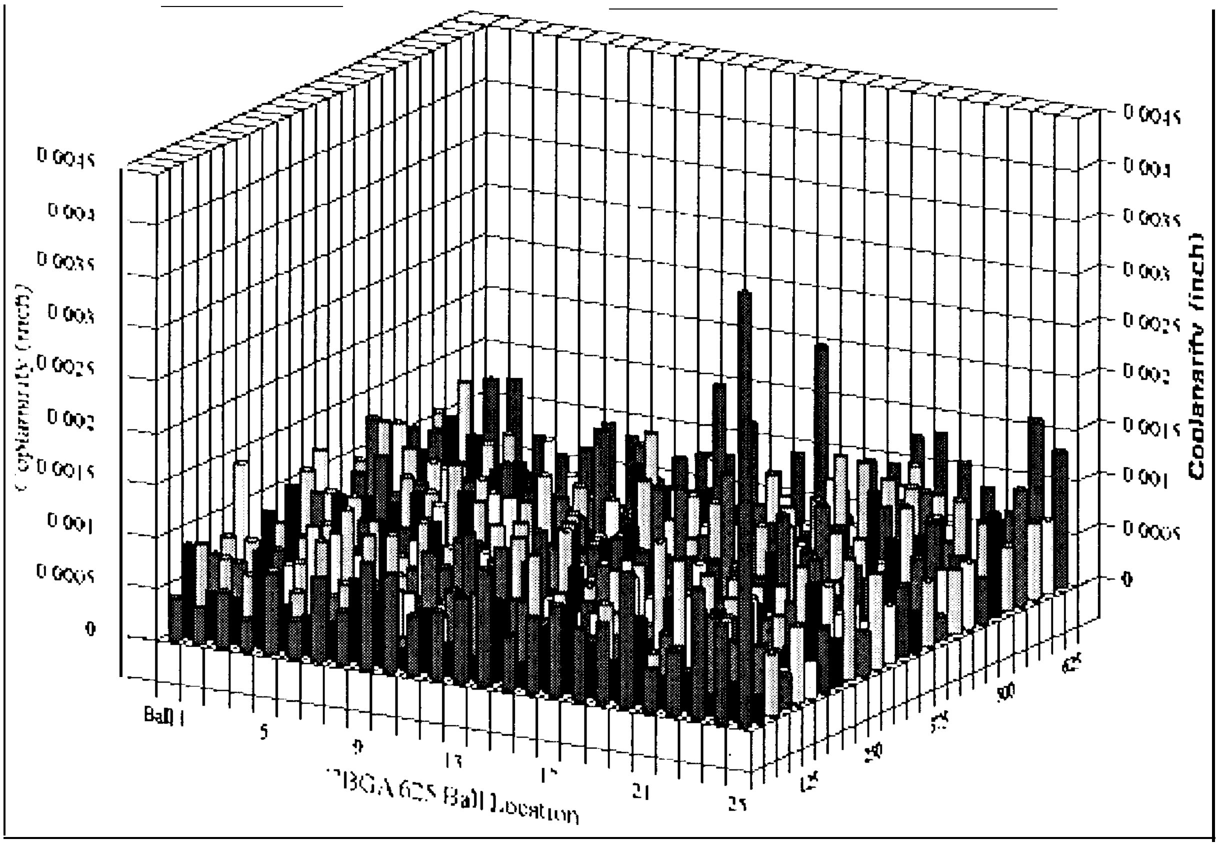
The coplanarity distribution plot for this part reveals that the solder balls were generally uniform in height with a few at two extreme levels that were randomly distributed.



a) Maximum Coplanarity Distribution



b) Maximum Warpage Distribution



c) Coplanarity Distribution for a CBGA 625 Package

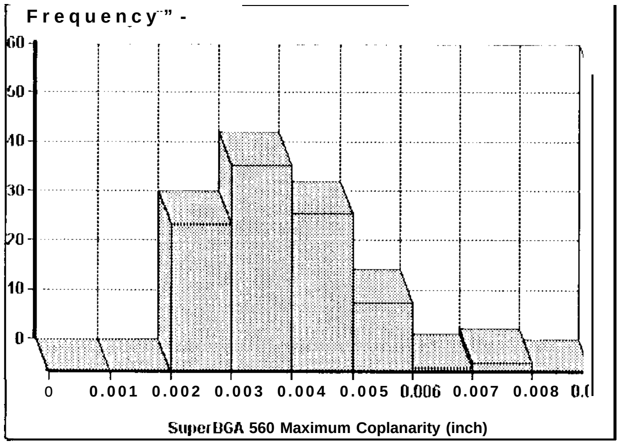
Figure 2. Package Dimensional Characteristics of Ceramic BGA with 625 1/0s

Dimensional Characteristics of SuperBGA 560

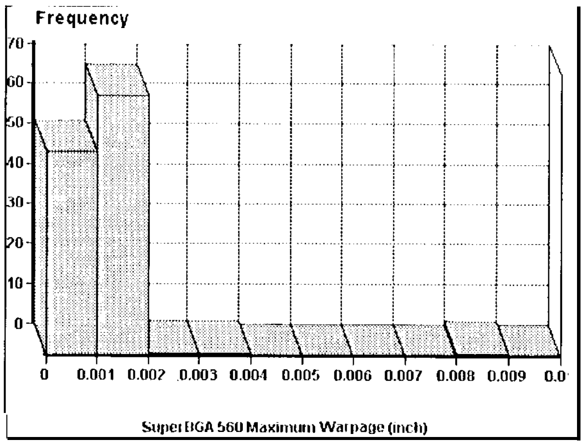
Figure 3 shows histogram plots of coplanarity and warpage for 120 SBGA560 and the coplanarity distribution for a package with the maximum coplanarity of 0.0054 inch. Results of these and similar plots are as follows:

- Bali coplanarities were 0.002 to 0.004 inches for 72 parts, 0.004 to .006 for 45 parts, and 0.006 to 0.00766 for 4 parts.
- Maximum solder ball diameters were 0.0275 to 0.0290 inches, minimums were 0.0213 to 0.0263 inches.
- Maximum warpages were 0.00165-0,0096 for 110 packages, 0.01012-0.021 inches for 8 packages, and 0.034 inches for one package.

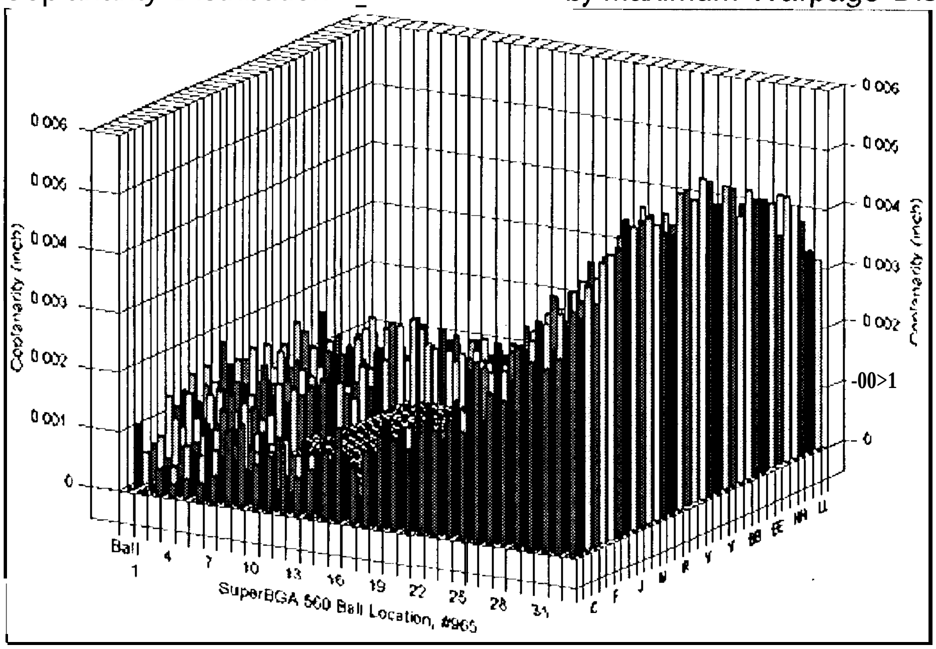
The coplanarity distribution plot for this part reveals a nonuniformity where one region shows higher heights than the other. Such nonuniformity could cause package lifting during reflow; thus, increasing the likelihood of manufacturing defect formation.



a) Maximum Coplanarity Distribution



b) Maximum Warpage Distribution



c) Coplanarity Distribution for a SuperBGA 560 Package

Figure 3. Package Dimensional Characteristics of SuperBGA with 560 1/0s

Solder Ball Diameters

Solder ball diameters as measured by View Engineering do not agree with the values reported by IBM. Ceramic packages use high melting solder balls with 0.035 inch diameter. The values from the 3-D laser images for both 361 and 625 1/0s were lower than 0.035 inch. In IBM's recent random measurements of ball diameter measurements of 50 out of 300,000, as part of their incoming inspection, the values were within their ball diameter specification.

One possibility is that even though the View Engineering system is accurate for measuring coplanarity and other dimensional parameters, it is not accurate for solder ball diameter measurement. A solder ball diameter is calculated from a mathematical curve which is fitted to the laser image of the ball. Therefore, the estimated diameter depends on how well the fitted curve is representative of the actual shape of the ball.

Another possibility could be due to the tilt and skewness of solder balls as shown in Figure 1. The tilt could cause distortion in the image detected by laser scanning, resulting in different values than those reported by IBM. Diameter of solder ball were measured using the SEM as shown in Figure 1: it was found to be 0,0355 inch.

Conclusions

- Solder ball planarities were significantly higher for plastic than for ceramic packages. PBGAs, however, are more robust and the large planarity values might not be a detriment on the solder joint reliability. Some planarity differences among the balls are accommodated by their collapses during the reflow process. This is not the case for CBGAs where high melt solder balls remain intact during reflow. The solder ball diameter controls the stand-off height which is a key factor to solder joint reliability.
- 3-D laser scanning is excellent for characterization of package dimensions, but possibly not for solder ball measurement. It did read lower values for ceramic solder ball diameter than was actually true. One possible cause could be due to the skewness of the ceramic solder balls observed visually and by SEM.

Acknowledgments

The research described in this publication is being carried out by the Jet Propulsion Laboratory, California Institute of Technology, under a contract with the National Aeronautics and Space Administration. I wish to acknowledge the in-kind contributions and cooperative efforts of BGA consortium team members including: P. Barela, K. Bonner, K. Yee, S. Bolin, C. Bodie, S. Walton, *JPL*; M. Andrews, *ITRI*; S. Lockwood, M. Simeus, P. Drake, *HMSC*; 1. Sterian, B. Houghton, *Celestica*; M. Ramkumar, *RIT*; S. Levine, R. Lecesse, *Altron*; P. Mescher, *AMKOR*; **N.** Kim, ***Boeing;*** W. Goers and J. Mearig, *EMPF*; M. Cole, A. Trivedi, *IBM*; and T. Tarter, *AMD* F, Schlieper, C. Walquist, *Nicolet*; R, Dudley, R. Balduf *View* ***Engineering,*** W. Szkolnicki, *Loral (lockheed-Martin)*. My deepest appreciation to others who had or are being contributing to the progress of both programs.