Case Study of the Design of a Viterbi Decoder

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This paper describes the design of an ASIC performing the Viterbi decoder function with a constraint length of 15 and at a speed of 4.4 Mb/s. The architecture of the chip is described, as well as the design challenges which were overcome. Some of the challenges included a large amount of I/O, application of low-noise interconnection scheme to reduce the ground noise of the system, and low-voltage signaling. High chip complexity at 970k transistors for logic and 54k bits of RAM, transfer of data between ASICs at system clock speeds, and internal data path speed at 62 MHz. The author also describes the successful application of the design system.

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