QUALIFICATION OF BALL GRID ARRAY ASSEMBLIES FOR SPACE FLIGHT APPLICATIONS

by

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Background

JPL, in partnership with an industrial consortium, is engaged in the investigation of reliability and quality issues of ball grid array (BGA) packages for space flight electronics applications. This effort is funded in part by NASA R&D funding and partly by the industry partners contributing IRAD funds. JPL is the lead in this consortium with the others supplying parts, assembly labor, printed wiring boards, and design of the test printed wiring boards. JPL is also performing a significant portion of the laboratory tests on the samples to determine the reliability of the interconnections of the BGA packages to the printed wiring boards (solder joints).

Approach

It was recognized early in the program that a large number of the BGA solder joints would be under test simultaneously and that some sort of computer based assistance would be required to accurately track the failures and the time at which they occurred. The test plan called for over 1500 channels of data, each channel representing up to 150 solder joints to be monitored 24 hours a day over the duration of temperature cycling. The plan is to cycle to complete failure. At the initiation of the project, the test capacity at JPL met approximately one-tenth of this requirement. A detected channel failure was not only to be identified as to the particular card and channel, but also to be correlated with the real time of failure, temperature at the time of failure, and the total number of temperature cycles experienced by the particular channel from start to failure. However, it was also recognized that the purpose of the NASA R&D funds was primarily to investigate ball grid array interconnects and not to design and develop test instrumentation. Therefore, the approach adapted was to use off-the-shelf hardware and software and to minimize development. This approach was, in the main, quite successful, but some development, particularly in the software arena, was found to be necessary.

JPL has been using the National Instruments LabVIEW™ software and has collectively a great deal of experience in its application to laboratory testing. National Instruments also offers an assemblage of hardware which complements the software operating system. As an added attraction to the BGA solder joint reliability team, the JPL equipment loan pool owned sufficient inventory of software and hardware so that the project could rent and return it at the end of the investigation, thus minimizing the costs to the project.

Test article

The BGA test assemblies were specifically designed for testing solder joints. Each test board consists of four BGA packages, with each part having four daisy chains. Each of these daisy chains represents one channel monitored by the system. There are two types of test assemblies. Type I, shown in Figure 1, consists of a 352 SBGA (Super BGA), 361 CBGA (Ceramic BGA), 352 OMPAC (Overmolded Pad Array Carrier), and 313 PBGA (Plastic BGA). Type II consists of a 560 SBGA, 625 CBGA, 256 BGA, and a 256 Gullwing. The test assemblies were designed so that any quarter of the board could be cut out without interfering with the remaining test assemblies by creating four separate

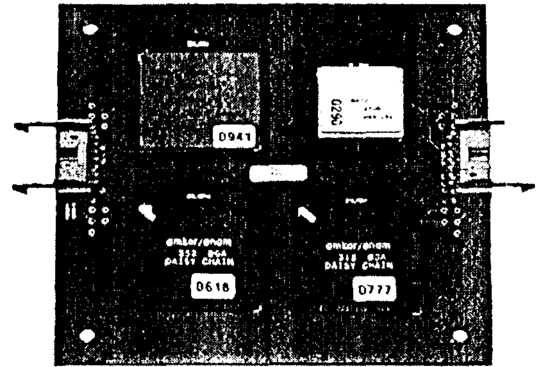

Figure 1. Type I BGA Test Assembly

ground planes. There is a pad for each of the daisy chains and the ground plane on the test boards. This makes failure verification and inspection much easier. The resistance of each daisy chain can easily be measured with an ohmmeter by probing the corresponding pads. These pads also make it easy to wire bond any daisy chains/channels that need to be closed. Special racks were designed and built to hold the maximum number of test boards in the JPL thermal chambers. Figure 2 shows a thermal chamber with loaded test racks.

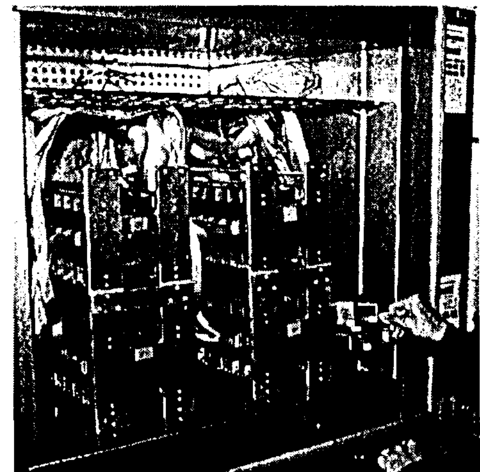

Figure 2. BGA Test Boards in the Thermal Chamber

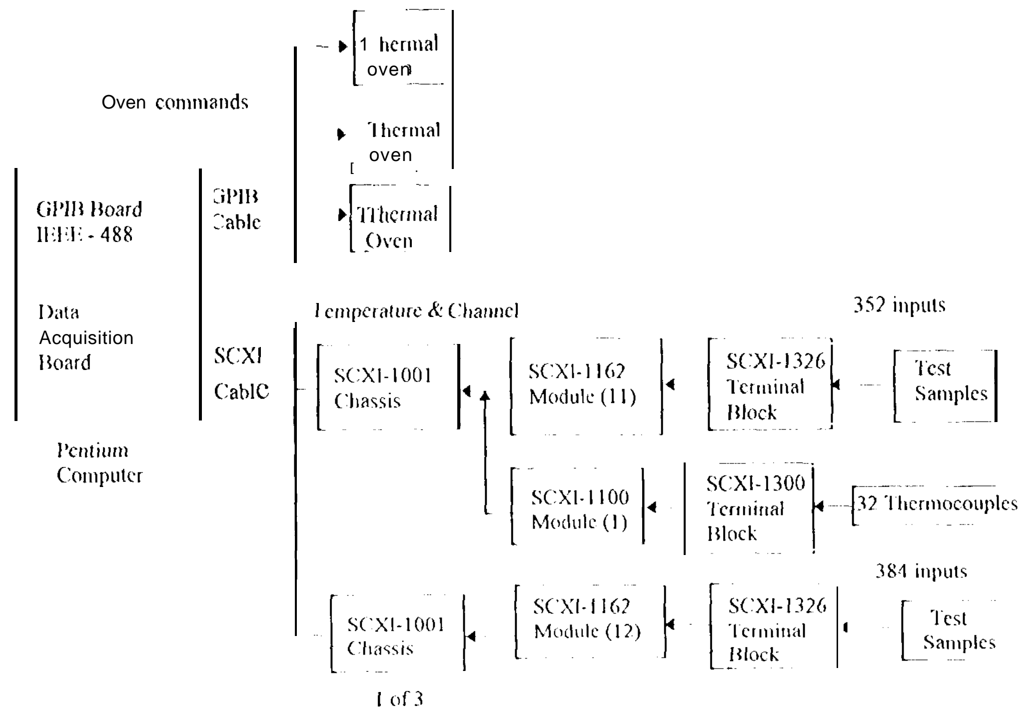

Figure 3. Instrumentation System Block Diagram

Detailed Description Of The Test Setup

The data acquisition system program, DAQ.VI, was written around the LabVIEW graphics based operating system and using the hardware handlers provided by National Instruments The program controls the temperature chambers, gathers the data from the inter face cards, logs the data onto a spread sheet type data base, and provides operator interface for ease of operation. Figure 3 is a block diagram of the laboratory test system

The software is installed in a Pentium Personal Computer which also contains a National Instruments IEEE-488 General Purpose Interface Bus (GBIB) Board and a special Data Acquisition (DAQ) hoard Model AT-MIO- 16E-10 also supplied by National Instruments Connected to the GPIB board are three Thermotron® thermal chambers. This bus can be expanded to control other devices such as power supplies for the cycling of heating elements mounted on the BGA devices to simulate the heat that active devices would normally dissipate.

The DAQ board is connected to National Instruments SCXI hardware interface modules installed in four National Instruments card cages The SCXI hardware consists of 4 SCXI-1001, 12 card chassis, 47 SCXI-1 162 discrete input modules, and I SCXI-1 100 thermocouple input module for a total capacity of 1504 discrete inputs and 32 temperature inputs

The Discrete Input module (SCXI-1 162) is a 32 channel device with optical input coupling Input isolation provided by the optical **coupler** front cod of this module was considered to be a prc-requisite because of severe ground loop noise problems encountered with other instrumentation schemes that had been used in the test laboratory, The relatively low input impedance of the front end , 360 ohms, also helps tight the electrical noise inherent in the environment of the test facility. Figure 4 is a block diagram of the input stage of the module.

The thermocouple module provides 32 channels of input which provides for the measurement of local temperatures (i.e. in the viciniry of the test samples).

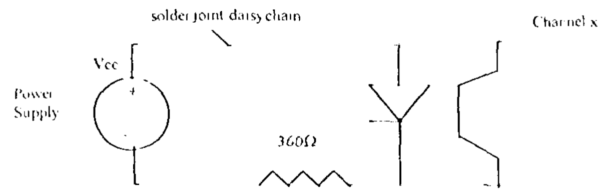

Figure 4. Input Block Diagram

The BGA packages are wire bonded internally so thar when combined with the circuitry on the test PWB a daisy chain of up to 150 solder joints is formed Each discrete input channel monitors one such daisy chain by detecting the presence or absence of approximately 7 milliamps of current through the LED portion of the optical coupler device

When a solder joint breaks, the current will not be able to pass through the solder joint, so the LED will not get the current it need< to light When the LED is turned off, the light sensitive transistor sends back a logic high to the computer telling the computer that something is wrong with the channel The computer reads rhc logic high and knows that a solder joint has failed.

The DAQ.VI program will display an event (a circuit either opening or closing,) along with a message that shows the channel number, test board number, board location, time, cycle number, date, and temperature that the event occurred Figure 5 is a depiction of the operator interface displayed on the computer monitor. It was decrned important to record both openings and closing, of the circuit to detect intermittants if they occur.

This information is also written to a file that can be brought Lip in a spreadsheet program DAQ.VI also keeps track of the number of thermal cycles each board accumulates, the board location, serial number, and its corresponding channels (16 per board).

The assembled National Instuments haradware, cables, and power supplies are shown in a rack in Figure 6.

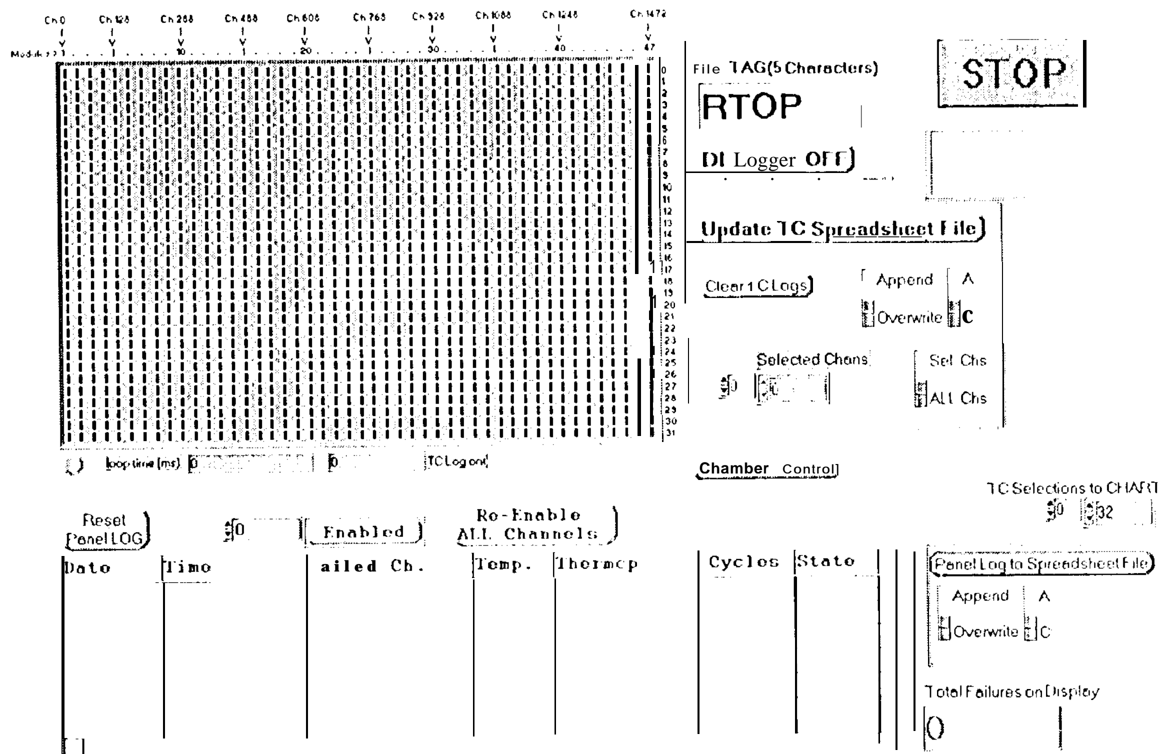

Figure 5. Operator Interface Display

Figure 6. Test Hardware

Results To Date

Thermal cycling of the test assemblies began in May 1996. The test assemblies arc subjected to a thermal cycle with a temperature range from -30°C to 100°C, with dwell times of 20 minutes and 5°C/min ramp rates. A complete cycle takes just over 90 minutes. As of September 1996 the test assemblies have 1400 cycles. The failures, to date, arc mostly in the ceramic package daisy chains. There have been no failures in any of the other packages.

Conclusion

JPL has developed an instrumentation system for the testing of solder joint reliability and longevity. This software/hardware system greatly simplifies the task of monitoring and tracking failures and the coalitions when the failures occurred of a large number of solder joint channels through the automatic gathering and recording of the test results onto a personal computer database.

Acknowledgments

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