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ADVANCED FLIGHT COMPUTING TECHNOLOGIES FOR VALIDATION BY NASA'S NEW MILLENNIUM PROGRAM

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ABSTRACT

The New Millennium Program (NM P) consists of a series of Deep-Space and Earth Orbiting missions that are *technology-driven*, in contrast to the more traditional *science-driven* space exploration missions of the past, These flights are designed to validate technologies that will enable a new era of low-cost highly miniaturized and highly capable spaceborne applications in the new millennium. in addition to the series of flight projects managed by separate flight teams, the NM P technology initiatives are subsumed by the following six focused technology programs: Microelectronic Systems, Autonomy, Telecommunications, Instrument Technologies and Architectures, in-Situ instruments and Micro-electromechanical Systems, and Modular and Multifunctional Systems. Each technology program is managed as an Integrated Product Development Team (IPDT) of government, academic, and industry partners. In this paper, we will describe the technology roadmap proposed by the NM P Microelectronics IPDT. Moreover, we will relate the proposed technology roadmap to existing NASA technology development programs, such as the Advanced Flight Computing (AFC) program, and the Remote Exploration and Experimentation (REE) program, which constitute part of the existing NASA technology development pipeline. We will also describe the Microelectronics Systems technologies that have been accepted as part of the first New Millennium Deep-Space one spacecraft, which is scheduled for launched in July 1998.

1. INTRODUCTION

The initial plan for the New Millennium Program (NMP) comprised of 6 technology validation missions: three deep-space, and three Earth orbiting missions, with the first launch scheduled for July 1998. Current plans envision the program extending further, as an on-going program for technology validation. The technology planning process is captured by Integrated Product Development Teams (IPDT) of government, industry, and academic partners selected using a competitive process. The six IPDTs include: Microelectronic Systems, Autonomy, Telecommunications, instrument Technologies and Architectures, In-Situ instruments and Micro-electromechanical Systems, and Modular and Multifunctional Systems. The primary responsibility of the IPDTs is to continuously roadmap, rank, select and deliver technologies for validation on the New Millennium flights. This is a team effort that requires participation of diverse and often competitive industrial partners working towards a common god. After flight delivery, the 1l)l)'1's will be involved throughout the technology validation phase, and will be responsible for the transfer of knowledge to future missions. in the following section, we first describe the technologies selected by the NMP Microelectronics Systems 11'1)'1' for roadmapping. These technologies are derived from the basic scientific vision and capability needs for the NMP. In Section 3, we describe the technologies selected for validation on the first deep-space flight. In Section 4, we describe two on-going technology development programs in NASA's technology development pipeline: Advanced Flight Computing (AFC), and Remote Exploration and Experimentation (REE), followed by concluding remarks in Section 5.

2. MICROELECTRONICS SYSTEMS TECHNOLOGY ROADMAP

The competitively selected 11'1)'1' for the Microelectronics Systems technology area consists of the following government, industry, and academic members:

- Government: NASA/JPL, NASA/GSFC, DOD/AF, MIT/Lincoln Lab., and Sandia Nat. Lab.;
- Industry: Boeing, Honeywell, Lockheed MFS, Optivision, Space Computer Corp., TRW;
- Academia: Georgia IT, UC SD, and USC.

The basic capabilities derived from the vision of space exploration in the new millennium consists of two orders of magnitude reduction in mass, volume, and power, for all spacecraft electronics; and a highly autonomous, self-oi~crating spacecraft, with on-board scif-repair, diagnostics, and other highly advanced software systems for on-board scientific data analysis and knowledge extraction. The following is a list of the specific technology areas addressed by the Microelectronics Systems Ii'I)"]' in response to these needs. The fall technology roadmap is outlined in [1], and is beyond the scope of this paper.

- Semiconductor technologies: Continued scaling of semiconductor devices (both front end of the line FEOL, and back end of the line BEOL) represents the fundamental technology upon which other components are built. It is essential to establish a commercially sustainable semiconductor foundry that could be used for the production of radiation tolerant, ultra low-power, devices, circuits, and integrated systems. A potential candidate semiconductor technology is the Sol (silicon on insulator) CMOS technology which has many desirable attributes applicable to space, such as latch-up tolerance, and scaled iow-opcl-sting voltage and thus low-power performance at higher clock rates.
- Advanced processing: The PowerPC architecture and roadmap were selected as the direction for general-purpose CPUs in space. The main reason was the well understood commercial roadmap as well as its broad commercial use. The PowerPC is also being baselined by various commercial satellite systems. Amongst the PowerPC CPU products, our preference was for the 603e low-power roadmap.
- 1,mv-power high-capacity storage: A number of different storage technologies were considered, including: EEPROMs; Flash Memory; and alternative technologies such as:

Vertical Bloch Line (VBL); FeRAM; Magneto-resistive RAM; and ! holographic storage. in the near-tcm, commercial Flash technology maintains the highest non-volatile capacity per ma. In the long-term, technologies such as 1 lolographic storage could reach higher levels of volumetric density (but problems still remain in the technologies for rc.ad/write).

- Low-power I/O: The use of low-power fiber-optic transceivers could potentially enable the use of low-power high-bandw idth, highly reliable serial and parallel communication protocols.
- Advanced packaging technologies: Multichip Modules; 3D chip and MCM stacking. The ultimate volumetric density of electronics is achieved by designing 3D VLSI.
- Power management and distribution: Power Management And Distribution includes high-efficient power conversion (DC/DC); highly integrated solid state switches and device drivers.
- Advanced design autom ation, design for testability and built-in self test: The consistent and complete use of a high-level hardware description (specificatio n) and simulation language such as VHDL for both behavioral modeling, and low-level design and simulation would represent a major breakthrough, relative to the stale of the art. Subsequent design changes should be Illa(lctlsillgl]igll-level design synthesis tools.

3 NMP DS1 MICROELECTRONICS SYSTEMS

Perhaps the most significant challenge to the 11'1)'1" was to roadmap the individual technologies into a meaningful system. An assumption was made that future low-cost avionics architectures for small and micro -spacecraft systems would have to rely on advanced technology development driven by the fast growing commercial semiconductor and consumer markets. Therefore, standard commercial interfaces for both hardware and software were preferred. We selected the use of the commercial Peripheral Component Interface (PCI) high-speed local bus, which is primarily a personal computer local-device bus. The interface to the spacecraft system is via two buses: the avionics standard VME parallel system bus, and the Al AA standard AS 1773 fiber-optic serial bus. in addition, the standard JTAG boundary-scan bus is used for all testing, debugging, and integration. in addition, the commercial VxWorks operating system is used, with the C programmin g language and application interfaces as well. The architecture, as defined using only standard interfaces is modular, and can be tailored for a variety of applications such as: embedded instrument controllers; distributed high-performance and highly available systems; and special-purpose applications. As shown in Figure 1, the NMP J)ccp-Space 1 flight computer architecture consists of 4 slices: the processor slice; local memory slice; non-volatile memory slice; and the I/O slice. Each slice is packaged either using MCM technology, or 3D chip stacking technology. Moreover, each slice is then stacked into a 3D MCM architecture, and mounted on a single VME card. In Figure 1, the four slices arc shown above the PCI bus. Below the I'C1 bus (also in Figure 1), wc show three possible extensions to the. architecture, that would include a I'(;I-slice for the support of an instrument; a PCI slice for the support of a special-purpcmc neural-net co-processor; ma PCI-slice for a connection to a high-bandwidth distributed network architecture for high-performance and high avail ability.

3. ADVANCED FLIGHT COMPUTING PROGRAMS

The NMP Microelectronics System If '1) 'I' roadmap is supported by al least two large technology development programs: Advanced Flight Computing (AFC), and Remote Exploration and Experimentation (REE). AFC's technology elements include: Advanced avionics architectures for 3D MCM stacking; Next Generation PowerPC Architectures; Advanced MCM Design Laboratory; Holographic Storage; 3D Neural Network Architectures; Collaborative Engineering Workbench; Ultra Low Power design for reliability; and Distributed Reliable Computing. The main thrust areas of REE include: Ultra Low Power Electronics materials, Circuits, and systems; and Scaleable Fault Tolerant Computing. The purpose of the AFC and REE programs is to develop technologies that may be selected for validation on future NMP flights.

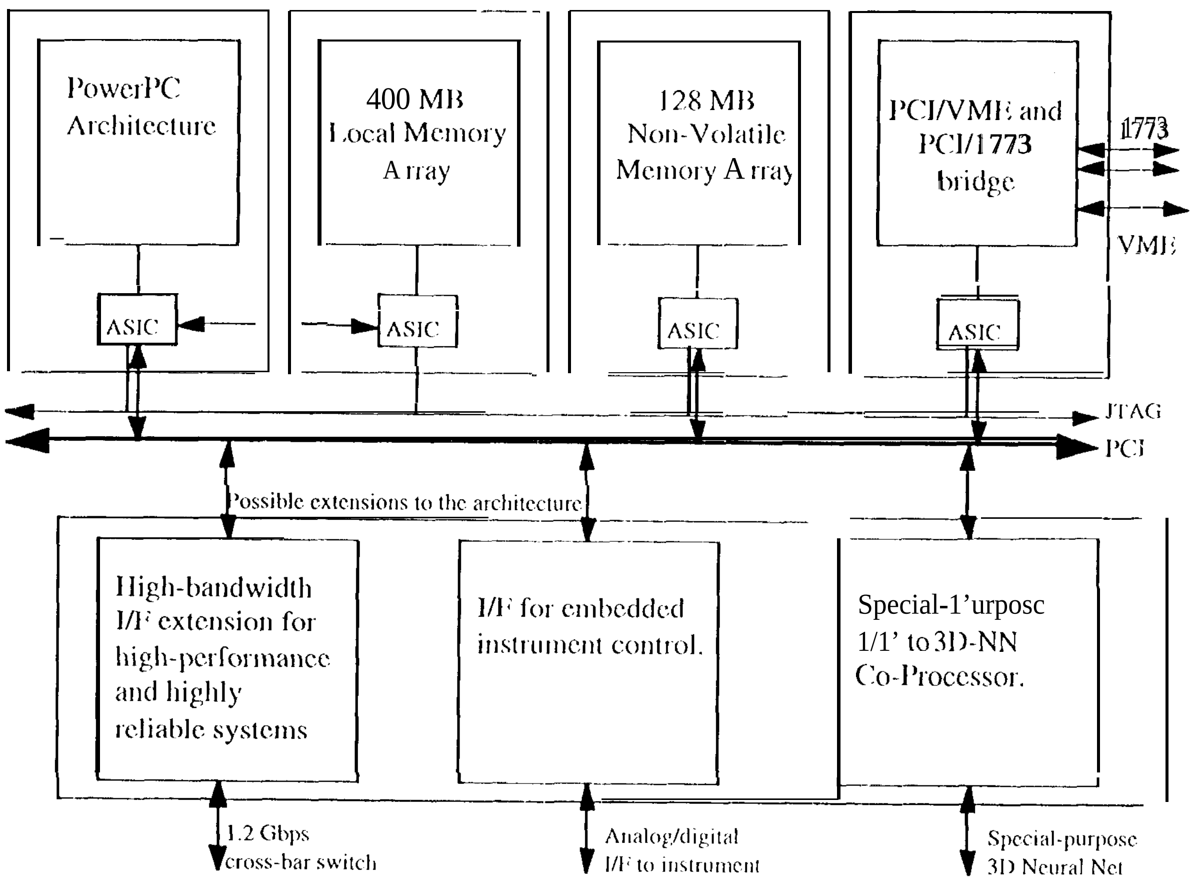

Figure 1. A modular architecture: PowerPC CPU, PCI bus, local memory, non-volatile storage, and I/O. Extensions include: instrument controller, a high-bandwidth link, and a NN co-processor.

4. CONCLUSIONS

NMP is a technology validation program that relics on existing technology development programs to deliver advanced technologies for flight validation. The NMP Ilccp-Space 1 flight