

# Fast Optical Hazard Detection for Planetary Rovers using Multiple Spot Laser Triangulation\*

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**Abstract** A new laser-based optical sensor system that provides hazard detection for planetary rovers is presented. It is anticipated that the sensor can support safe travel at speeds up to 6cm/second for large (1m) rovers in full sunlight on Earth or Mars. The system overcomes limitations in an older design that require image differencing to detect a laser stripe in full sun. The new system ensures the projected laser light is detectable in a single image, eliminating the requirement for additional difference images. The improvement is significant since any reduction in image gathering or processing time provides for faster rover motion. The savings are even more important in the case of a Mars rover since power and radiation-hardening requirements lead to severely constrained computational resources. The paper includes a thorough discussion of design details and tradeoffs for optical hazard sensing that will benefit future efforts in this area.

## I. INTRODUCTION

This article presents a new laser-based optical system for mapping the terrain before a planetary rover. Although some components of the design have appeared in an earlier system, this is the first in-depth discussion of many of the factors involved in the design of both.

Planetary rovers must be able to accurately, quickly, and reliably assess the terrain before them. Several active and passive technologies are available for the task, including IR proximity detectors, "laser radar," stereo vision and structured light. In the case of rovers embarking to other planets, the rigors of space travel and the target planet's environment must be considered. Fragile moving parts like the nodding mirror of a laser

radar might not survive the G-forces of atmospheric entry and landing. In the case of Mars, computing power is another important consideration. Radiation hardening and flight certification for instance, have restricted the Mars Pathfinder rover to an 8085-class CPU. This impacts the processing power available for all tasks including vision. In this context, stereo vision approaches are too costly to provide safe rapid rover motion. Some specific constraints and goals for the hazard sensor system include:

- **Schedule:** Mars exploration efforts will likely accelerate in the next few years. Such flight schedule pressures underscore the importance of using extant technologies to the largest extent possible in rover design.
- **Flight-qualified components:** This is always a requirement for planetary rovers, but development schedule constraints dictate the use of *already* qualified components and materials to the maximum extent possible.
- **Mass:** All sensor systems should be low-mass to provide for larger science payloads and the potential of sample return missions.
- **Power:** Most rover designs utilize solar or battery power for all on-board systems. Mission success and duration depend heavily on power consumption.
- **Mechanical simplicity:** Reliability in space requires mechanically simple systems with few or no moving parts.
- **Computational simplicity:** Reduce image processing demands to a minimum.

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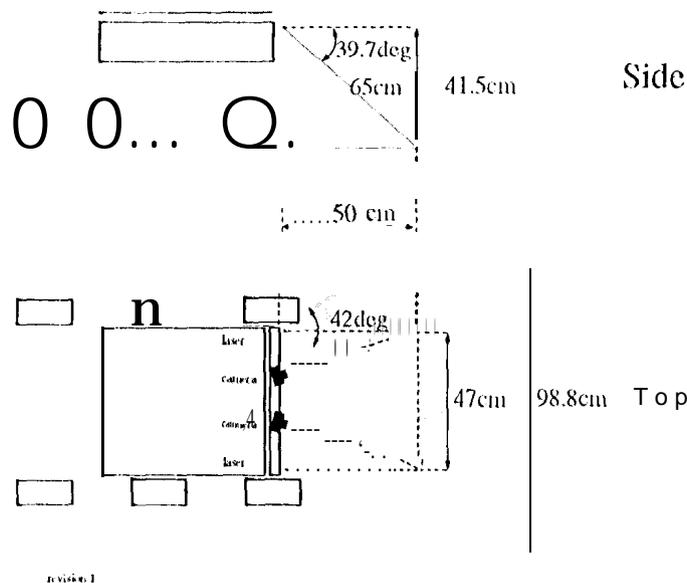


Fig. 1. Laser and camera configuration aboard LSR-1. The shaded areas represent distributed laser beams

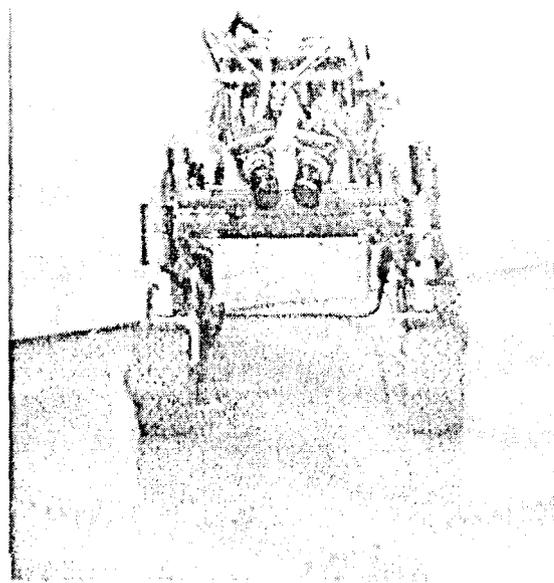


Fig. 2. Front view of the Rocky III rover. This front view of the robot shows how the laser spots are arranged as a "push-broom" ahead of it.

## 1.1. BACKGROUND AND RELATED WORK

The sensor is a derivative of the hazard detection system scheduled to fly aboard the Mars Pathfinder rover. Pathfinder uses a laser stripe-based structured light system. Five lasers project stripes onto the terrain imaged by the rover's cameras. Two images are taken for each hazard scan: one with the lasers turned off and one with them on. The difference between the two images reveals the stripes on the terrain. The lasers and cameras are arranged so that the height of the terrain relative to the rover can be determined using simple geometry once the stripes are detected.

The Pathfinder system is reliable and accurate. It is also fast compared to stereo vision approaches since the computational requirements are significantly lower. There is, however, one important avenue for improvement. Image differencing is time consuming since image acquisition on a 8085-based system is slow. If image differencing could be eliminated from the hazard detection algorithm, its speed would be greatly improved.

The requirement for image differencing on Pathfinder is primarily due to its optical design. There is simply not enough power available to make the stripes bright enough for reliable detection in sunlight without differencing. The new approach also uses laser illumination, but discrete spots are projected rather than a continuous line. At an individual pixel, this can offer several hundred times the brightness.

This article covers design of the system, and consid-

erations for choices made in selection of optical components.

## 1.1.1. APPROACH

The new system has been integrated into two rovers: the Lightweight Survivable Rover (1, S1{-1}) and Rocky III (Figures 1 and 2). Both robots utilize a six-wheeled rocker-bogey suspension like that of the Mars Pathfinder rover. 1, SR-1 is equipped with one of the 8085-based computers developed for Pathfinder; while Rocky III uses a 486-based computer.

The rovers are equipped with two laser/camera pairs for hazard detection. Each laser/camera pair operates as an independent hazard sensor. For now, consider one of the pairs by itself. First, laser light is split into 15 co-planar beams with the central beam aimed at the ground in front of the rover (50cm ahead for 1, S1{-1}). The rest of the beams fan out to the left and right. On flat terrain, the beams form a straight line of spots. If an obstruction is present, they follow its contour instead (Figure 3). The camera is offset horizontally from the laser at the same height above the ground. On-board software finds the spots in the image which are in turn used to determine coordinates of the terrain. From the camera's point of view, each spot shifts left or right depending on the height of the terrain the corresponding beam strikes.

Since the energy is split between 15 discrete beams rather than across a continuous plane (as in Pathfinder), illumination is much brighter at individ-

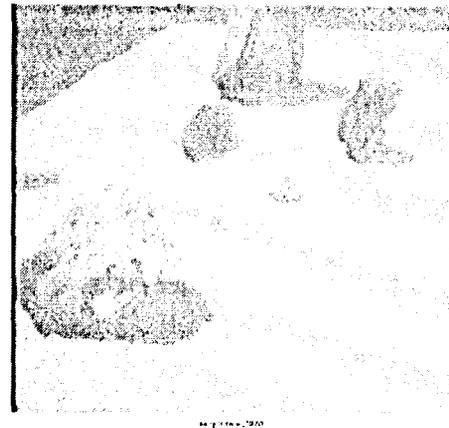
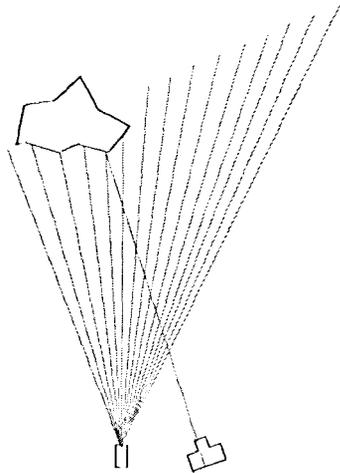


Fig. 3. Laser and camera geometry, left; example image acquired by the sensor, right. The bright spots are laser beams.

ual points (III) the ground. This increased signal-to-noise ratio eliminates the need for image differencing. More details concerning the signal-to-noise ratio are covered in Section I V.

In this system the disparity is computed between where a laser spot should appear if the rover were on flat ground and where it is actually detected. The approach is similar to other structured light systems [1]. Equations for each beam, and a model of the camera's optics are computed ahead of time in a calibration phase. These equations are sufficient for computing the locations of the laser spots on the terrain.

One issue remains: how can the 15 beams be differentiated? Fortunately, the geometry of the system provides a convenient solution. Since the laser and camera are positioned at the same height, each beam will always appear on the same scanline, assuming linear camera optics<sup>1</sup>. If the plane of the beams is tilted slightly, each beam will appear on a separate scanline. The beams may then be found unambiguously, by scanline. Furthermore, the knowledge that each beam will only ever appear on a specific scanline may be used to reduce the image processing necessary to find them.

#### IV. OPTICAL DESIGN CONSIDERATIONS

##### A. Laser versus Solar Brightness

To meet performance goals for hazard detection, the camera system must image laser spots at a nominal range of 0.65m in full sun. A key factor regarding spot detectability is the ratio of spot brightness to reflected sunlight in the image. This design seeks to maximize

<sup>1</sup>In test runs radial distortion in the camera optics has caused the centroid of spots to vary up or down up to 2 scanlines

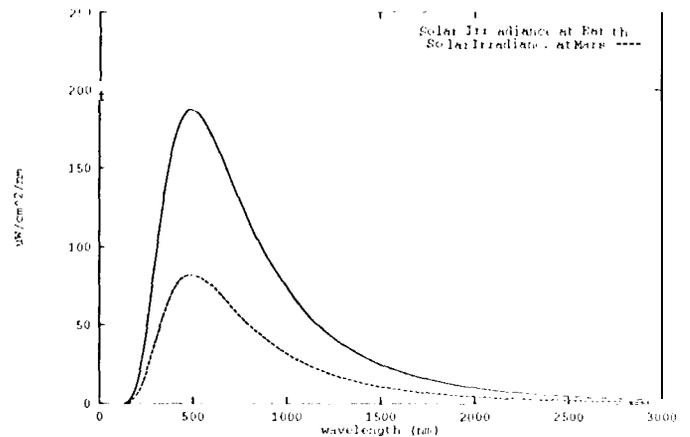


Fig. 4. Comparison of solar irradiance at Earth and Mars, with the Sun modeled as a 5900 degree K black body [3].

the ratio in two ways: first by using a laser whose wavelength (860nm) is in a region where solar power is low (see Figure 4); second, by filtering the reflected light to a narrow band around that wavelength before the scene is imaged. As Figure 4 illustrates, solar irradiance at the distance of Mars from the Sun is 43% of that at Earth. The system was designed for the brighter conditions of Earth for convenient testing, so it will work even better on Mars.

Before introducing the equations governing performance of the system, it is useful to consider the path light follows from the Sun to a pixel in the robot's camera. Upon reaching the Earth or Mars, collimated sunlight passes through the atmosphere, where sev-

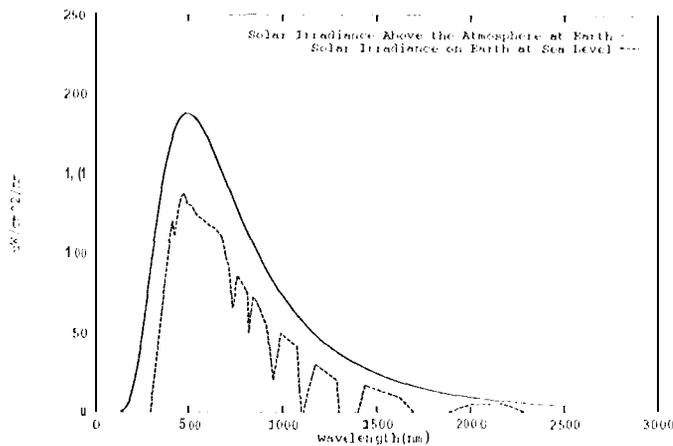


Fig. 5. Solar irradiance on the surface of Earth showing absorption of some frequencies by the atmosphere [3].

(P) frequencies are fully or partially absorbed before striking the terrain (see Figure 5). The terrain absorbs some more of the light, depending on its albedo, and reflects the remainder in all directions across a hemisphere of  $2\pi$  sr, assuming planar surface. The intensity of light that bounces in the direction of the camera depends on the angle at which it struck the surface (incidence) and the angle from which the surface is being viewed (reflectance). Finally, the light is gathered by the lens and focussed on a pixel. The larger the diameter of the lens, the more light it can gather and the brighter the apparent image. Laser light projected by the sensor follows a similar path, but atmospheric attenuation is negligible for such a short trip. For this discussion we consider the overall irradiance at a patch of terrain to be the sum of solar and laser light at that point.

An empirical measure of laser spot to solar brightness in the 800-900nm band was determined on Earth using a UDT 21A power meter and the 800-900nm band pass filters used in the camera's optics. Mid-day sunlight was measured through the filters at  $8.06 \times 10^{-5} \text{ W/cm}^2$ . Laser output was measured at  $3.98 \times 10^{-3} \text{ W}$ . Recall, however, that the laser light is split into 15 beams. A separate test found the splitter transmits 76% of the energy into the primary beams. Assuming uniform beams, each one contains  $2.01 \times 10^{-4} \text{ W}$  after passing through the filter set. If each beam is concentrated within  $0.5 \text{ cm}^2$ , the power is  $4.02 \times 10^{-4} \text{ W/cm}^2$  which results in a ratio of 5 to 1 for laser spot to solar intensity. Since the beam has been focused to less than  $0.5 \text{ cm}^2$  at .65m it is reasonable to expect this ratio is achieved.

### B. Camera Optics

Assuming laser light incident on the terrain is approximately 5 times as bright as sunlight in the pass band, camera design can proceed with the goal of exposing pixels to 20% of their capacity for nominal images of terrain. This exposure will provide the greatest dynamic range in the image and facilitate differentiating the laser spots from other image features.

Our analysis includes the following factors and assumptions:

- **Solar illumination** with a spectrum as depicted in Figure 5.
- **Angle of incidence:** assumed to be normal, to provide the brightest illumination.
- **Angle of reflectance:** assumed to be normal, to provide the brightest image.
- **Lambertian reflectance:** the Sillfil (reflects light uniformly in all directions).
- **Albedo:**  $\rho$ , the surface albedo, is 0.3 at all frequencies. Viking orbiter measurements show Mars surface albedo to vary from 0.10 to 0.36 [2].
- **Optical filters:** to admit a 100nm band of light centered at 850nm. The transmittance of the filter is assumed to be uniform across the pass band.
- **Aperture:** the diameter of the camera lens' opening.
- **Focal length** of the lens.
- **Quantum efficiency** of the CCD imaging device.
- **Size of pixels** in the CCD imaging device.
- **Well depth** of pixels in the CCD imaging device.
- **Exposure time:** 0.1sec. The shortest reliable exposure for the camera hardware is 0.01sec. Using 0.1sec provides room for adjustment later.

We do not consider:

- **Focus**
- **Diffraction effects**
- **Phase angle**

The analysis will proceed from each "end" of the problem. First, the power necessary to expose one image pixel to 20% capacity is considered. Next, filter and lens components to meet that requirement are selected.

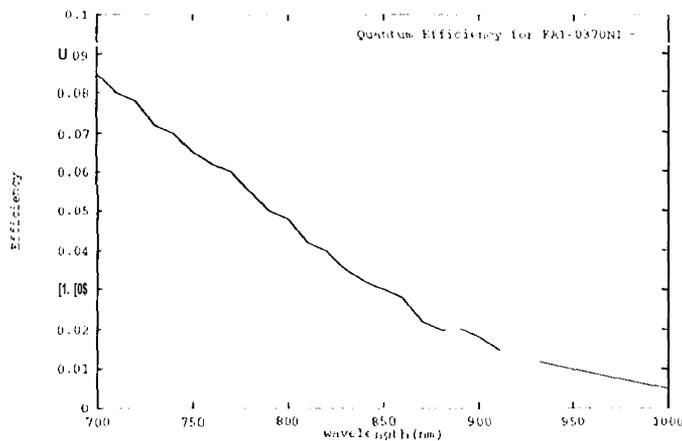


Fig. 6. Quantum efficiency of the KAI-0370N1 CCD.

### C. Pixel Exposure

In this section the energy required to expose one pixel to 20% of its capacity is calculated. The computation is based on manufacturer's specifications for the Kodak KAI-0370N1 CCD, but the approach is appropriate for other imaging devices as well.

A CCD imager is a 2-dimensional array of individually-addressable elements (pixels) whose outputs may be combined to form an image. Important factors in CCD pixel performance are **size**, **well depth**, **quantum efficiency**, and **fill factor**. Size refers to on-center spacing between pixels. Spacing is most often rectangular, but not strictly square. Incident photon energy at a pixel is measured as the charge on a capacitor, with well depth being the fully saturated charge (in electrons). Quantum efficiency is the rate at which the device converts photons to electrons at the capacitor. Figure 6 shows how quantum efficiency varies with wavelength in the region of the spectrum around the laser's wavelength. Finally, fill factor is the percentage of pixel area able to gather light. The KAI-0370N1 specifications incorporate fill factor into the quantum efficiency chart.

The equation governing intensity registered at a pixel is:

$$\text{intensity} = \frac{\Phi_i \times \text{exposure\_time} \times \text{quantum\_efficiency}}{E_p \times \text{well\_depth}}$$

Intensity refers to the level of exposure from 0.0 to 1.0 (fully saturated).  $\Phi_i$  is the power incident on one pixel,  $E_p$  is energy per photon.  $E_p$  is computed for light in the middle of the filter band-pass region (850 nm). Since 20% exposure is desired,

intensity = 0.2. Other parameters are easily computable, dictated by hardware constraints, or are available from the manufacturer's specification sheet. For this system:

Pixel Size 158  $\mu\text{m}^2$   
 Exposure Time 0.1 [1 sec  
 Quantum Efficiency 0.03 (at 850nm)  
 Well Depth 60,000 electrons  
 Photon Energy  $2.34 \times 10^{-19}$  J (at 850nm)

Now, solving Equation 1 for power, and substituting in the known quantities:

$$\begin{aligned} \Phi_i &= \frac{\text{intensity} \times E_p \times \text{well\_depth}}{(\text{fill\_factor}) \times \text{exposure\_time}} \\ &= \frac{0.20 \times 2.34 \times 10^{-19} \text{ J/photon} \times 60,000 \text{ electrons}}{0.03 \text{ electrons/photon} \times 0.1 \text{ sec}} \\ &= 9.35 \times 10^{-7} \mu\text{W} \end{aligned}$$

$9.35 \times 10^{-7} \mu\text{W}$ , is the power of light at 850nm required to expose one pixel 20% in 0.1 seconds.

### D. Lens and Filter Characteristics

This section considers lens and filter components that will deliver  $9.35 \times 10^{-7} \mu\text{W}$  to each pixel for an image of nominal terrain. Since only the light incident on a single pixel is of interest, it is assumed for now that the surface being imaged is a small patch of just the right size that its focused image exactly covers one pixel. The result generalizes across the entire image. The power of light at a pixel is given by:

$$\Phi_i = \omega L \cos \theta_c \Lambda_s T_f$$

where

- $\omega = \pi d^2 / 4r^2$  is the solid angle subtended by the lens, as viewed from the surface patch [sr].  $d$  is the diameter of the lens [m] and  $r$  is the distance from the lens to the surface patch [m].
- $L$  is the radiance of the surface [ $\text{W m}^{-2} \text{sr}^{-1}$ ].
- $\cos \theta_c \Lambda_s$  is the fore-shortened area of the surface patch [ $\text{m}^2$ ], where  $\theta_c$  is the emittance angle between the surface patch and the receiver line of sight.
- $T_f$  is the transmittance of the filter.

For now, the lens parameters are fixed and an appropriate filter transmittance ( $T_f$ ) is computed. To

proceed,  $A_s$ , area of surface patch,  $d$ , the diameter of the lens,  $L$ , radiance of the surface,  $r$ , the range to the surface patch,  $f$ , focal length of the lens, and  $\theta_c$ , and the emittance angle must be found.

The lens has a focal length of 8mm and an f-number of 4. f-number is defined as  $\frac{\text{focal length}}{d}$ , so  $f = 2.0 \times 10^{-3} \text{m}$ . The camera is 0.65m from the surface and it is assumed  $\theta_c = 0$ . With these parameters,  $\omega$  is computed as:

$$\begin{aligned} \omega &= \pi d^2 / 4r^2 \\ &= \pi (2.0 \times 10^{-3} \text{m})^2 / 4(0.65 \text{m})^2 \\ &= 4.83 \times 10^{-6} \text{sr} \end{aligned}$$

Next,  $A_s$  is calculated. The area of the surface patch depends on the area  $A_i$  of an image pixel, the focal length,  $f$ , of the lens, the range,  $r$ , and the viewing angle  $\theta_c$  as

$$\begin{aligned} A_s &= \frac{A_i r^2}{f^2 \cos \theta_c} \\ &= \frac{158 \mu\text{m}^2 (0.65 \text{m})^2}{(8 \text{mm})^2 \cos 0} \\ &= 0.0104 \text{cm}^2 \end{aligned}$$

Finally,  $L$ , radiance of the surface, is given by:

$$L = \frac{\rho E}{\pi}$$

Where  $E$  is the surface irradiance  $\text{W}/\text{m}^2$ , and  $\rho = 0.3$ , is the surface albedo.  $E$  can be approximated by inspecting Figure 5. Irradiance near the center of the 800-900nm band is  $70 \mu\text{W}/\text{cm}^2 \text{nm}$ , or  $7000 \mu\text{W}/\text{cm}^2$  across the whole band. So  $L = 668 \mu\text{W}/\text{cm}^2 \text{sr}$ . Therefore, the power at a pixel (no filter) is:

$$\begin{aligned} \Phi_i &= \omega L \cos \theta_c A_{\text{surface}} \\ &= 4.83 \times 10^{-6} \text{sr} 668 \mu\text{W}/\text{cm}^2 \cos(0) 0.0104 \text{cm}^2 \\ &= 3.36 \times 10^{-5} \mu\text{W} \end{aligned}$$

Based on this, and the requirement for  $9.35 \times 10^{-7} \mu\text{W}$  at the pixel, the desired transmittance for the filter is  $T_f = \frac{9.35 \times 10^{-7} \mu\text{W}}{3.36 \times 10^{-5} \mu\text{W}} = 0.028$

Reviewing the calculations up to this point: a filter system that transmits 2.8% of the light uniformly between 800 and 900nm, and 0% elsewhere will expose one pixel 20% in 0.1sec and will provide a 5 to 1 ratio of laser to solar brightness in the image. The 100nm pass-band filter is created by combining two colored

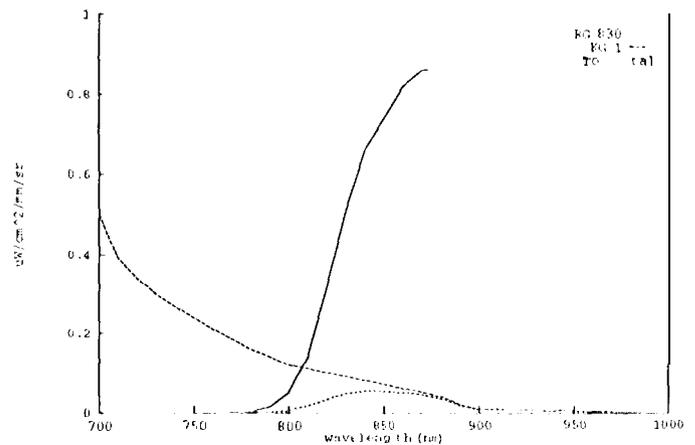


Fig. 7. Two filters are used in combination to restrict light to an 800 to 900nm band. About 4% of the light in that band is transmitted.

glass filters: one cuts light below 800nm (RG-830), and another cuts light above 900nm (KG-1). The combination of the two results in 4% transmission between 800 and 900nm (Figure 7). The difference between the desired 2.8% and 4% is made up by adjusting exposure time of the CCD appropriately.

## V. RESULTS

The primary goals of this work are to provide fast, reliable and accurate information about the terrain for rover navigation. Each of these will be examined in turn.

The overall time required for a hazard scan depends primarily on time required to expose and collect images of the projected laser spots. Since the system uses simple logic for spot detection, image processing is negligible. On the 486-equipped rover (Rocky III) exposure time is 100ms per camera, acquisition takes 600ms, and an additional 30ms are required to turn the lasers on and off, find the spots and compute hazard heights. As a result, Rocky III can complete a hazard scan in 830ms. This is over 20 times the rate for Mars Pathfinder hazard scans. We estimate the 8085-based LSR system will require 4 seconds per scan. This is about 5 times as fast as Mars Pathfinder using the same computer and camera technologies.

As a rule of thumb, rocker-bogie type rovers travel safely at  $\frac{1}{4}$  of a wheel diameter per hazard scan. The new sensor provides  $\frac{1}{4}$  of a wheel diameter per hazard scan. The new sensor provides  $\frac{1}{4}$  of a wheel diameter per hazard scan. The new sensor provides  $\frac{1}{4}$  of a wheel diameter per hazard scan. The new sensor provides  $\frac{1}{4}$  of a wheel diameter per hazard scan. This is 5 to 20 times as fast as could be maintained using the older sensor aboard Mars Pathfinder. Rocky III can travel safely

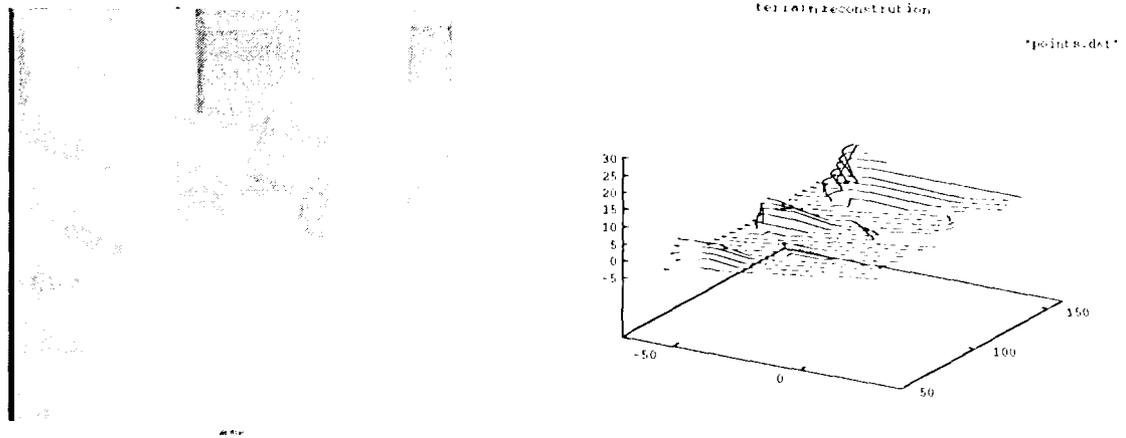


Fig. 8. Sample terrain (left), and a reconstruction based on sensor data (right).

at 3.6cm/sec.

The speed of the system arises from the fact that a simple peak-detection logic is used to find the laser spots. The reliability of this approach was evaluated by measuring the rate of spot detection in a series of 24 test images acquired over an area of simulated Mars terrain in full sun (Figure 8). In the 24 images, 339 spots were visible. Of these, 335, or 99% were detected. In two cases, or about 0.5% of the time, a bright patch of ground was mistaken for a laser spot.

The sensor's accuracy in reporting the coordinates of obstacles was evaluated using the same test images. The reported height for each rock was found to be within 1cm of the true height. Accuracy in lateral and fore-aft dimensions was evaluated qualitatively by inspecting a reconstruction of the scene generated using the sensor data (Figure 8). Every hazard was detected.

The new system returns 50% more information about the terrain in each hazard scan than the older design (30 data points versus 20). When accurate odometry is available, the uniform arrangement of data points provides for 3cm grid terrain maps, similar to the one illustrated in Figure 8. These maps are likely to be exploited in future work aimed at more efficient navigation. Conversely, the Mars Pathfinder sensor's 20 points are arranged in a non-uniform 4x5 grid that is not as appropriate for building terrain maps.

## VI. CONCLUSION

We have presented the design and implementation of a hazard sensor that provides for safe travel at 5 to 20 times that of earlier technologies. Additionally, the sensor offers:

- **Reliability:** 99% of detectable spots are found using simple peak-detection logic.
- **Accuracy:** The system has demonstrated better than 1cm accuracy in detecting obstacle height.
- **Flight-qualified components:** The system is primarily built of already qualified components. The only *in-flight* modification is a diffraction grating for splitting laser light.
- **Low mass:** The sensor weighs approximately 200 grams, excluding cabling.
- **Low power:** Consumption peak is 1.1 Watt. The same sensor power budget as Mars Pathfinder provides hazard scans at 5 to 20 times the frequency, offering equivalent increases in safe traversal speed.
- **No moving parts.**

## VII. ACKNOWLEDGEMENT

Todd Litwin developed the camera 1D and 3D-dimensional line intersection software used in this system; he also provided several helpful suggestions. Hrand Aghazarian provided technical assistance on Rocky 111 and 112.

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Obviously, the requirement shown in Figure 1 is derived from experience with some typical measurements shown here. The increase in peak acceleration with increasing frequency is a measured fact, and occurs because of the low effective mass generally associated with higher frequency structural resonances.

### 2.1.1 Failure Modes

The failure, modes produced by shock excitation can be broadly grouped into four categories. First are those failures associated with high stresses, such as buckling of long and slender structures, plastic deformation of structures or fracture in brittle components. Next are failures due to high acceleration levels, which can cause relays to chatter, potentiometers to slip and bolts to loosen. Third are problems associated with excessive displacement, which include broken solder joints, cracked PC boards and wave guides, or general problems associated with the impact of one structural component into another. The final category consists of transient electrical malfunctions, which occur only during application of the shock environment. Such malfunctions occur in capacitors, crystal oscillators and hybrids, the latter of which can temporarily short circuit during a shock event due to contact between the device package and internal die bond wires.

### 2.1.2 Supporting Data

Many studies regarding the effects of pyrotechnic shock have been conducted during the life span of the aerospace industry, but one of the best is perhaps that provided in Reference 1. Conducted by the Aerospace Corporation under contract to the Air Force Systems Command Space Division, the study examined and summarized ordnance-related shock failures over a period spanning some 20 years, dating from the first missile-related pyro shock failures in the early 1960s to about 1982 when the study was concluded. A total of 85 flight failure events are summarized in the paper, reflecting events ranging from relay chatter, broken electrical wires and leads, cracked glass diodes or fracture of brittle ceramic components and a number of others.

## 3.0 Tradeoffs

Failure mode sensitivities and cost tradeoffs for the pyrotechnic shock environment need to be discussed in the context of a particular test technique. The three principal methods for shock testing include shaker synthesis, resonant plate testing and actual firing of pyro devices.

In the shaker synthesis technique, the article to be shock tested is mounted to an electrodynamic vibration shaker using an appropriate fixture. A function generator is connected to the shaker, and a triangular, square wave, half-sine or similar time-based pulse is input to the test article in an attempt to generate the desired frequency response spectrum,

Generally, this is a trouble-prone and ineffective exercise because, as stated above, a pyro shock pulse rarely manifests itself as a simple function. Furthermore, the shaker synthesis technique tends to input excessive energy to the structure at low frequencies and insufficient energy at high frequencies. As a result, hardware subjected to such tests is often overtested in the low frequency regime and undertested elsewhere.

In an attempt to improve upon the synthesis method, many environmental test engineers have attempted to modify the input to the shaker using so-called "chirp" techniques. In this case, output from the function generator is passed through a graphic equalizer before being routed to the shaker. The shaker input spectrum is then "tuned" through an increase in the gain of high frequency signals, and through an attendant gain reduction at low frequencies. Unfortunately, such efforts offer marginal improvements at best, due to the inherent low-pass filter characteristics of a mechanical shaker.

In the resonant plate technique, advantage is taken of the fact that a stiff, free-free metal plate can exhibit very high frequency resonances. The article to be tested is mounted to an aluminum or steel plate, and the plate is subsequently suspended in mid-air. A metal pendulum is then swung into contact with the plate, inducing transient vibration. If the frequency response of the mounted test article is measured with an accelerometer, a plot such as that illustrated in Figure 4 can result,

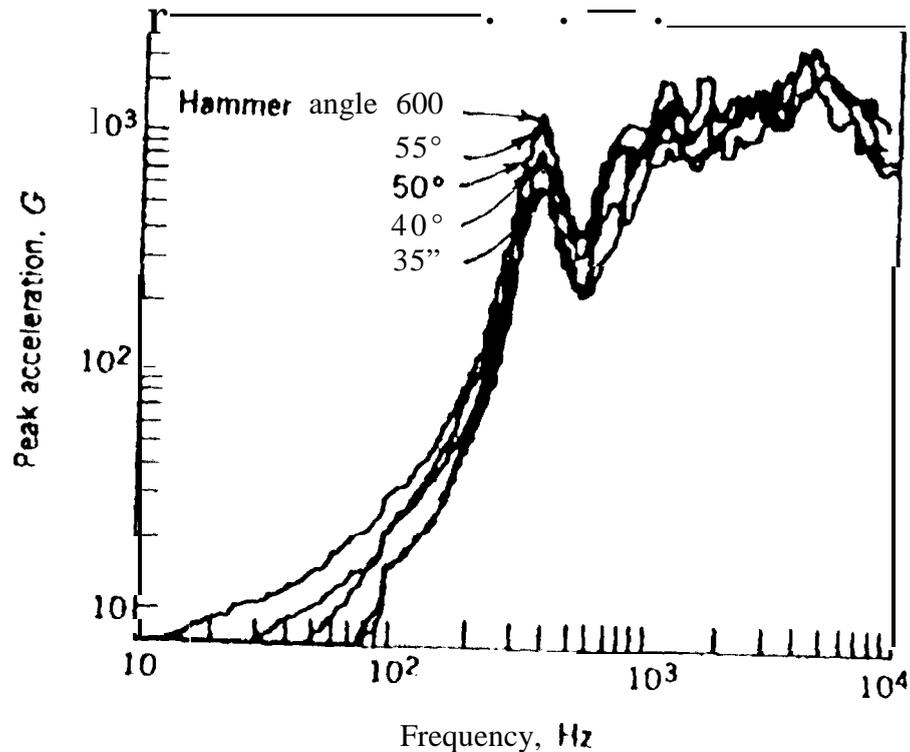


Figure 4 - Response Spectrum in Resonant Plate Test

Although this technique can clearly produce a response, exhibiting the desired trend of increasing acceleration with increasing frequency, it is still less than ideal. Tuning of the response spectrum such that the correct accelerations occur at the desired frequencies is very difficult, involving modification of the plate thickness, shape or suspension method, modification of similar hammer characteristics, or modification of the hammer swing angle as illustrated in Figure 4. These activities are time consuming and generally based on trial and error, and may never produce the correct response spectrum.

The best pyrotechnic shock test method, then, is one which utilizes pyrotechnic devices. Due to safety, facility and related requirements, this can be an expensive proposition. However, considering the time which might otherwise be wasted during the construct of a simulation, and considering the potential for over-design or underdesign of hardware which could occur if the simulation is inaccurate, the pyro method may in fact be a bargain. It should be utilized if at all possible.

Armed with our vast knowledge of the primary shock testing methods, we can now present appropriate test control parameters, the sensitivity of failure, modes to changes in these parameters, and cost tradeoffs associated with each, Figure 5 provides a summary matrix of this information.

| Control Parameters | Failure Modes          | Sensitivity to Increase |     |      |   | Cost                          |   |
|--------------------|------------------------|-------------------------|-----|------|---|-------------------------------|---|
|                    |                        | g                       | dur | rise | f |                               |   |
| g peak             | intermittents          | +                       | -   | -    | 0 | g increase = bigger shaker    | + |
| t duration         | broken solder joints   | +                       | +   | +    | - | t duration change             | 0 |
| t rise             | opens                  | +                       | -   | -    | + | t rise redct = better fcl gen | + |
| f frequency        | shorts                 | +                       | -   | -    | + | f increase = chirp test eqpt  | + |
|                    | broken connectors      | +                       | -   | +    | - | <b>Resonant Plate Method</b>  |   |
|                    | broken wave guides     | +                       | -   | -    | - | g incr = plate/pendim change  | + |
|                    | broken crystals        | +                       | -   | -    | + | t duration change             | 0 |
|                    | cracked diodes         | +                       | -   | -    | + | t rise reduction              | 0 |
|                    | relay chatter          | +                       | -   | -    | + | f incr = plate/pendim change  | + |
|                    | fastener loosening     | +                       | -   | -    | + | <b>Pyro Device Method</b>     |   |
|                    | potentiometer slippage | +                       | -   | -    | + | g incr = charge change        | + |
|                    |                        |                         |     |      |   | t duration change             | 0 |
|                    |                        |                         |     |      |   | t rise reduction              | 0 |
|                    |                        |                         |     |      |   | f increase                    | 0 |

Figure 5 - Control Parameter Sensitivity and Cost Sensitivity

4.0 References

1. Mocning, C. J., "Pyrotechnic Shock Flight Failures," The Aerospace Corporation, 1984,

S.0 Bibliography

1. Steinberg, D. S., Vibration Analysis for Electronic Equipment, New York: John Wiley & Sons, 1986.
2. Markstein, Howard W., "Designing Electronics for High Vibration and Shock," Electronic Packaging & Production, April 1987, pp. 40-43.

### 3. Radiation Design Margin Requirement

#### 1.0 Objectives

One of the design drivers of spacecraft is the requirement to survive in the radiation environment expected to be encountered throughout the mission. Flight assemblies shall be designed to withstand ionization effects and displacement damage resulting from the flight radiation environment with the required radiation design margin (RDM).

The definition of RDM is the ratio of radiation capability of the part or component for a given application to the expected radiation environment at their respective location during the mission. The part/component radiation capability is defined to be the fluence (or dose), flux (or dose rate) of charged particles or nuclear radiation which will produce enough change (degradation or radiation-induced interference) in the part characteristics to cause the part to operate outside of its specification for the particular circuit application.

The RDM requirement is imposed on assemblies or subsystems to assure reliable operation and to minimize risk, especially in mission critical applications. The general use of an RDM acknowledges the uncertainties in environmental calculations and part radiation hardness determinations.

#### 2.0 Typical Requirements

Based on flight experiences, it is standard practice, at JPL, to require an RDM of 2 for most applications if only the inadvertent shielding of the surrounding spacecraft or instrument enclosure materials are considered in the radiation/shielding analysis. However it requires an RDM of 3 when local shielding, such as component/part package or spot shielding, is taken into account.

The RDM requirement does not apply to single event effects (SEE), such as single event upset (SEU), single event latchup (SEL), etc., since SEE is evaluated on a probabilistic basis.

##### 2.1 Rationale

The uncertainties in radiation environment estimates and the part or component radiation capability determinations lead to RDM values between 3.5 to 11.5 (Ref.1). Historically, the introduction of an RDM of 2 stems from the Voyager Project and was established based solely on not having sufficient mass allowance for shielding. An RDM much greater than 2, perhaps as high as 10, would have been selected to cover all uncertainties if there had been sufficient mass available (Ref. 1).

An RDM of 3 is imposed when local shielding, such as component/part package or spot shielding, is taken into account. There is an implied greater risk associated with taking the local shielding into consideration because this is done in cases where soft parts, rather than inherently hard parts, must be used that are dependent on local shielding and their calculated shielding effectiveness.

##### 2.1.1 Failure Modes

###### (1) Long-Term Ionization Effects

Potential problems with the electronics and material arise from the long-term effects of ionizing radiation. The magnitude of long-term ionization is a function primarily of ionizing energy deposition, i.e. the dose measured in rads in the material in question.

in semiconductor devices, these are manifested in charges being trapped in insulating layers on the surface of the semiconductor devices. They are most important in MOS structures in which trapped charges in the gate oxide layer produce a change in the apparent gate voltage. Trapped charges in surface passivation layers are also important in junction devices where they may produce an inversion layer that spreads out over the effective surface area, thereby increasing the recombination-generation currents. These currents are most important in bipolar transistors that are operated at low collector currents and in n-channel JFET devices. The susceptibility to surface recombination depends on the quality of the oxide layer and the applied electric field,

in optical materials, long-term ionization effects appear primarily as an increase in optical absorption. These are usually manifestation of charges trapping at a pre-existing defect, so the absorption rate is a strong function of the initial material properties. For example, fused quartz generally colors less than alkali glasses for a given ionizing dose.

in quartz crystal used for precision oscillators or filters, long-term ionization effects can produce significant resonant-frequency shifts. Again there is a strong dependence upon the type of material used. Natural quartz shows the largest frequency shift for a given ionizing dose, synthetic quartz shows less, anti swept synthetic quartz shows even less. In these cases proper selection of the quartz crystal growth method can minimize the effect.

The devices and materials of concern and the most serious radiation induced effects are:

- (1) MOS devices (threshold voltage shift, enhanced leakage).
- (2) Bipolar transistors ( $h_{FE}$  degradation, especially at low  $I_C$  ; leakage current), and junction field effects transistors (JFETs) (enhanced source-drain leakage current).
- (3) Analog microcircuits (offset voltage, offset current and bias-current changes, gain degradation).
- (4) Digital microcircuits (enhanced transistor leakage, or logic failure due to ionizing dose induced  $h_{FE}$  &  $V_T$  changes).
- (5) Quartz, resonant crystals (frequency shifts).
- (6) Optical materials (increased absorption).
- (7) External polymeric surfaces (mechanical degradation).

## (2) Transient Ionization Effects (Interference)

Interference is defined as transient ionization effects that persist only while the electronics are being irradiated, and whose severity is generally proportional to the dose rate. Interference effects depend primarily on the rate of ionization energy deposition, i.e., the dose rate measured in rad/s.

There are four types of interference in electronics devices and optical materials:

- (1) Primary photocurrents in low current sensitive input stages to the electronics,
- (2) Electron emission from cathodes of electron multiplier-type detectors.
- (3) Ionization-induced conductivity in photo-sensitive materials, such as those in detector surfaces.

(4) Ionization-induced fluorescence in optical materials, such as detector windows and lenses (fluorescence efficiencies vary strongly with the types of material).

### (3) Displacement Effects

Displacement of atoms in crystal lattices cause permanent changes to material properties. The expected proton and electron fluences usually do not represent as severe an environment for displacement effects as for long-term ionization effects. Therefore, only the most sensitive devices will be affected significantly by displacement effects.

Displacement effects can affect the following devices and properties in the electronics:

- (1) Bipolar transistors with low  $f_1(h_{FE}, V_{CE\ SAT}, V_{BE\ SAT})$ .
- (2) PN junction diodes ( $V_F, V_R$ ).
- (3) Light emitting diodes (LED) ( $V_F, V_R$ , light emitting efficiency).
- (4) semiconductor photodetectors (quantum efficiency).
- (5) Devices incorporating lateral p-n-p transistors ( $h_{FE}, V_{CE\ SAT}, V_{BE\ SAT}$ ).
- (6) MOSFETs (resistance, leakage current).

### 2+1.2 Supporting Data

The JPL PFR database was searched for types of failures and failure modes recorded during the radiation tests and in flight. An abstract of some of the PFR data related to radiation effects are shown in Table 1.

| S/C     | PFR # | Environment | Description  | Failure Mode   |
|---------|-------|-------------|--|--|
| Voyager | 41048 | Flight      | Nrr counts in rate channels of HET 2 telescope                                       | Probably one of the 3 hi-polar transistors in the circuit failed due to radiation  |
| Galileo | 52602 | Flight      | Observed noise spikes characteristic of radiation induced events in SS1              | A likely correlation with high solar activity level  |
| Galileo | 41341 | Test        | The ultra stable oscillator (USO) shifted frequency -1.676 Hz due to a 5 Krads dose. | (1) negative frequency shift is to be expected when swept synthetic quartz is irradiated<br><br>(2) the offset voltage changes in the LM108HR of the inner oven control circuit resulting from radiation |
| Galileo | 44287 | Test        | Some of CDS's memory RAMs got worse with radiation                                   | Significant degradation of the read disturb threshold  |

### 3.0 Tradeoffs

Often an RDM of 2 is perceived by many people as being overly conservative. The selection of an RDM may be somewhat arbitrary and will tend to be driven by mass limitations, acceptable risk versus cost, and the total radiation hardness program.

Projects typically have resources and mass limitations which preclude usage of more conservative RDMs. Based on the "best" radiation model at the time, the part radiation hardness test data, and the expected mass and other resource limitations, a radiation design factor of 2 (3 if local shield is

considered) is required for spacecraft flight elements. The term used to describe this radiation design factor is "radiation design margin", and this is the source of most common misunderstanding. The problem arises from the fact that there are significant uncertainties in all the elements in the radiation susceptibility calculations, and the term "radiation design margin" implies a known factor of safety, which in turn implies a large degree of certainty of survival in the radiation environment. For this reason RDM which implies a margin is really a misnomer. It may be more appropriate to refer to a radiation design factor and not inadvertently mislead people to believe a conservative margin exists. An RDM of 2 is not, nor was it ever, intended to imply 100% margin as it has sometimes been misconstrued to mean. An RDM of 2 does not cover the uncertainties as indicated in Reference 1. However, in the world of practicality an RDM of 2 was all that was affordable on Voyager, and it worked on the one spacecraft that was tested. It is important to reiterate that there are uncertainties in environmental calculations and part radiation hardness determinations in the use of RDM.

### (1) Radiation Hardness Determination

There are at least four quantities that can contribute to the uncertainty in the part radiation capability: the part type, the manufacturing process, the circuit design, and the particular circuit application. There are many different part types, many circuit designs and applications and perhaps several different manufacturing processes. Consequently, the uncertainty in the part capability has to be sufficiently large to account for the large variations from part to part. Most of these are difficult to quantify and testing is the only method of determining the radiation capability to be expected in a given flight lot. Even though the uncertainty for any one specific part may be quite small, different radiation test conditions can generate different capability values. For some linear integrated circuit devices, the total ionizing dose (TID) capability could drop dramatically if tested with low dose rate instead of high dose rate. For example, OP42 was rated a radiation-hard device (> 100 Krads) in the past but was recently found to be very soft (~ 15 Krads or lower) when tested with low dose rate which better simulated the flight environment.

As electronics parts now have higher capacity and smaller volume compared to those used on Voyager and other spacecraft, it is prudent to carefully re-examine RDMs of higher magnitude on future spacecraft programs or to refine the part radiation hardness determination technique if an RDM of 2 or lower is demanded. The part radiation hardness test is generally a cost driver. This is primarily due to the fact that a more accurate test requires more samples, more realistic flight simulating radiation sources and conditions, and longer test time.

The alternative to overcoming the test uncertainties is to perform the worst case analysis (WCA) for the circuit applications. For example, if a bipolar transistor was rated 50 Krads in terms of  $h_{FE}$  degradation, but the parameters shift due to an irradiation of 100 Krads is still acceptable based on the worst case analysis, this part has the required RDM of 2 if the local environment is 50 Krads.

### (2) Radiation Environment Calculation

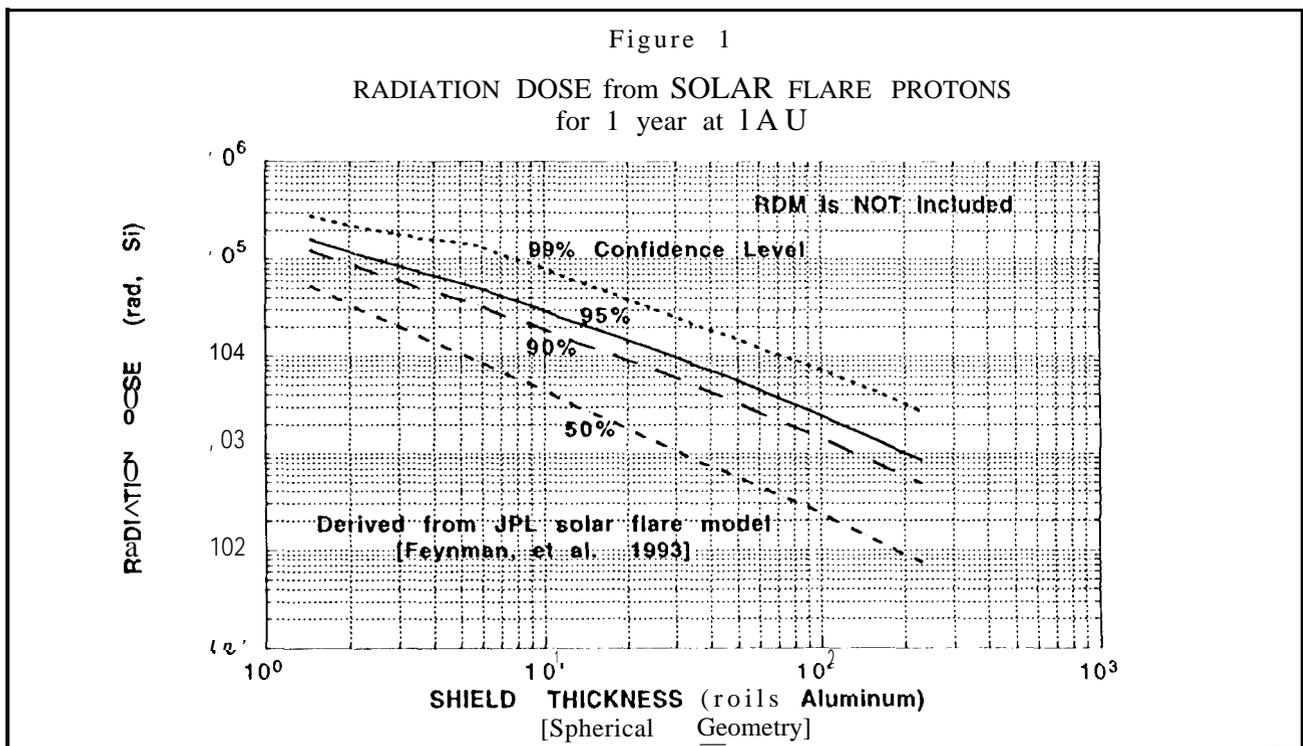
The local ambient radiation environment is dependent on the mission design, the environmental radiation models, the radiation transport code, and the spacecraft mass model. The calculated radiation environment might be the total ionizing dose (TID), 20 MeV equivalent proton fluence for displacement damage, or flux for detector interference effects.

The uncertainty in the radiation model depends on the environment in question and the mission design. Uncertainties in the mission design are difficult to quantify. The parameters involved here include the trajectory (heliocentric distance, mission length, altitude, inclination, etc.) and launch date. The uncertainty in the radiation environment depends on the environment in question. As an example, prediction of proton fluences from solar flares is treated probabilistically and the discrepancy between predictions for the 10 MeV fluence between two different solar flare models

is a factor of 2 (at the 95% confidence level) (Ref. 1). Similarly, the uncertainties in the Jovian trapped electron environment and the Earth's trapped radiation proton model AP8 arc also estimated to bc a factor of 2. The uncertainties resulting from the use of different radiation transport codes and different spacecraft mass models arc generally less than a factor of 2 (Ref. 1).

Typicall y, once the mission design is confirmed, the TID as a function of shielding thickness (dose-depth data) arc generated for a simplified geometric mass model, such as the spherical shell model. Figure 1 is an example of a flight mission at 1 AU from the sun during the solar max period. It is standard practice to apply the dose,-depth curve at 95% confidence level for the flight assembly (unit) design. This radiation dose curve can be used to obtain conservative "first-look" shielded dose values without hardware configuration modeling. These dose plots should only be used to obtain dose value by using the minimum shield thickness applicable to a given hardware location. Since these plots do not represent flight hardware configurations, they should be used for design assessment only if they arc applied in a conservative manner (minimum shield thickness used). If the concerned part does not meet the RDM of 2 requirement based on this conservative TID level, a three dimensional mass model simulating the flight assembly (unit) is then constructed for the radiation transport code. The resulting TID level will be lower than the TID data from the spherical shell model and therefore the concerned part is more likely to meet the RDM requirement. However, when the part/component package has to be included in the 3D mass model or a spot shield has to be added, the RDM is increased from 2 to 3 as explained earlier. The more extensive radiation/shielding calculations tend to be a cost driver, but it relieves the shielding requirement and therefore saves more mass.

Radiation/shielding analysis is relatively cheap compared to spot shielding design/in~plcnclntation or part radiation hardness tests. It takes several days to analyze TID with a simplified mass model, such as a box, or several weeks to generate more accurate TID results with a more realistic mass model) to simulate the flight assembly (unit). The resulting lower TID level reduces the unnecessary shielding mass-and relieves-the part hardness test rigidity



Failure mode sensitivities and cost tradeoffs for the radiation design margin (RDM) requirement are illustrated in Table 2.

| Table 2. Control Parameter Sensitivity and Cost Sensitivity |                                 |                              |                                  |   |  |   |
|---|---------------------------------|------------------------------|----------------------------------|---|--|---|
| Requirement   | Control Parameter               | Failure Modes                | Sensitivity to Increase Failures |   | cost                                       |   |
|   |                                 |                              | P                                | D |  |   |
| Radiation Design Margin<br>( $RDM = P/D$ )                  | Radiation Capability (P)        | Long-Term Ionization Effects | -                                | + | Refining Radiation Capability Test         | + |
|   | Local Radiation Environment (D) | Transient Ionization Effects | -                                | + | Refining Radiation Environment Calculation | + |
|   |                                 | Displacement Effects         | -                                | + |  |   |

#### 4.0 References

1. JPL IOM 5217-88-39, "Radiation Design Margins", S. B. Gabriel to Distribution, September 22, 1988.

## 4. Minimum Operating Time Requirement

### 1.0 Objectives

The objectives of operating assemblies or subsystems for a minimum period of time or number of cycles are to verify their operation in accordance with the design requirements and to ensure that the manufacturing workmanship or integration processes have not compromised their reliability. It also verifies the appropriateness of the design for the mission, based on the anticipated failure modes.

### 2.0 Typical Requirements

operational hours (for electronics) or the number of mechanical cycles (for periodic or continuous cycling mechanical units) should be sufficient to demonstrate operation despite of design, workmanship or integration problems.

Minimum operating time requirements, as specified in JPL-D-8966, for different spacecraft classes are:

- 1,000 hours for Class A spacecraft
- 500 hours for Class B spacecraft
- 200 hours for Classes C and D spacecraft
- Mechanical cycling is 1.5 times the mission-required cycles

industry requirements for electronic burn-in vary from 100 to 2,000 hours. In most cases, the available specifications for operational hour/cycle requirements do not provide the rationale or methodology for their determination.

### 2.1 Rationale

The operational duration and power cycling of electronics, or the number of cycles of mechanical cycling devices serve to uncover electrical/mechanical infant mortality or latent defects, thus assuring spacecraft reliability. They also provide information on integrity, as well as operational or reliability expectancy of the equipment being tested. During the testing, some or all of the expected stresses are applied to the equipment. Depending on the failure modes expected for the applied stresses and their duration, failures of weak components or assemblies will appear on a certain time scale. As indicated in Reference 1, time dependent failure mechanisms can be important for a significant number of hardware elements.

#### 2.1.1 Failure Modes

Examples of time-dependent deficiencies and defects are summarized below:

##### 1. Design deficiencies, such as:

- a. Electrical or mechanical component, or mechanical assembly wearout caused by excessive stresses, poor tolerancing, or workmanship.
- b. Electrical or mechanical over-stress of components causing hard failures.
- c. Thermal design deficiency causing component parametric drift and an increase in inherent failure rate.
- d. Loss or inadequate lubrication of mechanical cycling devices.

##### 2. Workmanship defects, such as:

- a. Poor solder joints (also temperature/cycle dependence).
- b. Damaged component hermetic encapsulation.
- c. Inadequate welding of pyre-activated devices (such as bellows) causing leaks and failure to actuate.

3. Software problems, such as:

- a. Errors that can only be identified when the codes in question are executed. This may take a long period of time.

The JPL Problem Failure Reporting, PFR, database was searched for failure modes found in tests and the test operational time and/or operational cycle duration. Examples of some of the failure modes are tabulated below:

| <b>Examples of Failure Modes</b>   |   |  |
|--|---|--|
| <b>Design (electrical)</b>   | <b>Design (mechanical)</b>  | <b>Workmanship</b>   |
| Functional anomalies<br>Out of spec operation<br>Detectable over-stress<br>Electronic instabilities<br>Parameter variation<br>Sneak circuits<br>Shorting to ground<br>open circuits<br>Inadequate interfaces<br>Cracked PCB traces | Poor solder joints<br>Overheating<br>Material interference (dissimilar materials) | Poor solder joints<br>Low or high torque on fasteners<br>Cracks in component encapsulation |

Each failure mode typically has a different time dependency that requires individual consideration. For some failure modes, operational duration/cycle requirements may be statistically estimated from a knowledge of the detailed mechanisms of specific failure modes. For other time- or cycle-sensitive failure modes, they may be determined through factorial design or estimated from a database search. For many of the failure modes, the minimum operating time based on this factorial design has been determined and they can be found in the literature.

**2.1.2 Supporting Data and Recommendations**

The JPL PFR database was searched to determine the types of failures and failure modes recorded during operational time or cycling duration tests. An abstract of some of the PFR data is shown in Table 1.

The JPL flight anomalies database was examined to establish their time or cycle dependence. For the latter, some orbiter S/C data from GSFC were also reviewed, together with the JPL interplanetary S/C database. The reason for including both orbiters and interplanetary S/C is that the New Millennium is a series of S/C which will be designed and manufactured more like commercial orbiters than traditional JPL interplanetary S/C. Data from some orbiters show flight failures that are directly related to the operating time or operational cycle duration, possibly indicating an inadequacy of testing.

Table 1, Ground Test Anomalies Related to Operational Time and/or Cycling for Interplanetary and orbiter S/C.

| S/C                    | PFR #  | Description  | Nature of Test            | Comment  |
|------------------------|--------|--|---------------------------|--|
| Viking                 | 30716  | Power events meter for TMU-a failed cycling  | Power Cycling             | Power monitor drawer problem                                       |
| Voyager                | 36144  | Scope display not calibrated at screen top   | operating Time            | Found defective oscilloscope                                       |
| Voyager                | 37221  | Chain A #03 signals incorrect frequency width  | S/W Error                 | Shown when this code executed                                      |
| Voyager                | 40330  | Erratic limit cycling in pm burn mode  | S/W Error                 | Shown when this Code executed                                      |
| Voyager                | 40724  | Shunt radiator simulator relay cycling   | Cycling                   |  |
| Voyager                | 105581 | Prop valve leaked after hot cycling  | Cycling                   |  |
| Acoustic               | 40529  | L&R sample handle.r retraction time increased  | Operating time or cycling | Wearout, mechanical  |
| ATMOS                  | 31744  | No flight vib. isolator helicoil lock capability   | Operating time            | Wearout, fasteners   |
| ATMOS                  | 51054  | IR detector could not be cooled down to its normal temp.   | Operating time            |  |
| Illn'sex;              | Z10249 | Valve switch drive circuit failure   | Power Switching Or)/off   |  |
| Cassini                | 59729  | S/W error in hot and cold temperature  | Execution time            | S/W' errors should not be dependent on temperature                 |
| Galileo                | 54308  | Let air conditioning failed/CI)S-SII overheated  | Operating time            |  |
| Galileo                | 54570  | PPE failed to achieve 1.5 ppm dewpoint spec.   | Operating time            | New filters installed  |
| Galileo                | 41308  | S-band command switch sticks in S/C HI position  | Operating Time            | S w i t c h wearout  |
| Microwave Limb Sounder | 58099  | The antenna is not forward stepping,   | Operating Time/Cycling    | Wearout; Flight Failure. Motor bearings                            |
| NASA Scatterometer     | Z10100 | Configuration: dss b, TWTA #2 selected; receive-only mode  | Power cycling             |  |
| Pioneer                | 100723 | Preamp output low on turn-on, increases as a function of the operating time. Contamination found       | Operating time            | Would not be found without test.                                   |
| SIR-C                  | 56172  | Cassette tape loading problem led to power supply failure. Cycling power on/off caused the 1'S failure | Power cycling             |  |
| Tiros                  | 1316   | Gunn oscillator SW regulator PWR Supply failed   | Operating time            | 15V shorted to the ground  |
| WFPC                   | 49460  | A latch plate damaged by collar on the shaft   | Operating time            | Reworked; Galled surface machined, base cleaned, surface re-lubed. |

No definitive conclusions could be made about the appropriate test or cycling duration from the present JPL PFR Database, as the test time for the failures is not routinely recorded. With cooperation from projects, efforts are underway to ensure this information is always entered in the database.

The operational time into flight can be obtained from the flight data. But, these data do not assure knowledge of how long a particular assembly (unit) has been powered on or the number of cycles accumulated on a particular switch since they do not include ground test information. However, this information can be obtained from ground testing records or from test personnel, Table II shows examples of flight anomalies related to the operating time or cycling of orbiters and an interplanetary S/C (Voyager).

Table 11. Examples of Flight Anomalies Related to the operating Time or Cycling of Orbiters and an Interplanetary S/C (Voyager).

| PRF No. | S/C     | Sub-system             | Assem. Part       | Symptom  | Cause  | Action  | Recommendation   | Refs. |
|---------|---------|------------------------|-------------------|--|--|---|--|-------|
| A01282  | COBE    | Structural             | Solar Array N-BOP | Wing-B outer panel telemetry displays > 95% deployment. Should show lock position as nominal. (switch did become functional after a period of about 6 months.)<br>Comment: no effect on COBE mission.        | Microswitch did not fully close (make contact). 1 he microswitch T LM suddenly indicated a "lock" condition.                                   | None possible - potentiometer telemetry shows deployment to be 10070.   | Always provide backup device to microswitch.   | (     |
| 101059  | AP      | Gamma ray spectrometer | Electronics       | Gain shift occurred in lunar orbit/sci data ok.  | Other causes   | Traced to aging characteristic of sensor. Pre-aged sensors w/simulated space environment.   | Age AGRS S/N 003 (flight spare unit) same manner as 004 (Apollo 16 flight unit). Verify GR! calibration valid each flight unit subsequent to age   | 72    |
| A00369  | DE      | Fine Sun sensor        |                   | Sun sensor beta angle electronics changed gain and bias settings for no known reason.  | Actual cause unknown. Suspect degradation of LM108 in processing electronics of one of four fine bit channels.                                 | beta read out continues to degrade with time. Use alpha information only in producing attitude information. Definite attitude not affected. |  | 456   |
|         | ERBS    | Sun sensors            | Harness (FRM SS2) | Incorrect alpha angles from sun sensor #2. Eight lsb telemetry bits are inverted. The ninth bit is incorrect.  | Spacecraft sun sensor #2 was wired incorrectly. (That is, harness from sun sensor #2 to the electronics box was mis-wired two wires reversed). | Flight dynamics (code 581) changed their ground calibrations to fully correct for this error in the spacecraft.                             | Flight dynamics (code 581) changed their ground calibrations to fully correct for this error in the spacecraft. Action to be taken follow-up: none.  | 72    |
| 11031   | Voyager | RF Sub-system          |                   | S-band HGA drive dropped 5 db analysis of trend data, indicating antenna drive has been decreasing and becoming increasingly noisy since day 289 (1977). This confirmed problem in the S-band SSA in S/C 32. | High thermal delta of the transistor - MSC 3005. Detailed defect of the transistor remained unknown - probably wearout phenomena               | None.   | None - used as it was. Comments: for flights the MSC 3005 should be replaced with transistors having barrier rr and go through a extended burn-in. Performance was normal in the low power mode on amplifiers. | 189   |

From this table, it is apparent that some design failures (wearout is considered as a design failure in this discussion) during flight could have-been prevented by appropriate testing and design improvement, Test acceleration may be a feasible solution to mitigate flight failures occurring late in flight for long missions.

### 2.1.3 Calculation of Total Minimum Operating Time

The minimum operating time is determined based on the Duane graphical reliability growth model that has been used in industry for over a decade. The relationship between the initial and final mean time between failures (MTBF's) is given below:

$$\frac{\theta_F}{\theta_0} = \frac{1}{1-\alpha} \cdot \left( \frac{t_F}{t_0} \right)^\alpha$$

where:

$\theta_F$  = achieved final MTBF

$\theta_0$  = initial MTBF

$t_F$  = operational test duration

$t_0$  = initial test time (short burn-in time to correct for workmanship flaws)

$\alpha$  = growth rate

During operational testing, a S/C, is considered a repairable system, thus the reciprocal of its final MTBF is its failure rate at the beginning of flight. Since the initial and final MTBF vary exponentially with the growth rate, small variations in the growth rate result in significant changes in the achieved final MTBF or the operational test time duration.

Test durations, shown in Table III, are calculated with the following assumptions:

1. The subsystems or a combination of them have been functionally tested prior to S/C integration,
2. All test times are additive.
3. The design and construction of interplanetary S/C are similar to Earth orbiters.
4. The test failure correction uses an aggressive, industry-recommended average reliability growth rate of  $\alpha = 0.6$ . For further cost savings, a more aggressive failure investigation and correction process may be introduced to achieve a higher reliability growth rate of  $\alpha = 0.65$ .
5. Test failure modes include design, workmanship, and random failures.
6. Scored test failures are critical at the subsystem level and one failure is fatal. All failures are assumed independent. However, in the case of critical, dependent/induced failures, only the first, original failure is scored,
7. The failure rate at launch is assumed to be 10 times the desired mission failure rate, as per widely-accepted industry rule for newly-developed or newly-produced items.
8. Mission duration does not have any influence on test duration. The S/C are designed and constructed as per mission duration requirements,

Table 111. Operational Test Duration, Calculated for Average Reliability Growth Rates of  $\alpha = 0.6$  (currently attainable with existing JPL failure investigation and concurrent engineering practices) and  $\alpha = 0.65$  (Recommended for Faster Better Cheaper Missions).

| Item  | Failure Type        | Calculated Test Duration, $\alpha = 0.6$ (hours) | Calculated Test Duration, $\alpha = 0.65$ (hours) |
|---|---------------------|--|---|
| Subsystems, a group of subsystems, or a single string s/c.                | Design              | 500  | 350   |
|   | Workmanship         | (see Note 2)                                     | (see Note 2)                                      |
|   | Random (see Note 1) |  |   |
| Integrated system (assumed integration completed after subsystem testing. | Workmanship         | 200<br>(see Note 3)                              | 170<br>(see Note 3)                               |
|   | Design              |  |   |
| Total Test Time   | Worst case          | 700<br>(see Note 4)                              | 520<br>(see Note 4)                               |
|   | Normal              | 500<br>(see Note 5)                              | 350<br>(see Note 6)                               |

Note 1. Reduced random failures assume system improvement (i.e. a better quality or higher rated component, design improvement, fault protection, etc.). Replacement of the failed component does not guarantee elimination of a future failure of the same component.

Note 2. Test times can be accumulated during various engineering evaluation or environmental tests.

Note 3. Additional test times at the integrated system level are needed to screen for workmanship or design (compatibility) defects that may be introduced during integration or as a result of subsystem interaction.

Note 4. This is a case in which all tests are conducted sequentially.

Note 5. Normally, 300 hours at the subsystem level and 200 hours at the integrated system level, giving the required total of 500 hours.

Note 6. Normally, 180 hours at the subsystem level and 170 hours at the integrated system level, giving the required total of 350 hours.

The number of test cycles of mechanical devices depends on whether they have previously been tested. Mechanical devices, in most cases, are also subject to normal wearout. Therefore, the number of test cycles depends on the desired mission reliability. If the average number of wearout desired is 4 (normally the case with mechanical cycling devices), then the number of test cycles should be 1.7 times the required mission cycles. However, for Faster Better Cheaper Missions it is recommended that 1.5 times the required mission cycles be used, resulting in an increased average number of wearout of between 5 and 6.

Software operation cannot be separated easily from the hardware's and its reliability must also be taken in consideration. The software should be tested with a test compression factor and its reliability determined with a test duration determined based on the required or desired reliability.

### 3.0 Tradeoffs

System operation time is both a cost and schedule driver. Operation time may be reduced to prolong the useful life of devices that are subject to wearout, if cycling time has been accumulated. At JPL, the minimum operating time for an integrated system may be reduced if operating times have been accumulated on individual assemblies, operating times at the assembly (unit) level may be sufficient to disclose failure modes, such as poor solder joints, out of spec operation, parameter variation, materials interference, PCB defects, etc. The accumulated test times on assemblies under

various test conditions (environmental or engineering evaluations) can considerably reduce the minimum operating time required for the integrated S/C system, and still provide reasonable verification of S/C integrity, robustness, and expected mission reliability.

Failure mode sensitivities and cost tradeoffs for the minimum operating time and minimum operating cycles requirements are illustrated in Table 1 V. During minimum time operation it is also important to exercise all potential combinations of operating modes of the hardware at least once to identify mission critical modes.

Table IV. Control Parameter Sensitivity and Cost Sensitivity.

| Requirement       | Control Parameters     | Failure Modes          | Sensitivity to Increased Failures |    |    |    | cost              |   |  |
|-------------------|------------------------|------------------------|-----------------------------------|----|----|----|-------------------|---|--|
|                   |                        |                        | dur                               | ES | TS | MS |                   |   |  |
| Operating Time    | Duration               | Funct. anomaly         | +                                 | +  | +  | 0  | Duration          | + |  |
|                   | Electrical stress (ES) | Out of spec. operation | +                                 | -  | +  | 0  | Electrical stress | + |  |
|                   |                        | Elect-wear             | +                                 | +  | -  | 0  | Thermal stress    | - |  |
|                   |                        | Shorts                 | +                                 | +  | 0  | +  | Mechanical stress | + |  |
|                   | Thermal stress (TS)    | Mechanical stress (MS) | Poor solder joints                | +  | +  | +  | +                 |   |  |
|                   |                        |                        | Parameter variation               | +  | +  | +  | 0                 |   |  |
|                   |                        |                        | Open circuits                     | +  | +  | +  | +                 |   |  |
|                   |                        |                        | Cracks                            | +  | 0  | +  | +                 |   |  |
|                   |                        |                        | Poor bonding                      | +  | -  | +  | +                 |   |  |
|                   |                        |                        | Poor interfaces                   | +  | +  | 0  | +                 |   |  |
| (racked CB traces |                        |                        | -                                 | 0  | +  | +  |                   |   |  |
| Operating Cycles  | Duration               | Braking                | +                                 | 0  | 0  | +  | Duration          | + |  |
|                   | Electrical stress (ES) | Deformation            | +                                 | 0  | +  | +  | Electrical stress | + |  |
|                   |                        | Elect-wear             | +                                 | 0  | +  | +  | Thermal stress    | + |  |
|                   |                        | Shorts                 | +                                 | +  | -  | +  | Mechanical stress | + |  |
|                   | Thermal stress (TS)    | Mechanical stress (MS) | Poor solder joints                | +  | +  | +  | +                 |   |  |
|                   |                        |                        | Parameter variation               | +  | 0  | +  | 0                 |   |  |
|                   |                        |                        | Open circuits                     | -  | +  | +  | -                 |   |  |
|                   |                        |                        | Cracks                            | +  | 0  | -  | +                 |   |  |
|                   |                        |                        | Poor bonding                      | -  | +  | -  | +                 |   |  |
|                   |                        |                        | Poor interfaces                   | -  | +  | +  | +                 |   |  |

#### 4.0 References

- 1, MIL-STD-1450C, Test Requirements for Launch, Upper-Stage, and Space Vehicles.

#### 5.0 Bibliography

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2. MIL-H18718 Reliability Test Methods, Plans and Environments for Engineering Development, Qualification and Production.
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## 5. System Level Fault Tree

### 1.0 Objectives

The System Level Fault Tree (SFT) pictorially depicts those failure modes that result in mission failure. In addition, the SFT identifies single point failures (SPFs) and depicts mitigating design features that are implemented. The SFT analyzes and documents the significant high-level system functional failure modes that are important to various phases of the mission. The SFT provides a seamless link between the system level functional failure modes and the failure modes identified in the subsystem Failure Modes, Effects and Criticality Analyses (FMECAs).

### 2.0 Typical Requirements

Develop a spacecraft level fault tree for each of the mission phases (i.e., launch, cruise, orbit insertion, tour, etc.). Depict the spacecraft and ground system functional failure modes for those phases. Guidelines for performing Fault Tree Analysis (FTA) are provided in JPL D-5703 (Ref. 1). The SFT is supported by the subsystem level FMECAs.

### 2.1 Rationale

The SFT approach provides a systematic, logic based, graphical approach to analyze and document the major failure modes that can lead to loss of the mission. The SFT displays the logical relationship between the system level failure modes and the lower level events that lead to these failure modes. This representation provides the development team, from the manager to the working level engineer, with a view of significant threats to the mission. It also offers the team and its review board a chance to add failure modes not yet included in the model. This improves the chances of including a complete set of failure modes. The guidelines in JPL D-5703 are provided to promote uniformity of analysis methods within and across various projects. This approach is beneficial for both the preparer and the independent reviewer.

#### 2.1.1 Relevant Failure Modes

The SFT can be used to represent all possible failure modes, but its presence or absence does not avoid or cause any one specific failure mode. The SFT is, however, especially useful in identifying interface problems between two or more hardware elements when one element has a failure and another is required to perform some function to mitigate the effects of the failure. For example, consider a design where there is no autonomous fault protection that deals with a particular failure. In this case the plan is to have ground support respond to the failure with some mitigating action. If the required response time is significantly shorter than the mission two-way light time, the ground system action would be of no use. This type of situation could, and has been found and corrected,

#### 2.2 Methods

The SFT should be developed in the early design phases, and progressively refined and updated as the design evolves. The initial SFT will generally represent high level functional blocks (e.g., units, equipment, etc.), but later become more definitive at lower levels as the design matures. The first step in developing the SFT is to develop Functional Flow Diagrams (FFD) depicting all the functions required to achieve the mission objective. The FFD depicts all the ways the top level function is achieved. For example, if there is block or functional redundancy within the spacecraft the alternate paths for providing the function are depicted. Once the FFD is completed, the SFT can be developed. In the SFT, the top level functional failure is indicated as well as all the lower level events that can lead to the top level failure. Some failure modes require only one of several

events to lead to the upper level failure. In this case, the lower level failure would be depicted as inputs to an "or" gate under the upper level failure, thus indicating that any one of these events would lead to the upper level failure. Other failure modes require two or more events to lead to the upper level failure. In this case the lower level events would be depicted as inputs to an "and" gate under the upper failure, thus indicating that all of the events under the "and" gate are required for the upper level failure to occur. As is done in the FFD, block or functional redundancy is depicted in the SFT. In most cases, various phases of the mission require slightly different lower level functions, so each phase may have a distinct SFT. These can be considered as subtrees of the overall mission SFT. Guidelines for performing FTA are provided in JPL D-5703 (Ref. 1).

### **3.0 Tradeoffs**

The project tradeoff for doing the SFT is based on the actual cost of developing the SFT model versus the reduction in expected cost (in a probabilistic sense) associated with an unidentified inflight failure occurring. Specifically, the actual cost includes: developing the functional flow diagrams, the SFT models and the associated design interface support. These actual costs are compared to the reduction in expected cost of an inflight failure. The latter cost is based on several factors including: the reduction in the probability of an inflight failure associated with an unidentified failure mode, the fraction of the mission lost and the monetary value of the lost spacecraft/science. A second project tradeoff to consider when offsetting the cost of SFT is the avoided cost of redesign if SFT was not done, but a serious failure mode was found late in the development cycle requiring design changes to prevent it from occurring.

### **3.1 Effectiveness Versus Failure Modes**

As mentioned in section 2.1.1, SFTs do not avoid any specific failure mode, but do depict and facilitate an understanding of all known failure modes and interactions between elements of the spacecraft. The SFT model development, if done rigorously, increases the chance of launching a spacecraft with no unidentified or inadequately mitigated failure mode. It should be acknowledged that neither SFT nor any other form of analysis can be guaranteed to identify all possible failure modes. However, SFTs are very effective tools for systematically analyzing, documenting and communicating information about failure modes and their mitigation on both simple and complex systems.

### **3.2 Sensitivities**

SFT methods are straight forward, but accurately representing a spacecraft design requires a somewhat unique combination of System Engineering, Software Engineering and the failure mode analysis skills of a Reliability Engineer. If personnel possessing the relevant skills are assigned to the task, very complex spacecraft, such as Cassini, can be accurately represented at a cost of two to three work years. Otherwise, the cost could be substantially higher and the resulting model could be of much less value. In summary, the most important parameters are the SFT analyst and the design information available to develop the model. Other parameters that influence types of failure modes detected by the SFT and the cost of performing the SFT are identified in Table 1.

Table 1. Control Parameter Sensitivity and Cost Sensitivity

| Requirement             | Control Parameters (1')       | Effectiveness (E) vs Failure Modes (generic, specific) for default parameters | Parametric Sensitivity (dE/dP)<br>+ more effective<br>0 neutral<br>- less effective |    |   |     |    |    |    |    |    |    |    | Cost Function (p)             |                         |   |
|-------------------------|-------------------------------|---|---|----|---|-----|----|----|----|----|----|----|----|-------------------------------|-------------------------|---|
| System Level Fault Tree | S/C Complexity (CX)           |   |   |    |   |     |    |    |    |    |    |    |    |                               | S/C Complexity (CX)     | + |
|                         | Link to S/S FMECA (FL)        |   |   |    |   |     |    |    |    |    |    |    |    |                               | Link to S/S FMECA (FL)  | + |
|                         | No. Dev Partners (N)          |   | Cx  | FL | N | MI' | ML | SI | MR | TS | DM | FP | Sw | No. Dev Partners (N)          | +                       |   |
|                         | Mission Phases (MP)           |   |   |    |   |     |    |    |    |    |    |    |    |                               | Mission Phases (MP)     | + |
|                         | Mission Life (ML)             | Interface Errors  | +   | -  | + | +   | +  | +  | +  | +  | -  | -  | -  | Mission Life (ML)             | +                       |   |
|                         | No. Science Instru (SI)       |   | 1   | 1  | 1 | 1   | 1  | 1  | 1  | 1  |    |    |    |                               | No. Science Instru (SI) | + |
|                         | Margins [Pwr, Men, Mass] (MR) | In-ID'd S/S Function Failures   | +   | -  | + | +   | +  | +  | +  | +  | -  | -  | -  | Margins [Pwr, Men, Mass] (MR) | 0                       |   |
|                         | Dev Team Size (TS)            | In-ID'd S/S Part Failures   | +   | -  | + | +   | +  | +  | 0  | 0  | -  | 0  | 0  | Dev Team Size (TS)            | +                       |   |
|                         | Dev Mode [Cling] (DM)         |   |   |    |   |     |    |    |    |    |    |    |    |                               | Dev Mode [Cling] (DM)   |   |
|                         | Fault Protection (FP)         |   |   |    |   |     |    |    |    |    |    |    |    |                               | Fault Protection (FP)   | + |
| s/w IV&V (SW)           |                               |   |   |    |   |     |    |    |    |    |    |    |    | S/W IV&V (SW)                 |                         |   |

4.0 References

1. JPL 1>-5703, "Jet Propulsion Laboratory, Reliability Analyses Handbook", prepared by Project Reliability Group, July 1990. "

## 6. Electronic Parts Stress Analysis

### **S.0 Objectives**

The highest level objective is developing spacecraft which meet the reliability expectations of a specific program. One of the activities used to assure high reliability of electronic circuits is derating of the circuit components to reduce their failure rates. Derating provides the circuit components with reduced failure rate and robustness, so if unexpected conditions (e.g. increased duty cycle, warmer than expected operating temperatures, etc.) develop, the components will not fail prematurely. The objective of reducing failure rates of electronic circuit components during space missions is achieved when the lower level objective of validating, via Part Stress Analysis (PSA), that the design meets the parts derating criteria is met.

### **2.0 Typical Requirements**

Perform electrical circuit analysis on all electronic and electromechanical hardware to validate that stress levels on circuit components comply with derating requirements, under worst case conditions. The electronic PSA is supported by a piece part thermal analysis. Guidelines for performing PSA are provided in JPL D-5703, (Ref. 1).

#### **2.1 Rationale**

Electronic circuit components are prone to early failure when overstressed, (i.e., excessive power dissipation, high current, over voltage, high junction temperatures, etc.). Conversely, reduced failure rates can be achieved by reducing circuit component stress levels by design practices that reduce stress levels. Reducing circuit component stress levels has become well developed and is called "Derating". Electronic PSA verifies compliance with the derating requirements. The guidelines in JPL D-5703 are provided to promote uniformity of analysis methods used by various hardware suppliers, within and across various projects.

#### **2.1.1 Relevant Failure Modes**

Typical relevant failure modes are:

1. Design, Parts, Parts Stress/Selection/Wear out/Aging.
2. Design, Life, Deterioration/Random Failure.

Note: Not included in this miniproduct are unacceptable functional failures due to component degradation with age and stress levels. These functional failures are addressed in the circuit Worst Case Analysis (WCA).

#### **2.1.2 Supporting Data**

As indicated in Section 3.1, PSA is virtually the only gate that validates that components in the electrical/electronic circuit comply with their derating requirements. This is manifested by the lack of JPL ground testing PFRs that are related to overstressed components. In addition, there are no known inflight failures on JPL programs that were linked to component overstress. Only a few ground testing problems have been linked to errors in the derating validation as indicated in the Table 1,

| Table 1. OVERSTRESS-RELATED PFRs of JPL's MISSIONS |      |                          |                                     |
|--|------|--------------------------|-------------------------------------|
| Program  | Year | Subsystem                | Failure mode                        |
| Mars Observer                                      | 1991 | Camera                   | Over-voltage to transistor          |
| Sir-C  | 1992 | Replay/Stow Control Unit | Overstress of Opto-isolators        |
| Sir-C  | 1993 | RF Electronics           | Over current through relay contacts |

## 2.2 Methods

Electronic PSA uses electrical circuit analysis to verify that the circuits' components comply with the derating requirements of Mil-Std-975, Appendix A, under all expected operating conditions, including short term transients associated with on/off switching, mode changes, etc. In most cases, the PSA (and the circuit Worst Case Analysis) require a supporting piece part thermal analysis. To simplify the analysis and provide a conservative design, the PSA is done using worst case assumptions. These assumptions include: 1) initial component variations, 2) environmental extremes plus margins, especially ambient temperatures, the thermal rise to the component and component internal thermal rise, 3) input variations plus margins, including voltages, currents, frequency, and duty cycle, and 4) outputs, including variations in load impedance. Guidelines for performing PSA are documented in JPL D-5703. It should be noted that PSA does not address protecting circuit components from the transient effects of Electrostatic Discharge (ESD).

## 3.0 Tradeoffs

Since most stress related early failures are not detectable in the normal ground testing program, the PSA tradeoff evaluation considers the cost of performing the analysis versus a reduction in expected cost (in a probabilistic sense) of a premature failure during the mission by avoiding overstressed circuit component parts. Specifically, the actual cost of providing the PSA is compared to the change in expected cost of an premature inflight failure. The latter is based on the change in the probability of premature inflight failure, the fraction of the mission lost and the monetary value of the lost spacecraft science. Another issue to consider when offsetting the cost of the PSA is the avoided cost of redesign that might be required if overstressed circuit components are discovered late in the development cycle.

### 3.1 Effectiveness Versus Failure Modes

PSA is very effective in avoiding over-stress in electronic circuit components and the associated premature failures during the mission. In fact, the PSA is virtually the only gate that validates the designer's nominal circuit design complies with the derating requirement during adverse conditions. Stated another way, there are no other activities, including tests which validate that circuit components meet their derating requirements. Consequently there is no way of verifying that the circuits components will survive for the duration of the mission. Accelerated testing at elevated temperatures could be used to identify the "weak link" in the circuit components, but this approach does not directly reveal information about the other circuit components, so it has not been used extensively.

### 3.2 Sensitivities

The sensitivity of premature mission failures to "doing/not doing" PSA is potentially significant, unless the original circuit design includes the validation that circuit components meet their derating requirements under equivalent PSA conditions. "There is a monetary cost associated with expanding the basic circuit analysis to include the derating validation, but that cost should be less than a separate PSA performed by a different analyst, Table 11 identifies PSA parameters and their influence on failure modes detection and the cost of performing PSA.

Table II. Control Parameter Sensitivity and Cost Sensitivity

| Control Parameters (l)      | Effectiveness (1) vs Failure Modes (generic, specific) for default parameters | Parametric Sensitivity (dF/dP)                    |    |    |    |    |    |   | Cost Function (p)           |   |
|-----------------------------|---|---|----|----|----|----|----|---|-----------------------------|---|
|                             |   | + more effective<br>0 neutral<br>- less effective |    |    |    |    |    |   |                             |   |
| Circuit Complexity (CC)     | Over Stressed Components  | CC  | QT | FA | DT | ML | DC | A | Circuit Complexity (CC)     | + |
| Qual Temp (QT)              | -Electromigration   | +   | +  | ±  | 0  | +  | +  | + | Qual Temp (QT)              | 0 |
| Flight Allow Temp (FA)      | -Interface Diffusion  | +   | +  | +  | +  | +  | +  | + | Flight Allow Temp (FA)      | 0 |
| Delta-T [S.Plate-Part] (DT) | -Dopant Migration   | 0   | +  | +  | +  | +  | +  | + | Delta-T [S.Plate-Part] (DT) |   |
| Mission Life (ML)           | -Over temp of Components  | +   | +  | +  | +  | 0  | 0  | 0 | Mission Life (ML)           | + |
| Ckt Duty Cycle (DC)         | -Phase Change   | +   | +  | +  | +  | 0  | 0  | 0 | Ckt Duty Cycle (DC)         | 0 |
| RSS vs EVA (A)              | -Out Gassing  | +   | +  | +  | +  | -0 | 0  | 0 | RSS vs EVA (A)              | + |
|                             | Performance Degradation   |   |    |    |    |    |    |   |                             |   |
|                             | -Timing   | +   | +  | +  | +  | +  | +  | + |                             |   |
|                             | -Output Voltage   | +   | +  | +  | +  | +  | +  | + |                             |   |

4.0 References

1. JPL D-5703, "Jet Propulsion Laboratory, Reliability Analyses Handbook", prepared by Project Reliability Group, July 1990.

## 7. Unit Level Temperature Design Requirement

### 1.0 Objectives

Design requirements are used to ensure that the hardware is designed, built, and tested to be compatible with the spacecraft, as well as with other hardware. Temperature design requirements are used to ensure that the assembly (unit) will operate as intended over the range of mission environments seen during its life, including assembly, test, and launch operations.

Design requirements usually include margin beyond the intended use environment. These margins are used to account for any differences between the ground activities and the mission environment. They are also intended to provide a buffer for variations in the intended application, inherent uncertainties in the predicted mission temperatures, and to provide for testability at higher levels of integration.

The temperature design requirements need to be compatible with the thermal test requirements, since the thermal tests are a critical part of the overall reliability demonstration for an assembly (unit). A typical set of temperature design requirements has the widest temperature ranges at the assembly (unit) level, with gradually narrowing range for the subsystem, and finally system levels. This ensures that the assemblies are robust enough for their application, and that their capabilities are well outside what they will be subjected to on the spacecraft. This not only increases confidence in the reliability of the assembly (unit), but it also results in available flexibility in mission operations if the available margin is known.

### 2.0 Typical Requirements

The typical temperature design requirements consist of the following components: 1) operating temperature range; 2) non-operating temperature range; and sometimes: 3) survival temperature range; and 4) in-spec operation temperature range.

These parameters address the needs and uniqueness of each assembly (unit) and mission. The temperature design requirements must be coordinated with the thermal test requirements for the assembly. The design requirements must, at minimum, encompass the expected test temperatures (which, in turn, encompass all the temperatures seen throughout the life of an assembly).

#### Operating Temperature Range

The operating temperature range is the range over which the assembly (unit) must operate and meet the applicable functional requirements. This range is typically -20 to 75 °C or greater, and provides compatibility with the thermal test requirements for the assembly (unit), and minimizes problems when testing at higher levels of assembly.

#### Non-operating Temperature Range

The non-operating range is often the same as the operating temperature range above. However, it can be used to define 'survival extremes' (see below). If the operating temperature range encompasses all operating and non-operating scenarios for the assembly (unit), the non-op range is not used. If the assembly (unit) is expected to be powered off for some conditions, then a non-operating range can be defined which is wider than the operating temperature range. The assembly is designed to turn on safely at the extremes of the non-operating temperature range, and return to in-spec. functional performance as the temperatures return to the operating range. This allows for S/C safing modes, loss of attitude control, and other modes in which the assembly (unit) is not required to operate within specified functional requirements. This requirement is mission specific.

### **Survival Temperature Range**

A survival temperature range is occasionally specified. This is usually defined as an extreme temperature that the assembly (unit) can be exposed to, yet turn on and operate without degradation after returning to a more benign state. Survival temperature requirements mostly affect the rupture, or hysteresis failure modes, encompassing mechanical, packaging, and tolerances within an assembly (unit). Fluid filled devices, or other devices relying on sealing must retain their integrity in such a condition, Survival temperature requirements are mission specific.

### **In-specification operating Temperature Range**

In designing assemblies for space use, certain technologies exhibit temperature dependence that make it prohibitive to expect compliance with all functional specifications over a wide temperature range. Typical of these are RF systems, optics, and some mechanisms. In order to accommodate this, these types of assemblies are usually devoted special resources in the system design to maintain them within a tighter temperature range than other subsystems. Correspondingly, the temperature design requirements can specify a narrower range in which in-specification operation is required. The performance is allowed to degrade outside this narrower range. This performance degradation, however, is expected to be predictable and repeatable, returning to a stable, in-spec functional state as the temperature returns to the specified range. This requirement is usually an addendum to the operating temperature requirement, and it varies on a case by case basis. However, typical in-spec temperature ranges have been 5 to 55 °C for some recent projects.

## **2.1 Rationale**

Temperature affects most mechanical and electrical designs due to material property dependencies on temperature, temperature induced tolerance changes, and temperature effects on electronic device parameters. These effects must be accounted for in the design of structures, mechanisms, and circuits in order for the design to function as intended when exposed to the various temperature regimes seen throughout the life of an assembly (unit).

### **2.1.1 Relevant Failure Modes**

Some temperature induced effects on assemblies are listed by type:

#### **Structures (both macro and micro):**

1. Subject to internal stresses due to temperature and CTE (coefficient of thermal expansion) mismatches - these can result in either rupture, unwanted deformation, or early fatigue failure. These stresses can be residual due to processing history, or can be induced by the operating environment.
2. Low cycle fatigue can be induced by cyclic temperature variations. Primarily seen in electronic interconnects such as vias and solder joints.
3. Interfacial stresses can result in cracking and failure of bonded joints, or in cracking or delamination of the materials on either side of a bonded joint.

#### **Electronics:**

1. Functional failures can be experienced due to electronic component parameter variations which are temperature dependent. Examples are: transistor gain, diode forward current, CMOS switching speed (and hence power dissipation) variations, timing margins, and voltage thresholds, among others.
2. Start-up transient conditions such as excessive inrush current can be caused by temperature effects on the components.
3. Device failure mechanisms such as electromigration and time dependent dielectric breakdown, among others are accelerated to varying extents by temperature. For failure mechanisms with positive activation energies (those just mentioned), extended high temperature operation will

lead to early device failure. Conversely, for failure mechanisms with negative activation energies, such as hot carrier injection, cold temperatures will accelerate the failure mechanism, 4, Extreme temperature conditions can also combine with electrical parameters to result in part overstress.

#### **Mechanisms:**

1. Tolerance variations due to CTE effects.
2. Variation in motor torque output and current draw.
3. Fluid viscosity and density changes that can lead to leakage, deformation, or undesired operational characteristics.

#### **Optics**

Optical systems are typically sensitive to temperature variations. Performance of reflective optics is dependent on the distance between and alignment of optically reflective surfaces. Dimensional changes will affect the focal point of the system. Refractive optics have additional sensitivities due to the variation of the index of refraction with temperature. Low CTE materials are used to minimize dimensional changes, and lens and mirror mounts must accommodate dimensional changes without inducing large stresses in the optical elements. Residual stresses in the materials due to machining can aggravate the temperature sensitivity of optical structures. Optical coatings and filters are usually sensitive to temperature, indicated by either performance changes, or accelerated degradation.

#### **Synergism**

Since so many electronic and optical parameters are affected by temperature, derating guidelines have been developed by the industry to enhance the life and reliability of electronic parts under various applications. When establishing design temperatures for electronic assemblies, it is important to work closely with the environmental compatibility, reliability, and parts experts to establish a coherent policy for the project which performs the tradeoffs necessary to arrive at an optimal set of design and test requirements. The same holds true for other types of assemblies. An apparently more restrictive requirement on one assembly (unit) may result in a much more relaxed requirement on a system. The subsystem and system must be considered when deciding on the assembly (unit) requirements, in order to avoid decisions which will result in unnecessary constraints on other assemblies, or higher levels of integration.

#### **2.1.2 Supporting Data**

One measure of the effectiveness of designs to accommodate the necessary temperature ranges is to examine the number of design related problems found in the test program. Although design problems are not indicators of the effectiveness of the requirement, they do point to the need for a designer to be aware of and adequately address the temperature effects on a given assembly (unit).

The P/FR database was searched to find P/FRs generated during thermal tests, and among these, to isolate design related P/FRs. The projects searched included Galileo, Mars Observer, Topex, MGS, NSCAT, SeaWinds, Cassini, MISR, and Mars Pathfinder.

The search priorities were: for the environment, temperature; and for the cause, design. Out of 775 total P/FRs for these projects, 130 (1796) of them satisfied the search criteria of originating during various temperature environments, and the cause attributed to design issues. Table 1, below shows the 130 P/FRs broken down by type of design problem.

**Table 1 - Distribution of Design Related P/FRs by Cause**

| Cause of Failure               | Number of occurrences | Percentage of Total |
|--------------------------------|-----------------------|---------------------|
| Design (unspecified)           | 44                    | 34                  |
| Functional Application         | 27                    | 21                  |
| Packaging or Mounting          | 7                     | 5.5                 |
| Producibility                  | 24                    | 18                  |
| Parts/Materials Misapplication | 21                    | 16                  |
| Tolerance Call-out             | 7                     | 5.5                 |
| <b>Total</b>                   | <b>130</b>            | <b>100%</b>         |

It is clear that a design requirement alone does not result in a good design, however, the requirement creates the awareness that temperature issues need to be accounted for in the design. It can be seen from the table above, that no one particular design problem dominates the types of failures observed. It is interesting to note that these design problems range from packaging and materials issues to specifications issues.

A close scrutiny of the P/FRs found that of the 130 initially flagged, 36 were not attributable to temperature effects, reducing the total related to design problems found during temperature testing to 94 out of 775, or 12%. The distribution of failures by design type remains approximately the same.

### 3.0 Tradeoffs

The temperature design requirement is necessarily tied to the temperature test requirement. The design must, at minimum, accommodate the qualification temperatures. Given this, it is more appropriate to make the tradeoffs on the test requirements. The assembly (unit) temperature test requirement write-up will address the tradeoffs that can be made in that area.

One trade-off that can be made is in the system design. The project and the system architects should carefully consider the tradeoffs between system level and assembly (unit) level requirements. Often the decision is made to restrict the operating temperature range of the assemblies in order to realize cost savings in procuring the assemblies. In considering such a decision, the project should be sure that the restricted temperature range would result in real cost savings at the assembly (unit) level. The project should also evaluate the resulting impact on the system level design due to increased constraints on the system level thermal control, which can result in increased mass, heater power requirements, and constrained equipment layout.

### 3.1 Sensitivities

in establishing temperature design requirements for assemblies, the parameters that can be varied are: temperature, in-spec operating range, and survival (or non-operating range). Table 2, below, attempts to show the impact of changes in these parameters to: 1) the effectiveness in mitigating the failure mechanisms discussed above; and 2) the cost of the assembly (unit).

**Table 2 - Control Parameter Sensitivity and Cost Sensitivity.**

| Control Parameters      | Failure Modes                               | Sensitivity to Parameter |         |          | Cost Sensitivity to Control Parameter |               |
|-------------------------|---|--------------------------|---------|----------|---------------------------------------|---------------|
|                         |   | T                        | in spec | surv     |                                       |               |
| Temperature Levels (T)  | Structural/packaging                        | +                        | +       | +        | Temperature Level                     | +/0 -i<br>(1) |
| In-Spec Range (in spec) | Electrical performance /parameter variation | +                        | +       | 0        | In-Spec Range                         | +/0<br>(1)    |
| Survival Range (surv)   | Optical performance                         | +                        | +       | 0<br>(2) | Survival Range                        | 0<br>(3)      |
|                         | Time dependent failures (Arrhenius)         | +                        | 0       | 0        |                                       |               |

- Notes:
- 1 ) Not a cost driver over typical temperature ranges (-20/+70 °C). RF and optics assemblies may have cost impact due to strong temperature sensitivity of their performance.
  - 2) Survival temperature is not a driver, unless the range is wide enough to cause permanent change in the optics structure.
  - 3) Not a cost driver unless effect mentioned in (2) is an issue.

Temperature design requirements, while not guaranteeing a quality design, do define many issues to be addressed during the design process. Tolerances, material compatibility, electrical parameter variations, and functional requirements all need to be considered when designing to operate in a given environment, It is also important to note that the temperature design requirements need to be closely tied to the test requirements, as well as the part stress analysis, derating, and worst case analysis requirements in order to assure consistent application of environmental requirements.

## 8. Unit Level Thermal Test Requirement

### 1.0 Objectives

The objective of unit level thermal testing is to demonstrate the flight worthiness of the hardware. This is done by simulating the relevant synergistic environmental and operational conditions through selection of appropriate combinations of environmental, electrical and mechanical parameters. To be effective, parameters should be selected that validate the design, demonstrate its robustness, screen for workmanship defects, and demonstrate an acceptable level of reliability. Thermal tests are designed to be non-destructive and are performed under either vacuum or atmospheric pressure conditions.

### 2.0 Typical Requirements

The typical unit level test requirement consists of the following parameters: test pressure, operating temperature range, non-operating temperature range, dwell times, temperature transition rates, number of temperature cycles, and functional testing,

These parameters are chosen to best achieve the test objectives for a given unit and mission. The test parameters are necessarily synergistic with the temperature design parameters for the unit, and must encompass all the temperature regimes experienced throughout the life of the unit. These parameters will be discussed in more detail in more detail in section 2.1, outlining the effect of these parameters on the failure mechanisms involved and on the effectiveness of the test.

A typical unit thermal test requirement is:

Hot/Cold Temperature Level (operating): -20/+75 °C

Hot/Cold Duration: 144/48 hrs

Number of Cycles: 1

Pressure:  $<10^{-5}$  Torr

Rate of Change of Temperature: 30 °C/hr

Functional Testing: to demonstrate in-spec operation over a temp range

This example is typical of traditional test requirements for assemblies used in long life planetary exploration missions. These requirements are tailored as mission requirements and program needs change.

### 2.1 Rationale

A well designed and implemented thermal vacuum test can expose most of the relevant failure modes. Published data shows that thermal vacuum testing is the most effective environmental test for space hardware. The following is a discussion of the rationale for the significant variables that affect the effectiveness of a thermal vacuum test.

**Functional Testing:** Functional tests are necessary to verify the performance of the hardware during environmental testing. Electrical stresses are combined with environmental stresses to effectively apply screening stresses to the hardware under test. Because of the synergism between the electrical and thermally induced stresses, the effectiveness of an environmental test can be significantly influenced by the selection and performance of various functional tests during the environmental test. Functional tests should be designed to allow verification of unit level functional requirements, including in-specification operation of all modes over the full operational temperature range, stability, calibration, and demonstration of cold- and hot-start capability. In many cases, out of specification operation at or near the extremes of the temperature range is

acceptable as long as the performance comes back in specification within the required range, and no permanent degradation occurs.

**Test Pressure:** The pressure during test results in both thermal effects as well as purely pressure dependent phenomena. The effects associated purely with pressure include corona and multipacting. These are most often associated with RF or high voltage circuits and devices. Introduction of a gas to the test environment (even fractions of an atmosphere) introduces additional heat transfer via convection, which alters the temperature distribution within the unit. Therefore, the vacuum ( $< 10^{-5}$  Torr) environment is most representative of flight for unit thermal tests. However, testing in a dry 1 atmosphere environment is acceptable if it has been shown that the hardware is not subject to corona and multipacting, and the internal temperature levels have been calculated and can be achieved by adjusting the test temperatures.

**Temperature Level:** For most failure mechanisms associated with space flight electro-mechanical hardware, the hot temperature level is one of the key parameters impacting the effectiveness of the thermal test. In general, the higher the level the more perceptive the test (Reference 3). Cold exposures are effective in precipitating many latent failure modes, and complement high temperature exposures. These levels have typically been the greater of  $-20/+75$  °C, or 25 °C beyond the worst case predictions. These levels assure robust screening of the hardware, in addition to providing adequate margins to account for environmental and modeling uncertainties.

**Duration:** The reliability of an electronic unit in flight is directly related to the number of operating hours experienced prior to flight. Additionally, since increased temperature accelerates many failure mechanisms, the time spent operating at elevated test temperatures is equivalent to a greater time spent operating at lower temperatures. The test dwell time can be traded off for increased operating time in other environments. However, since realistic acceleration factors must be used, this tradeoff should only be done after consulting with the project reliability engineer. Non-operating dwell times are not necessary unless the hardware is subjected to a hysteresis-type of mechanism.

**Rate of Change in temperature (dT/dt):** At high rates of change in temperature, large stresses can build up across material interfaces due to differential thermal expansion which can be significant enough to cause a failure of the material. There is concern that an excessive rate of change in temperature could cause possible failures which would not have occurred in flight. The current approach is to specify a rate of temperature change which is tied to the maximum rate expected in flight. The rationale for this is that any savings associated with a higher rate would be insignificant and this would subject the hardware to levels that could be in excess of any previous qualification rates. The allowed rate of change in temperature is dependent on the design and previous qualification of the hardware. Typical electronic packaging designs used for space applications should be capable of supporting rates in the range of 10°C/minute.

**Temperature Stabilization:** Thermal stabilization is important when the hardware under test has an extremely long thermal time constant (time to reach thermal equilibrium), uses localized internal temperature control, or where hysteresis phenomenon is involved.

**Number of Thermal Cycles:** Performing a single thermal cycle is effective for precipitating a broad spectrum of latent defects. These range from workmanship defects (poor interconnect integrity, missing parts, wrong part value, etc.) to electrical, optical and mechanical design defects. Performing multiple thermal cycles is effective in testing for hysteresis effects and life testing (such as qualifying the capabilities of a technology). Since life testing is not intended to be part of a test on flight hardware, the number of cycles should be the minimum number necessary to verify stability and/or repeatability in performance.

**Heat Sinking Method:** Heat sinking the unit under test in the same manner as in flight aides in the detection of any deficiencies in the thermal coupling of the unit to the next level of integration.

### 2.1.1 Failure Mechanisms & Tradeoffs

For the purpose of this discussion, all failure mechanisms are grouped into one of three general classifications. They are: 1) chemical/diffusion mechanisms (Arrhenius reaction rates); 2) hysteresis; and 3) stress rupture. A high-level summary of each of these classifications is presented below. Each discussion is followed by a list of the test parameters that influence that failure mode.

#### **Chemical/Diffusion Reactions**

The fabrication of electronic parts, circuit boards and circuit-board assemblies involves complex chemical reactions. Failures as a result of residual reactants, incomplete reactions or diffusion/migration processes would be classified as being Arrhenius in nature. This failure mode is most often associated with electronic parts (Reference 1). Moreover, Reference 1 also indicates that this mechanism can be the leading source of failures for a significant number of other hardware elements,

Relevant test parameters (listed in estimated order of overall significance) are:

Electrical loads, Hot Levels (including pressure level effects), Hot Dwell Time, Cold Levels, Cold Dwell Time, Ramp Rate.

#### **Hysteresis**

The forms of hysteresis most often of concern in electro-mechanical hardware used in space flight are: fatigue (both high and low cycle) and parametric drift. Low cycle fatigue and parametric drift are a function of dwell time and number of cycles.

High Cycle Fatigue: high cycle fatigue failures are best exposed by vibration testing and therefore not discussed herein.

Low Cycle Fatigue: The life-limiting failure mechanism of typical packaging designs is low cycle fatigue of electro/structural interconnects. This damage mechanism largely results from a global mismatch of the CTE between: (1) part body and "the board it is mounted on, (2) the board and the board housing. Local CTE mismatches (between solder material and metal pad on the board) also contribute to the problem. Similar problems occur in materials with the same CTE's but where large thermal gradients exist within the solder joint/lead system.

The material properties which govern the life of solder interconnects are very non-linear (Reference 3). As a result, cyclic exposures which involve higher peak thermal exposures are significantly more effective than cyclic exposures of the same total depth but which involve a lower hot peak temperature. Moreover, below 0°C, eutectic tin/lead solder becomes significantly stronger, and thereby, most likely changes the failure mode for the interconnect from a low cycle fatigue failure of the solder material to a brittle failure of either the solder material or the part package.

Parametric Drift: Another form of hysteresis is parametric drift. It can be due to Arrhenius type reactions or residual stress effects. Thermal cycling generally removes/stabilizes these stresses.

Relevant thermal test parameters (listed in estimated order of overall significance) are:

Hot level, total depth of thermal cycle, cold level, hot dwell time, electrical loads, ramp rate, Pressure level.

### Stress Rupture

Stress rupture failure can be introduced via mechanical loading or thermal displacement as a result of a CTE mismatch or large thermal gradients. Excursions away from the zero stress and/or residual stress state (associated with the formation/fabrication processes) create stresses in the hardware. Most stress ruptures are suspected to occur as a result of manufacturing flaws or new designs. This is a typical weak link failure mode for bondlines and composites.

Relevant thermal test parameters (listed in estimated order of overall significance) are: Hot & Cold Levels, Electrical loads, Pressure level, Ramp Rate.

### 2.1.2 Supporting Data

Studies of test results indicate that the thermal vacuum test is the most flight-like environment achievable prior to launch, and it is the most effective environmental test for revealing inherent failure modes (Reference 4).

The following data is based on studies of the JPL Problem/Failure Report (P/FR) database, and summarize test experience on major JPL flight projects.

General Effectiveness of Thermal-Vacuum Test: Analysis of the data shows that approximately 25% to 30% of the problems found during testing of flight assemblies on the Voyager and Galileo programs would not have been detected except by environmental testing. Additional studies were conducted to compare the relative effectiveness of the two major environments, vibration tests and thermal tests. These studies found that thermal testing detects from 1.3 to 3 times as many problems as dynamics testing. See Reference 6 (TO-0003) for further details.

Effectiveness of Functional Tests: Two spacecraft (Galileo and TOPEX/POSEIDON) and two instruments (the Wide Field & Planetary Camera II (WF/PCII) and the NASA Scatterometer (NSCAT)) were studied by performing a trend analysis of the problem/failures detected during system level thermal/vacuum testing to provide some insight on the role and effectiveness of functional testing. Table 1 summarizes the findings of this study. Of 20 PFs relevant to the study, 40% (8) should have been detected during lower level testing. Conversely, 35% (7) involved "interface issues" which could only be resolved by higher level testing. The remaining 25% (5) were detected during lower level testing but were not effectively resolved to prevent future occurrence. See Reference 7 (TO-0027) for further details.

**Table 1. Summary of Functional Test Effectiveness observations**

| CLASSIFICATION OF PF DETECTION                           | SPACECRAFT | INSTRUMENTS | TOTAL |
|--|------------|-------------|-------|
| Undetectable At Lower integration Level                  | 7          | 0           | 7     |
| Potentially Ineffective Problem Resolution               | 3          | 2           | 5     |
| Potentially Ineffective Functional Testing At Unit Level | 4          | 4           | 8     |
| TOTALS   | 14         | 6           | 20    |

Effectiveness of Vacuum: The use of vacuum conditions during thermal testing of hardware can significantly increase the effectiveness of the thermal test as a screen for detecting hardware defects. References 2 and 4 report that thermal/vacuum testing is more effective for revealing defects than thermal/atmospheric testing.

Reference 8 documents a survey made of the P/FRs written during unit level and system level thermal/vacuum (T/V) tests for the Voyager and Galileo Projects (pre-1986) to determine the necessity of a vacuum environment along with elevated temperature for uncovering P/Fs. Tables 2 and 3 summarize the unit and system level findings of this study, respectively. Note that on both programs and both levels of testing, vacuum effects played a major role in detecting the problem/failure.

**Table 2. Unit-level TV Test**

| DEPENDENCY                    | VOYAGER   |            | GALILEO   |            |
|-------------------------------|-----------|------------|-----------|------------|
|                               | NUMBER    | PERCENT    | NUMBER    | PERCENT    |
| Temperature Only              | 9         | 19.6       | 7         | 19.4       |
| Temperature & Vacuum          | 10        | 21.7       | 17        | 47.2       |
| "Pure" Vacuum                 | 21        | 45.7       | 8         | 22.2       |
| Indeterminate                 | 4         | 8.7        | 3         | 8.3        |
| Other (functional only, etc.) | 2         | 4.3        | 1         | 2.8        |
| <b>TOTALS</b>                 | <b>46</b> | <b>100</b> | <b>36</b> | <b>100</b> |

**Table 3. System-Level TV Test**

| DEPENDENCY                    | VOYAGER   |            | GALILEO   |            |
|-------------------------------|-----------|------------|-----------|------------|
|                               | NUMBER    | PERCENT    | NUMBER    | PERCENT    |
| Temperature only              | 0         | 0          | 4         | 10.3       |
| Temperature & Vacuum          | 6         | 13         | 5         | 12.8       |
| "Pure" Vacuum                 | 29        | 63         | 14        | 35.9       |
| Indeterminate                 | 2         | 4.3        | 2         | 5.1        |
| Other (functional only, etc.) | 9         | 19.6       | 14        | 35.9       |
| <b>TOTALS</b>                 | <b>46</b> | <b>100</b> | <b>39</b> | <b>100</b> |

Hot Level and Dwell Period: Exposure to high temperature testing has been found to be effective in revealing design and workmanship defects. Precipitation of latent defects associated with all three types of failure mechanisms discussed in section 2.1.1 is accelerated by exposures to hot levels (Reference 3). Although time itself is not an acceleration mechanism, it increases the probability of detecting a latent defect during the test. Table 4 summarizes several examples of PFs that were temperature level and or time dependent. These findings arc from a study performed to

investigate and document specific examples of PFs which were dependent on high temperature exposures and/or time at high temperature. (See Reference 9 for further details.)

**Table 4 - Causes and Mechanisms of Thermal Vacuum Hot Test Failures for Galileo**

| PFR   | Failure Description   | Failure Mechanism   | Failure Physics  | Time (hr) | Temp (°c) |
|-------|---|---|--|-----------|-----------|
| 43996 | T/V test data output became intermittent,                       | Three pins were not soldered to circuit traces.           | High temperature caused expansion leading to the discovery of un-soldered pins.  | 10        | 55        |
| 42485 | Memory errors found while debugging (ref PFR 42492).            | Breakdown in gate oxide of one of the memory transistors. | Most <b>probably</b> a ESD latent defect.  | 83        | 75        |
| 42492 | Excess current detected in memory array(ref PFR 42492),         | Breakdown in gate oxide of one of the memory transistors. | Most probably a ESD latent defect.   | 186       | 74        |
| 42492 | control failure found in trouble shooting (ref PFR 42493).      | Breakdown in gate oxide of one of the memory transistors. | Most probably a ESD latent defect.   | 143       | 75        |
| 42495 | Missing interrupt and no response to iso-valve (ref PFR 42492). | Breakdown in gate oxide of one of the memory transistors. | Most probably a ESD latent defect.   | 145       | 75        |
| 43283 | Memory array supply voltage out of spec.                        | Short between 10 V & Gnd layer at the positive terminal.  | Failure to correct for laminate shrinkage when terminal holes were drilled causing breakdown of epoxy insulating material under voltage and thermally induced mechanical stress. | 155       | 75        |
| 43588 | Memory array read zero after PWR reapply.                       | Short between 10 V & Gnd layer at the positive terminal.  | Same as 43283 above.   | 32        | 75        |
| 54458 | Memory address failures on the AACs.                            | Solder bridge found was causing contention.               | Expansion of board and/or conformal coat due to CTE effects, shifted entrapped solder particle such that the short occurred,   | 102       | 55        |

Cold Level and Dwell Period: A study of PFR data indicates cold exposure is effective in uncovering design and workmanship PFs in piece parts, electronic circuits and mechanisms,

Table 5 indicates several very significant part problems which were first detected at the unit level. The cold piece part problems documented were arguably the most significant problem to occur on the Galileo Project. See Reference 10 for further details,

Table S - Causes and Mechanisms of Thermal Vacuum Cold Test Failures for

| PF#  | Failure Description                             | Failure Mode  | Failure Physics   | Role of Low Temp.  | Role Of Test Tim   | Time (hrs)   | Te (%) |
|------|---|---|---|--|--|--------------|--------|
| 400  | LGA-2 actuator ran too slow                     | Actuator ran too slow.  | Viscosity of grease inversely proportional to temperature   | Increased viscosity of grease to point where actuator was to slow  | None   | 62.4         | -6     |
| 4248 | ACE MEM/DMA Memory failure                      | Gate oxide Breakdown  | Hot Electrons ( Note activation energy for this phenomenon is negative. )   | Current stress is inversely proportional to temperature. As the current stress increases the rate of gate oxide breakdown increases.   | Failure rate is time dependent. Therefore, cold dwell appropriate for screening these failure modes.   | 7            | -1     |
| 4249 | Star scanned MEM/DMA had address failures       | Gate oxide Breakdown  | Hot Electrons ( Note activation energy for this phenomenon is negative. )   | Current stress is inversely proportional to temperature. As the current stress increases the rate of gate oxide breakdown increases.   | Failure rate is time dependent. therefore, cold dwell appropriate for screening these failure modes,   | 58           | -20    |
| 2599 | Star scanned output word count errors           | Failure of signal lead  | Unknown, but suspect thermally induced strain.  | Unknown, but suspect thermal strain associated with cold level   | None suspected.  | 11.5         | -27    |
| 4191 | NIMS OAOAL VLDVT spectral measurement shift     | LVDT sensitivity below Specification.   | LVDT circuit sensitivity is a function of its natural frequency which in turn is a function of temperature  | LVDT circuit sensitivity is proportional to temperature.   | Not known, but assumed to be time dependent  | 26.5         | -10    |
| 1565 | Unshade cover failed to deploy after pyro. ring | Excessive cover preload + lubricator failure  | lubrication scrubbed off during vib test, resulting in failure in thermal/vac   | None associated with the failure that occurred,  | None   | 17           | 115    |
| 985  | IC design Disturb Problem in TCC244's           | IC design flaw & "Charge Pumping"   | low decoder transistor reach full turn on at low temperatures and high voltages   | Transistor turn-on time is shorter at cold thereby allowing charge pumping to take place.  | None. However, this pattern sensitivity PF requires a significant number of pseudo-random data attempts to be tried in order to have a reasonable probability of detecting an error. | 0            | 20     |
| 1596 | Read Disturb Failure in 1S6504 Device           | Unable to discharge the column line to "0" due to a poor contact between wcn metalization & Vss | The electrical resistance of contact degraded due to electro-migration While the alternative current discharge path is inversely proportional to temperature. | Electro-migration is accelerated by the higher current stresses associated with cold operation AND the leakage current increases as conductance increases with a decrease temperature. | degradation of the intact via electro-migration time sensitive cold  | initial test | 0C     |

Effectiveness of Time Rate-Of-Change of Temperature (dT/dt): Historically, the rate of change during the thermal/vacuum test has been tied to the maximum rate expected in flight. This approach was taken because it has been demonstrated that some types of hardware are sensitive to high rates of change in temperature. A good example of this type of hardware are solar panels. Hardware which is subjected to high rates of change in temperature during flight typically undergo some form of life/qualification testing to verify their flight worthiness. This type of testing tends to be costly. The selection of a temperature ramp rate to be used during a thermal test balances the cost savings (test time) versus the possibility of inducing unwanted failures by using too severe a ramp rate. The typical thermal test of electronic assemblies involves a single thermal cycle and therefore any potential cost saving would be insignificant. In light of this the typical rate specified for testing of bus electronics assemblies has been three times the maximum flight rate. In many cases this works out to be 30°C/hr.

Relative Effectiveness Of Thermal Cycles: Thermal cycle data collected for various electronic and electro/mechanical components shows a large number of failures on the first thermal cycle relative to the second and subsequent cycles. This appears to apply universally to electronic and electro-mechanical assemblies that are thermally cycled. Furthermore, there is little improvement beyond the second cycle in the number of failures detected. The best fit curve (of cycles 2 and beyond) shows that improvement is occurring, but at a slow rate. Upon analysis, the failure distribution appears to be bi-modal. The failures found after the first cycle appear to belong to a different group of failures than those seen in the first cycle. This is particularly evident when curve fits are made on the data. The majority of the temperature-change failures (ones which need exposure to a thermal cycle) are found in the first cycle, leading to the conclusion that subsequent cycles add little to further detection of these defects. The failure population for cycles 2 and beyond seems to be composed primarily of positive activation energy Arrhenius-Reaction-Rate type failure mechanisms. The cycling does not add significantly to the effectiveness of the test for this type of failure mechanism, (See Reference 11 for more details.)

### **3.0 Tradeoffs**

Tradeoffs can be made with each parameter involved in the thermal test: temperature levels, duration, test pressure, number of cycles, temperature ramp rates, and electrical testing. As discussed above, these parameters all impact the effectiveness of the test to varying degrees. Time in test can be traded for bench top operation, high levels can be traded for operating time, atmospheric pressure can be traded for vacuum, etc. These tradeoffs are best made with a solid understanding of test effectiveness and how it is impacted by various parameters.

### **3.1 Sensitivities**

In establishing thermal test requirements for assemblies, the parameters that can be varied are: temperature level, dwell times, pressure, electrical testing, number of cycles, and temperature ramp rate. Table 6 attempts to show the impact of changes in these parameters to: 1) the effectiveness in mitigating the failure mechanisms discussed above; and 2) the cost of the unit.

**Table 6 - Control Parameter Sensitivity**

| Test Parameter  |                | Arrhenius Reaction FMs |            | Hysteresis/Thermal Stress FMs |                 | cost Sensitivity |
|-----------------|----------------|------------------------|------------|-------------------------------|-----------------|------------------|
|                 |                | Pos Ea (1)             | Neg Ea (1) | Low cycle Fatigue             | Parameter Drift |                  |
| Temp. Level     | Hot            | ++                     |            | +                             | -               | o (5)            |
|                 | Cold           |                        | ++         | -                             | +               | o (5) :          |
| Dwell Time      | Hot            | +                      |            | +                             | -               | ++               |
|                 | Cold           | -                      | ++         |                               | +               | ++               |
| Pressure        | Vacuum         | ++                     | -          | +                             | +               | +                |
|                 | Atm.           |                        | ++ (2)     | -(2)                          | ?               | o                |
| Electrical Test | Voltage Margin | ++                     | ++         | +(2)                          | +               | (6)              |
|                 | Freq. Margin   | ++                     | ++         | +                             | +               | (6) :            |
|                 | Power Cycles   | ?                      | ?          | +                             | +               | (6)              |
| Ramp Rate       |                | o                      | o          | -/?                           | +/?             | o                |
| No. Of Cycles   |                | o                      | o          | +(3)                          | +(4)            | ++ (7)           |

(Effect of increasing parameter value: + increases effectiveness/cost, - decreases effectiveness/cost, O no effect)

Notes:

- 1) Ea: Activation Energy
- 2) Effect of the addition of a gaseous medium cold biases the temperature of the test article. Could result in reaching cold levels where specific failure mechanisms change.
- 3) Also consumes flight life.
- 4) However, only up to the point where change stops. Also consumes flight life.
- 5) Temperature level is not a cost drive unless it forces exceptional design considerations.
- 6) Small increase in cost related to test equipment, generally not great at the unit level.
- 7) Increases cost by increasing test time,

#### 4.) References

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## **9. Electronics Parts Destructive Physical Analysis**

### **1.0 Objectives**

The objective of destructive physical analysis (DPA) is to screen out parts with obvious defects and identify latent defects that could produce part (mission) failure at some later time. Most DPAs are performed on active devices, including diodes, transistors, micro circuits (integrated circuits), gate arrays and hybrids. On occasion, for special requirements, passive devices are also subjected to DPA.

### **2.0 Typical Requirements**

The database of the Cassini electronic parts acquisition was used for this study, since the Parts Program Requirements Document PD 699.212 called for 100% DPA on all part lots (a total of 756) other than capacitors and resistors. The faster, better, cheaper missions such as the New Millennium require a review of what is an effective screen and what could be eliminated to meet the new requirements.

### **2.1 Rationale**

A series of procedures to assess the acceptability of electronic parts for space flight use has evolved over a period of several decades. In the context of the Faster, Better, Cheaper mandate from our customer (NASA), these procedures are now being evaluated in terms of their effectiveness in providing mission threatening defect detection. Each of the procedures itemized in this report utilizes project time and money. This evaluation of their effectiveness is possible due to the availability of an extensive database on electronic parts acquisition, resident in the Electronic Parts Engineering Office. The goal is to provide project planners/designers with pragmatic guidelines to help determine what parts requirements can be modified or eliminated to save time and money and what risk (if any), is thereby incurred.

#### **2.1.1 Relevant Failure Modes**

The major relevant failure modes are listed below:

1. Visually apparent external non conformance
2. Radiographic detection of foreign material in the package
3. Corrosive gasses inside the cavity
4. Hermetic seal leaks
5. Scanning electron microscope (SEM) detected fabrication flaws
6. Wire bond pull force specification failure
7. Die Bond shear force specification failure (attachment)

#### **2.1.2 Supporting Data**

The following is a summary of the detailed data in Table 1 of the Appendix:

1. For the Cassini electronic parts acquisition program 786 DPAs were performed. There were a total of 61 lots that failed one or more of the DPA tests which represents approximately 8%.
2. Of the 61 failed lots, 32 were subjected to further analysis/tests and used as a result of MRB approval.
3. Five lots exhibited defects which resulted in being returned to the vendor. Ten lots were down graded to non flight status.

4. The use of DPA to determine suitability of a potential part for the Cassini mission resulted in eliminating five part types early, thereby saving possible redesign time and cost of unusable inventory.
5. As a result of the DPA process for Cassini, approximately 3% of the lots so tested were not used for flight.

## 2.2 Methods

The following test methods are documented in the appropriate MILSTDs such as 883D. The specific set of tests is dictated by the part type and the package type. For example if there is no cavity, the hermeticity test is not used.

1. External Visual Examination (EV)
2. Radiographic Analysis (RE)
3. Residual Gas Analysis (RGA)
4. Hermeticity Testing (HERM)
  - a) Pine Leak
  - b) Gross Leak
5. Internal Visual Examination
  - a) Low Power (LPIV)
  - b) High power (HPIV)
6. Scanning Electron Microscope (SEM) Examination
7. Wire Bond Pull Test (WBT)
8. Die Shear (attachment) Test (DST)

## 3.0 Tradeoffs

For a mission such as Cassini, the full DPA procedure was required. Current costs for a DPA range from \$500 to \$800 each. When the spacecraft at risk costs \$1.2 billion, the DPA cost is cheap insurance against electronic part failure. For the faster, better, cheaper missions, there are several ways the time and cost of performing DPAs could be tailored. The trend toward small assemblies with fewer parts (ICs having increasing circuit function density), the use of commercial grade parts and emerging technology along with limited project funding will bring pressure to reduce costs and maximize probability for success. "The database cited here was the result of testing grade 1 parts which were to meet MIL SPEC Class S or the Source Control Drawing (SCD) equivalent. Most of the failed DPAs were on lots where the manufacturer was required to test for the failed parameter. Referring to Table 1 in the Appendix, this study suggests that:

1. Hermeticity testing was ineffective and is a candidate for elimination. The lots that failed this test were analyzed and used, indicating the specification did not reflect the application.
2. Die attachment yields little value (2 out of 786 lots).
3. Residual Gas Analysis (RGA) failures were uniformly determined to be usable for Cassini. RGA is a good candidate for elimination from the DPA procedure.
4. Wire bond testing only found 2 lots that were deemed un flight worthy out of 786 DPAs.

These four steps, combining time and charges account for over half the cost of a typical DPA. A new project may examine the results presented here and decide whether or not a shortened (tailored) DPA is appropriate, thereby reducing time and cost in the electronic parts acquisition process. Part classes of lesser grade down to commercial (depending on several variables) will probably produce significantly different statistics than those in this study. Studies on parts of lesser grade are in process from several aspects and will result in up dated reports as the data becomes available. It is essential for each new mission/instrument to carefully assess the parts requirements, balancing, schedule, cost and the mission parameters. Early formation of a design team consisting

of the designer, parts specialist(s) and a procurement specialist will maximize electronic parts acquisition.

The use of lower grade or commercial off the shelf (COTS) electronic parts intuitively suggests DPA be required on all lots of active electronic parts, since as this study shows, even lots that have had full up S level screening still fail DPA at a 3% rate.

The faster, better, cheaper missions such as the New Millennium, require a review of what is an effective screen and what could be changed (if anything) to meet the new requirements. Several traditional steps in the DPA process might be eliminated for COTS. Plastic encapsulated parts will not use hermeticity, RGA, bond pull, or die shear testing. The study for this RTOP has shown that these four test were not very effective, even on parts with packages that have cavities.

### 3.1 Effectiveness Versus Failure Modes

Of all the failures noted, 3% were determined to be unsuitable (high risk) for flight use. This means that their use was judged to be potential cause for mission failure. For a mission of the Cassini type, the cost of retrofitting could be significant in terms of both time and money. The DPA expenditure in this case is considered inexpensive insurance. The DPA findings also identified problems with 32 lots that were subjected to additional analysis and testing to provide confidence that they meet the Cassini reliability requirements. The use of DPA early in the acquisition process resulted in the rejection of five part types that had been considered as candidates for Cassini. This step saved considerable time and cost by preventing design time as well as procurement of parts that ultimately would not have been acceptable for this mission.

### 3.2 Sensitivities

The sensitivity of mission failure to each DPA test mode is somewhat complex and dependent on a number of variables. Each mission duration, operating environment and launch mode will determine the specific sensitivities to failure modes detected with I<sup>2</sup> I<sup>2</sup> As. The standard DPA covers eight relevant failure modes as shown in paragraph 2.1.1 of this document. Table II reflects the results on the Cassini project lot acceptance for use. It should be revised as PFRs are received and analyzed.

Table 11. Control Parameter Sensitivity and Cost Sensitivity

| Requirement          | Control Parameters                 | FAILURE MODE  | Sensitivity to Defect Detection |   |   |   |    |    |    |    |    |    |    |   |    |    |    | Cost |    |   |   |
|----------------------|------------------------------------|---|---------------------------------|---|---|---|----|----|----|----|----|----|----|---|----|----|----|------|----|---|---|
|                      |                                    |   | P                               | L | S | M | FM | HE | FL | GL | BW | DD | MF | V | DT | BP | BD |      | DB |   |   |
| DPA                  | External Visual Exam (EVE)         | Package (P) Leads (L) Seals (S) Marking (M)             | +                               | + | + | + | -  | -  | -  | -  | -  | -  | -  | - | -  | -  | -  | -    | -  | + |   |
|                      | X-Ray Examination (RE)             | Foreign Material (FM)                                   | 0                               | + | 0 | 0 | +  | 0  | 0  | 0  | +  | +  | 0  | 0 | 0  | 0  | 0  | 0    | 0  | + | + |
|                      | Residual Gas Analysis (RGA)        | H2O Excessive (HE)                                      | +                               | 0 | + | 0 | +  | +  | -  | -  | 0  | 0  | 0  | 0 | 0  | 0  | 0  | 0    | 0  | 0 | + |
|                      | Hermeticity (HERM)                 | Fine Leak (FL) Gross Leak (GL)                          | +                               | 0 | + | 0 | 0  | 0  | +  | +  | 0  | 0  | 0  | 0 | 0  | 0  | 0  | 0    | 0  | 0 | + |
|                      | Internal Visual Exam               |   |                                 |   |   |   |    |    |    |    |    |    |    |   |    |    |    |      |    |   | + |
|                      | Low Power (LPIV)                   | Bond Wire (BW) Die Defect (DD) Foreign Material (FM)    | 0                               | + | + | + | +  | 0  | 0  | 0  | +  | +  | -  | - | -  | 0  | 0  | 0    | 0  | 0 | + |
|                      | High Power (HPIV)                  | Metallization Flaws (MF) Voids (V) Dielectric Thin (DT) | 0                               | + | + | 0 | +  | 0  | 0  | 0  | +  | +  | -  | - | -  | 0  | 0  | 0    | 0  | 0 | + |
|                      | Scanning Electron Microscope (SEM) | Metallization Flaws (MF) Voids (V) Die Defect (DD)      | 0                               | + | + | 0 | +  | 0  | 0  | 0  | +  | +  | +  | + | +  | +  | +  | +    | +  | + | + |
|                      | Wire Bond Testing (WBT)            | Bond Pull (BP) Bond Defect (BD)                         | 0                               | 0 | 0 | 0 | 0  | 0  | 0  | 0  | 0  | +  | 0  | 0 | 0  | 0  | 0  | +    | +  | 0 | + |
| Die Shear Test (DST) | Defective Bond (DB)                | 0   | 0                               | 0 | 0 | 0 | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0  | 0  | 0  | 0    | 0  | + | + |

## 4.0 Appendix

Table I. Detailed Supporting Data

| LOG #    | PART #          | D | TRACE # | TEST | FAILURE(A101)1.                     | MRBD IMPOSITION                              |
|----------|-----------------|---|---------|------|-------------------------------------|--|
| 5615*    | 2N2946          | Q | 2IX85   | WBT  | WIRE BOND PULL TEST                 | UAI MARGINAL BOND PULL FAILURE               |
| 5856     | XR2207          | U | 3II 10  | WBT  | WIRE BONO 1 ALL TOO LONG            | NON FLIGHT ONLY                              |
| 5984     | 9X008           | U | 3II05   | WBT  | BOND WIRES ON DIE                   | NON FLIGHT ONLY-DIE SURFACE IS PASSIVATED    |
| 6F92     | 26C32           | U | 3E134   | SEM  | METALLIZATION VOIDS                 | UAI SPECIAL LIFE TEST SHOWS LOT OK           |
| 5601     | FR19130         | Q | 4A124   | SEM  | METALLIZATION                       | UAI MINOR DEFECT                             |
| 5950     | 5411CS02        | U | 1GG86   | SEM  | METALLIZATION BRIDGE                | UAI GATE ARRAY TECH - DEFECT IN UNUSED AREA  |
| 6013     | 2N2907A         | Q | 4E035   | SEM  | METAL LINES <30%                    | UAI CURRENT DENSITY CALC. OK FOR RPWS ONLY   |
| 5988*    | 26C32           | U | 2H225   | SEM  | METALLIZATION VOIDS                 | UAI CURRENT DENSITY CALC. OK FOR APPLICATION |
| 6167     | 7533            | U | 3L030   | SEM  | METALLIZATION VOIDS                 | UAI CURRENT DENSITY CALC. OK FOR APPLICATION |
| 4414     | 2N2905A         | Q | 1GF64   | SEM  | SMALL METALLIZATION CRACKS          | UAI CURRENT DENSITY CALC. OK                 |
| 5873     | >N5116          | Q | 2J027   | SEM  | METALLIZATION LESS THAN 50%         | UAI CURRENT DENSITY CALC. OK                 |
| 5442     | IRHF7230        | Q | 1H047   | SEM  | SMALL METALLIZATION CRACKS          | UAI CURRENT DENSITY CALC. OK                 |
| 5613     | AD5855          | U | 3I099   | SEM  | SURFACE ANOMOLIES                   | UAI ANALYSIS SHOWS LOW RISK                  |
| 6088     | SPD5822         | o | 3G290   | SEM  | DIE CHIPPED-RANDOM ANOMALY          | UAI 5 MORE DPAs - ALL OK                     |
| 591x     | 2N2222A         | Q | 2H055   | SEM  | METAL THINNING TO < 50%             | RTV  |
| 5979     | 54HCS160        | u | 2E044   | SEM  | VOIDS IN THE METALLIZATION          | RTV  |
| 5990*    | 54HCSKMSR       | U | 4F260   | SEM  | CONTAMINATION                       | RTV  |
| 6102     | 54HCS14KMSR     | U | 5H143   | SEM  | METALLIZATION DEFECTS               | RTV  |
| 6377*    | 6617            | U | 2L016   | SEM  | METAL THINNING TO < 50%             | PENDING \$1 OR FURTHER ANALYSIS              |
| 6210     | CWR09           | c | 1A105   | SEM  | DIELECTRIC VOIDS                    | NON FLIGHT ONLY                              |
| 5893     | IN4569A         | o | 4C211   | SEM  | RADIAL CRACKS IN GLASS BODY         | NON FLIGHT ONLY                              |
| 6272     | 2N2990          | Q | 4K021   | SEM  | OIL CONTAMINATION                   | NON FLIGHT ONLY                              |
| 6612     | 54HCS02KMSR     | U | 4C315   | SEM  | METALLIZATION VOIDS > 50%           | NON FLIGHT ONLY                              |
| 6177     | HS1840          | u | 1C114   | SEM  | METAL THINNING TO < 30%             | NON FLIGHT ONLY                              |
| 5573     | 54HCS14KMSR     | U | 4K050   | SEM  | METALLIZATION DEFECTS               | NON FLIGHT ONLY                              |
| DPA LABS | IN4569A         | D | 4C211   | SEM  | CRACKS IN LEAD SIALS                | FOR QC TESTING ONLY IN UP-SCREEN             |
| 5652     | DXN688          | o | 1J090   | RGA  | WATER CONTENT TOO HIGH              | UAI 1.11 TEST PARTS OK                       |
| 5061     | D1777A          | D | 1J089   | RGA  | H2O EXCESSIVE                       | UAI ACCELERATED LIFE TEST OK                 |
| 5409     | 2N3501          | Q | 1GF68   | RGA  | H2O EXCESSIVE                       | UAI TESTED 4 MORE. ALL OK                    |
| 5761     | 2N6137          | Q | 2C056   | RGA  | H2O EXCESSIVE                       | UAI ANALYSIS SHOWS NO RELIABILITY RISK       |
| 5925     | 10525           | U | 3F208   | RGA  | H2O EXCESSIVE                       | UAI ANALYSIS SHOWS LOW RISK                  |
| 6138     | 1852            | X | 2J018   | RCA  | H2O EXCESSIVE AND BOND PULL         | UAI ANALYSIS SHOWS RGA OK - BOND PULL OK     |
| 5616     | IN49            | B | 3H039   | RF   | X-RAY- FOREIGN MATERIAL (BOND WIRE) | UAI ENTIRE LOT X-RAYED - PASSED              |
| 5472     | 1526B           | U | 1C032   | RF   | X-RAY                               | NON FLIGHT ONLY                              |
| 5903     | IN49            | B | 3H093   | LPV  | LOOSE WIRE INSIDE                   | UAI 4 MORE PARTS DPA - ALL OK                |
| 6106     | 2N3375          | Q | 3IX076  | LPIV | BOND WIRE ON DIE SURFACE            | UAI SCREENING DATA OK - AREA PASSIVATED      |
| 6190     | MA31750         | U | 2K070   | LPIV | VISUAL INTERNAL                     | UAI CURRENT DENSITY CALC. OK FOR APPLICATION |
| 5986     | HR1060          | u | 2G032   | LPIV | BOND WIRE SPACING TOO CLOSE         | UAI 1 PART REJECTED - REST OF LOT OK         |
| 5783     | 1047B           | U | N1964   | HPIV | VISUAL INTERNAL                     | UP SCREENED AND USED                         |
| 5790     | 54HCS08         | U | 3H423   | HPIV | METALLIZATION VOIDS                 | UAI REDUCED CURRENT OK IN APPLICATION        |
| 5993     | IN 647          | D | 4B016   | HPIV | VISUAL INTERNAL                     | UAI LEAD PULL TEST ALL OK                    |
| 6617     | 54HCS02         | U | 4C315   | HPIV | METAL THINNING TO < 50%             | RTV  |
| 6282     | M39010V03A102KR | L | 9528    | HPIV | WIRE WOUND TOO TIGHT                | PENDING                                      |
| 6166     | 05041C3321A19   | c | 9331    | HPIV | CHIP CAP - COVER PLATE THIN         | NOT USED                                     |
| 6210     | 500S43B224      | c | 9332    | HPIV | CHIP CAP - DIELECTRIC VOIDS         | NOT USED                                     |
| 661R     | 9G1103          | Q | 2A072   | HERM | FINE LEAK 1 LST, WIRE BONO SUSPECT  | UAI RGA OK FOR LARGE CAN - BOND PULL OK      |
| 6619     | 2N2880          | Q | 1H036   | HERM | FINE LEAK TEST THREE TIMES          | UAI PASSED RGA - MRB REVIEW APPROVED USE     |
| 5513     | STD3303         | Q | 1H037   | HERM | FINE LEAK TEST                      | UAI PASSED RGA - MRB REVIEW APPROVED USE     |
| 5644*    | 2N2219A         | Q | 1GF62   | HERM | GROSS LEAK TEST-ONLY LSPA PART      | UAI ENTIRE LOT PASSED LEAK TESTS             |
| 5567     | RM1101W         | U | 1C027   | HERM | GROSS LEAK TLS1                     | UAI ENTIRE LOT PASSED LEAK TEST              |
| 5568*    | RH1190AH        | U | 1C024   | HERM | FINE LEAK TEST                      | UAI ENTIRE LOT PASSED HERMETICITY            |
| 5494     | IN-1727         | L | 9S24    | HERM | GROSS LEAK                          | PENDING                                      |
| 5498     | IN 1726         | L | 9S24    | HERM | GROSS LEAK                          | PENDING                                      |
| 5782     | 7225            | U | 9325    | HERM | GROSS LEAK                          | NOT USED                                     |

|       |         |   |       |     |                                 |   |
|-------|---------|---|-------|-----|---------------------------------|---|
| 6157  | 1N4569A | D | 4B071 | EVI | L.F. AD SEAL LOOKS DEFECTIVE    | UP SCREENED - 100% VISUAL (ANI) LEAK TEST |
| 5431  | 1852    | X | 2J014 | EVI | GLASS SEALS HAD RADIAL CRACKS   | UAI RADIAL CRACKS IN LEAD SEALS CHECK OK  |
| 5992  | 422K    | K | 3B025 | EVI | LEAD BROKEN                     | UAI EXTENSIVE ANALYSIS CONCLUDED LOW RISK |
| 5997  | III. 24 | B | C1425 | EVI | PACKAGE DAMAGE                  | NOT USED                                  |
| 6001* | CWR11   | C | 1C035 | EVI | PACKAGE CRACKS                  | NON FLIGHT ONL%                           |
| 6139  | 1N4848  | D | 3J131 | EVI | LEAD SEAL LOOKS DEFECTIVE       | 3 PARTS SCRAPPED DUE TO 100% VISUAL       |
| 5879  | 1N6313  | D | 3C002 | DST | POOR DIE BOND                   | NON FLIGHT ONL%                           |
| 5858  | CIL357  | U | 9329  | DST | DIE & CHIP CAP ATTACHMENT FAILS | NOT USED                                  |

**\*Additional detail:**

|      |        |   |       |  |   |
|------|--------|---|-------|--|---|
| 6377 | 1J5855 | U | 3I099 |  | DIE SURFACE WAS IRREGULAR ON TWO PARTS OUT OF THREE ALSO ON ONE VOIDS WERE SEEN IN THE INSULATING OXIDE UNDER A BOND PAD REDUCING THE THICKNESS 100.7 MICRONS. THESE PARTS HAD PASSED A 2000 HOUR LIFE TEST AND THE MRB REVIEW RESULTED IN UAI  |
| 5988 | LR9130 | Q | 4A124 |  | ONE OF TWO PARTS SHOWED DAMAGED METALLIZATION OF 1% TO CORN ACT WINDOWS TWO MORE PARTS FROM THE SAME LOT PASSED DP MRB ACTION WAS TO UAI  |
| 6001 | 22K    | K | 3B025 |  | ONE OF THE LEADS WAS MISSING THIS LEAD TO AN EXTENSIVE ANALYSIS SINCE IN ASSEMBLY AT LORA TWO OTHER LEADS FRACTURED. THE CONCLUSION WAS THAT THE FRACTURES WERE CAUSED BY HYDROGEN EMBRITTLEMENT. THE MRB DECIDED THAT 1 HAD ALL THE LEADS THAT WOULD FRACTURE HAVE ALREADY DONE SO DUE TO LEAD FORMING AND HANDLING NO RETROFIT WAS DONE |
| 5990 | 533    | U | 3L030 |  | SEM EXAM FOUND THE METAL AT THE CORN ACT WINDOW WAS REDUCED TO 35% OF THE ORIGINAL THICKNESS. CURRENT DENSITY CALCULATIONS SHOWED THAT IF METAL WAS ADEQUATE FOR THE APPLICATION MRB ACTION WAS TO UAI  |
| 5644 | 1J103  | Q | 2A072 |  | THE LEAK TEST FAILURE WAS ATTRIBUTED TO A SURFACE NATURE RETISSING SHOWED NO FLAKS. THE BOND PULL FAILURE WAS AT 145 GRAMS FORCE (gf) ANI SHOULD BE 200gf. MRB REQUIRED THREE MORE PARTS TO BE SUBJECTED TO BOND PULL TESTS ALL BONDS PASSED. MRB DISPOSITIONED TO UAI  |
| WP15 | 42946  | Q | 2D085 |  | ONE WIRE BOND OUT OF NINE FAILED THE PULL TEST. IT MEASURED 1.4gf AND SHOULD HAVE BEEN 1.5gf AT A MINIMUM. THE REMAINING EIGHT BONDS PULLED AT 46 gf AS A MINIMUM. MRB ACTION WAS TO UAI  |
| 5568 | D3303  | Q | 1H037 |  | THE FINE LEAK WAS DETERMINED TO BE CAUSED BY SURFACE DEFECTS  |

**Acronyms:**

Log # = JPL FA Lab tracking number

Part # = JPL Generic part number

Trace # = JPL Lot tracking number

Test/Process Performed

WBT = Wire Bond pull Test

SEM = Scanning Electron Microscope Examination

RGA = Residual Gas Analysis of the package cavity

RE = Radiographic Examination (X-Ray)

LPIV = Low Power Internal Visual Examination

HPIV = High Power Internal Visual Examination

Herm = Hermeticity Test

EVI = External Visual Inspection

DST = Die Shear Test (attachment)

MRB = Material Review Board

UAI = Use As Is

## 10. Quality Assurance Site Survey Requirement

### 1.0 objectives

The objective of a Site Survey is to verify that the manufacturer uses standard, good manufacturing, test and handling practices, and is capable of building and delivering the product as specified. Findings likely to significantly impact reliability, cost, or schedule are documented and addressed in the survey.

### 2.0 Typical Requirement

Although vendor certification is required by NASA Handbook 5300.4 (1B) (111500), in general JPL survey findings are generic industry issues which could drive reliability cost or schedule. A survey is generally required every two years when procuring a spacecraft, subsystem, assembly (unit) or complex component from a vendor.

A survey consists of one to five persons visiting a plant from one to five days depending on the complexity of the manufacturing (component to spacecraft levels). A typical survey team consists of 2-3 persons including Quality Assurance (QA), and a packaging, fabrication, electronics or component specialist. A well organized survey team will meet prior to the survey to discuss the product and identify critical processes which should be scrutinized during the survey.

Follow up audit(s) may be required to verify that corrective actions have been properly implemented; these audits are often combined with other business at the vendor.

### 2.1 Rationale

Vendors who are new to military/space applications engineering may not have the personnel, systems and/or equipment in place to build reliable flight hardware.

Vendors who have new management, have moved, or have lost key personnel sometimes "lose the recipe" for building flight hardware. They may have made changes affecting the reliability of flight hardware manufactured in their plant.

Important areas which are covered, if applicable, during a survey include:

1. Contractor's Quality System
2. QA involvement in planning and reviews
3. Electro Static Discharge (ESD) controls
4. Alerts
5. Procurement controls
6. Subcontracted manufacturing/testing Operations
7. Approval, surveillance and auditing of subcontractors
8. Flow down of requirements to subcontractors
9. Non-standard parts approval and processing
10. Materials and parts qualification
11. Workmanship standards
12. Processes or tests new to the contractor
13. Process controls including those for unique processes or testing
14. Configuration management
15. Non-Conforming Material Controls/Material Review Board
16. Material traceability
17. Receiving inspection

18. Manufacturing and test documentation
19. Rework/Repair
20. Statistical process control
21. In-process and Final inspections
22. End Item Data Package review
23. Packaging/Shipping
24. Document/Software change control
25. Self-audit program
26. Cleanliness/clean room controls/environmental controls
27. Test controls
28. Stamp control
29. Metrology controls
30. Training

Surveys can indicate a contractor's weakest processes or systems. This helps focus JPL's efforts to select the contractor, and plan oversight of the contractor's activity. For example, if a contractor had never before performed centrifuge testing, it would be prudent to review their centrifuge procedure in depth and require their QA to monitor or witness the test.

#### 2.1.1 Avoidable **Deficiencies/Failures**

Listed are a few of the avoidable problems which may be identified during a survey:

1. Inadequate testing, products which do not meet the requirements of the contract, and/or hardware failures can result when requirements are not adequately flowed down to subcontractors. Manufacturers sometimes contract out manufacturing or testing without sufficiently handing down customer requirements and maintaining controls over their subcontractors.
2. Hardware failure and/or loss of configuration management can result when engineering changes are not communicated to the manufacturing floor due to inadequate document change control.
3. Poor Electro Static Discharge control procedures can lead to functional or latent failures of hardware. "At JPL, over a two year reporting period ('91 -'92), approximately 30% of all electronic part failures that had failure analysis, performed were attributed to ESD" (Ref. 2). These are only the failures found **after** assembly.
4. New processes may introduce new failure modes. "This will be dealt with during PDR/CDR if one is planned. If not, the survey combined with manufacturing process review (see Process Review Requirement **TBD**) may be able to point out potential problems.
5. Vendors may say and believe that their standard processes meet contract requirements while a closer look may reveal that they do not.
6. Reliability of the hardware can be affected by processes and workmanship which tend to drift over time without recurrent training.

All of these problems, if experienced, are likely to impact cost and schedule.

#### 2.1.2 **Supporting Data**

Table 1 provides a sampling of problems detected during site surveys on JPL programs.

Table 1. JPL Site Surveys - Problems Encountered

| S/C   | Survey Issues   | Corrective Action(s) / Outcomes  | Survey |
|---|---|--|--------|
| Topex<br>Spacecraft<br>Solar Array                  | Contractor subcontracted a major portion of solar array and refused to do source inspection.  | JPL did source inspection at subcontractor. Seven arrays were built before one passed shake test. The subcontractor dropped the flight solar array costing 6 mos. delay & tens of thousands of \$s.                                      | 039    |
| Pathfinder<br>(1986)<br>Spacecraft                  | Approved. Follow up audits to survey revealed that contractor handed off an experiment to a subcontractor who handed it off to another subcontractor with none of the project requirements handed down.   | JPL did source inspection at subcontractor. Unit failed 5 times in environmental test due to machined particles from grinding operation. Several redesigns occurred due to failures.   | 020    |
| NSCAT<br>Crystal<br>Oscillator                      | Loss of key personnel/facilities moved/management change. No operator/inspector training. Weak traveler design. No record of burn-in circuit tests prior to testing flight parts.   | Disapproved but contractor was single source with unique capabilities. JPL became heavily involved - did some of the soldering. Parts ended up working well.   | 125    |
| Cassini<br>Power Sys<br>SSIS hybrid                 | Contractor did not understand element evaluation and upscreening requirements, had never qualified a flight hybrid before, and had never purchased ASICs for use in flight hybrids.   | JPL became heavily involved in this procurement. Parts are presently working well.   | 146    |
| Cassini<br>Waveguide                                | Approved. Post award survey. Previous experience on NSCAT had revealed: Contractor had neither tools nor expertise to measure sophisticated waveguide geometry and stacked tolerances. Parts shipped to JPL, did not meet drawing dimensions. Delays of several months and additional JPL trips to bring equipment and instruct contractor on its use ensued. | Survey recommended contractor purchase appropriate equipment. Contractor purchased measuring equipment. No significant problems experienced to date.   | 282    |
| Cassini<br>Solid State<br>Computer                  | Disconnect between computer assembly facility and parts acquisition group. Limited flow down of parts requirements/change notices/corrective actions/MRB decisions. Loss of key person-no date review of parts. ESD controls not uniformly enforced. Limited QA involvement.  | JPL QA resident heavily involved. Parts were marked on wrong side & assembled marked side down due to disconnect between assembly & parts facilities- loss of serial number level traceability.  | 210    |
| Cassini<br>Printed<br>Wiring<br>Boards              | Conditionally approved. Contractor had moved. Equipment out of calibration, DESS certification had not been renewed since move.   | Corrective actions: Vendor to complete recertification. Equipment to be calibrated. Procedures to be updated.  | 120    |
| All Projects<br>fasteners/<br>rivets/ drills        | Not recommended. Contractor produces mainly commercial grade hardware.  | Contractor not used for JPL flight procurements.   | 206    |
| All Projects<br>locking<br>fasteners                | Conditionally approved. Raw material control is not implemented. Quality Manual does not address raw material traceability.   | Recommendations: Implement raw material control. Quality manual should reflect traceability requirements.  | 259    |
| Cassini<br>Engine<br>Gimbal<br>Actuator<br>Bearings | Conditionally approved. Problem with traceability of raw material to heat number/manufacturer. Possible GIDEP Problem Advisory re: wrong materials used on bearings.  | GIDEP Problem Advisory forwarded to contractor.  | 258    |
| Cassini<br>electronic<br>parts testing              | Conditionally approved. Vendor has only 6 months experience with class "S" flow & QA does not actively follow that flow for their single class "S" customer (customer QA monitors flow).  |  | 132    |
| Cassini A-D<br>Converters/<br>hybrids               | Conditionally approved. Verification of released test software is lax - danger that current version is not in use. Element evaluation and housekeeping issues also cited.   | Frequent JPL QA and engineering trips at added cost. Parts are currently working well.   | 179    |
| Pathfinder<br>DC-DC<br>converter<br>hybrids         | Post-Award Survey. Process controls inadequate. Process logs and tables referenced in process documents were not found on production floor. No cleanliness monitoring. Poor production practices. No evidence of calibration of critical equipment. No document change control for test procedure. ESD controls are weak.                                     | Contract was placed because price was low and schedule tight. Some parts failed electrically due to workmanship. Destructive Physical Analyses (DPAs) failed. Extra JPL trips due to problems. Parts passed qualification & are working. | NR     |
| Cassini<br>electronic<br>parts testing              | Conditionally approved. Non-responsiveness to prior JPL corrective action (CA). Rough handling of parts.  | Corrective actions recommended: Respond to CA. operator orientation/QA surveillance of parts during test. Increase staffing to accommodate workload.   | 105    |
| Cassini<br>TWTA                                     | Conditionally approved. Subsequent weakness in Quality engineering involvement, test coverage and end-item data submittal.  | Significant JPL Quality Engineering involvement - limited improvement in supplier QA role.   | 292    |
| Galileo<br>AACS                                     | ESD controls/procedure lacking. Contractor insensitive to easily damaged (at 30 volts) integrated circuits.   | JPL negotiated stringent ESD procedure. JPL QA resident required to monitor ESD practices. Supplier improved - few problems on Magellan and Cassini.   | NA     |
| Galileo<br>Power Sys<br>Relays                      | Post-award survey disclosed material / configuration / process controls not well planned nor documented.  | Significant JPL QA resident role. Delayed production of material and process problems surfaced. Eventually resolved - few problems on subsequent Cassini procurement.  | NA     |

Survey = Quality Assurance Survey number NK= Informal survey - not released NA= Survey not available

### 3.0 Tradeoffs

The survey tradeoff considers the cost of performing the survey and following up on corrective actions versus a reduction in expected failures, cost and schedule overruns due to poor quality hardware.

Pre-Award Surveys have the greatest potential for cost and schedule savings in that JPL has timely opportunity to negotiate corrections or take an alternate approach to the procurement, Cost savings can also be expected when a better vendor is selected.

Pre-Award Surveys for fixed price contracts offer opportunities to contain cost within the contract and identify hidden costs of JPL contract oversight.

### 4.0 References

1. NHB 5300.4(1 B), "Quality Program Provisions for Aeronautical and Space System Contractors", NASA Handbook, April, 1969.
2. Olsen, "Electrostatic Discharge (ESD) Control Program Requirement", April, 1996.
3. QAP 39.3 Rev.D, "Survey of Quality Assurance Systems and Facilities Flight Systems Contractors", JPL Quality Assurance Procedure, July, 1992.
4. QAP 41.20, "Survey of Flight Electronic Microcircuit Parts Suppliers", JPL Quality Assurance Procedure.
5. QAP 41.21, "Survey of Flight Electronic Part Screening Contractors", JPL Quality Assurance Procedure.
6. QAP 41.22, "Survey of Flight Microelectronic Hybrid Manufacturers", JPL Quality Assurance Procedure.
7. QAP 41.23, "Survey of Flight Electromagnetic Suppliers", JPL Quality Assurance Procedure.
8. QAP 41.24, "Survey of Flight Semiconductor and Discrete IC Part Suppliers", JPL Quality Assurance Procedure.

# J 1. Electrostatic Discharge Control Program Requirement

## 1.0 Objective

Electrostatic discharge (ESD) control requirements are used to protect electronic parts and systems against damage or degradation from ESD during routine handling, fabrication, testing and use. The objective of an ESD control requirement is to ensure that electronic systems operate as intended during development, launch and mission operations.

## 2.0 Typical Requirement

Proactive measures exist to protect ESD-sensitive (ESDS) parts and systems against the devastating effects of ESD. Several military and industry ESD control standards exist. JPL's ESD control program is defined in JPL D-1348, JPL Standard for ESD Control. In summary, this program contains requirements including:

1. Personnel ESD awareness and control training
2. Personnel grounding techniques
3. ESD-safe workstations and laboratories
4. ESD-safe packaging
5. ESD control facility audits
6. ESD-safe handling procedures
7. ESD-protective clothing
8. Control of relative humidity levels

## 2.1 Rationale

The rationale for an ESD control program is based on the fact that ESD can severely damage or degrade electronic parts and systems. Industry estimates are that ESD accounts for losses over \$1 billion in the US each year. At JPL, over a two year reporting period ('91 - '92), approximately 30% of all electronic part failures that had failure analysis performed were attributed to ESD.

ESD-sensitive electronic parts include discrete devices such as diodes, transistors, thin film resistors, charge coupled devices, surface acoustic wave devices, optoelectronic devices, hybrid integrated circuits, silicon controlled rectifiers, oscillators, microwave solid state devices, and integrated circuits. Integrated circuits are particularly vulnerable to ESD because of the small size of the constituent elements and their low thermal mass and low breakdown voltage. ESD will continue to be a problem affecting electronic parts. Semiconductor technological advancements are making parts smaller, faster, more complex, and requiring less power. As a result, electronic parts are becoming more susceptible to ESD.

By definition, ESD is the sudden transfer of electrical charge between two objects at different electrical charge potentials. Electrical charge, sometimes called static electricity, is a natural phenomena that occurs from routine handling, fabrication, testing and use of electronic systems. One technique to generate static charge, the triboelectric method, occurs when two dissimilar materials contact and separate. The contact-separation process creates either an excess or deficiency of electrons on both objects. Since electrons exhibit a negative electrical charge, an object with an excess of electrons is said to be negatively charged. Likewise, an object with a deficiency of electrons is said to be positively charged.

One example of the contact-separation charging phenomena occurs when a person wearing shoes walks across carpet. The contact and separation between the carpet and the shoe sole causes charge separation within both surfaces. Opposite free charges within the persons' skin layer are

attracted to the charges at the sole-skin interface. The result is a charge imbalance on the surface of their body. If the person contacted a conductive object such as a doorknob, free charges within the doorknob and the person would suddenly move. This sudden movement of charges is an ESD event .

Studies have shown that **tribocharging** of the human body in the manner described above can generate voltages in the 20,000V range. This voltage., if allowed to contact an ESD-sensitive electronic part or system could cause devastating internal damage. One method that is commonly used to reduce human body charges to safe levels is to electrical y ground the person. Personnel grounding is routinely accomplished using a wrist strap, which allows neutralization of the body surface charges.

Charge can also be generated inductively. Inductive charging differs from triboelectric charging since charge transfer occurs without physical contact. Inductive charging results when one object is placed within the invisible electric field of an electrically charged object. The charged object exerts a force on the object placed within its field, creating charge separation within the object. If the object were conductive and grounded while within the field, a net charge of opposite polarity would be transferred. An example of inductive charging occurs when an electronic part is placed near an electrically charged object such as an insulator that has been tribocharged. Internal part damage may be induced depending upon the strength of the electric field. Techniques have been developed to protect ESD-sensitive (ESDS) items from electric fields. One example is the use of enclosing ESDS parts within metallized barrier bags which blocks the force and charging effect of the electric field.

If not controlled, ESD will induce damage within ESDS parts and systems. This damage may lead to either catastrophic failures (the part doesn't work) , parametric failures (the part works, but not correctly), or it may remain latent (hidden) only to fail at some time in the future.

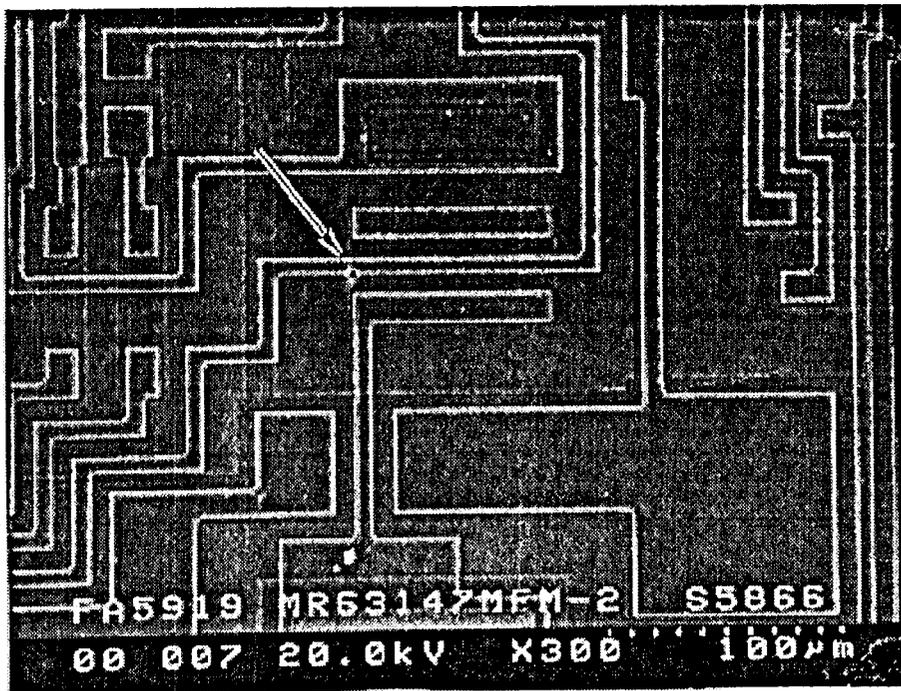
isolation and replacement of catastrophic and parametric failures is usually possible, since they are often revealed during product development stages. Replacement of latent failed parts may be possible depending upon the type of product, However, replacement of a latent failed part on the majority of JPL products is currently impossible, since these products are spacecraft. A latent part failure on a launched spacecraft could lead to reduction of mission objectives or possible loss of mission. Thus, the prime rationale for an ESD control program requirement is to safely protect ESD-sensitive parts and equipment against catastrophic, parametric and most importantly, latent part failures.

### 2.1.1 Failure Modes

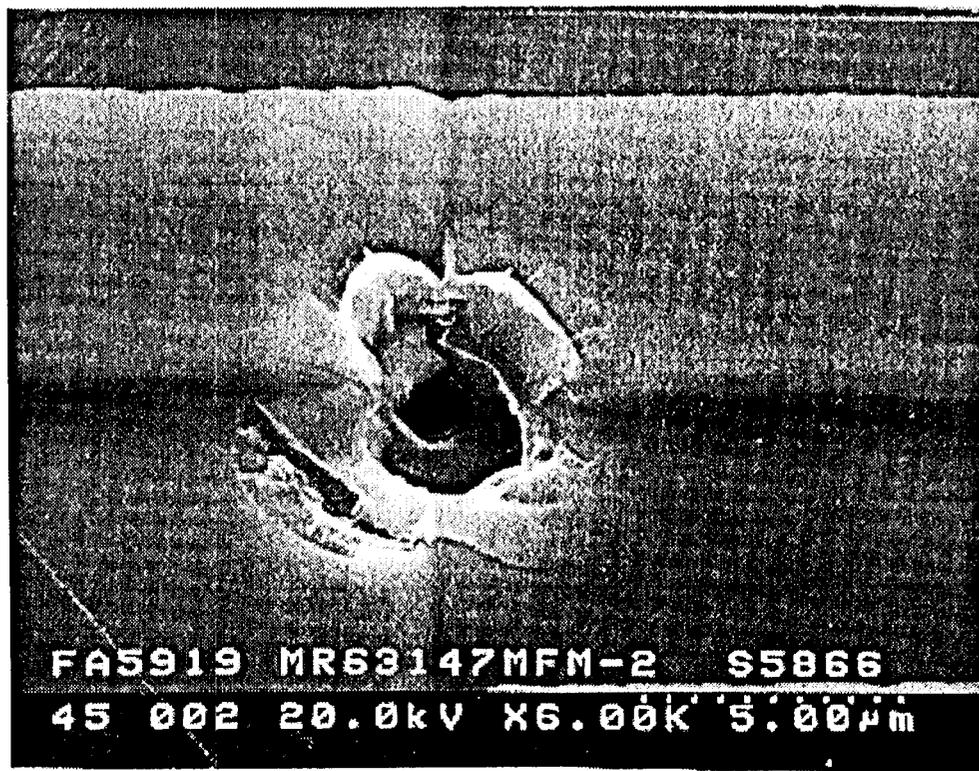
Common ESD-induced failure modes are listed below. These modes are indicative of internal damage sufficient to cause either catastrophic or parametric failures. Latent damage is difficult, if not impossible to detect,

1. Open circuits.
2. Hard short circuits.
3. Resistive short circuits.
4. Leaky input/output current.
5. intermittent operation.
6. Unstable operation.
7. Functional failure.
8. Out of spec failure.

Figures 1 and 2 show examples of ESD-induced damage within an integrated circuit.



**Figure 1.** Scanning electron micrograph (x300) showing internal circuitry within an integrated circuit, Arrow denotes ESD-damaged location.



**Figure 2.** Scanning electron micrograph (x6000) showing close-up of ESD damage denoted by arrow in Figure 1.

### 2.1.2 Supporting Data

The JPL PFR database was searched for failures attributed to ESD. A partial list of ESD-induced failures are shown in Table 1.

| S/C             | PFR # | Environment | Description   | Failure Mode                                   |
|-----------------|-------|-------------|---|--|
| Voyager         | 39620 | Ambient     | control logic #203 current high, bad IC U54               | ESD damaged CMOS IC                            |
| Galileo         | 44101 | Ambient     | CCD image sensor g100 no response to light                | ESD short caused by ESD.                       |
| Mars Pathfinder | D0850 | Ambient     | When turning system on, the CCD did not deliver an image. | ESD damaged CCD                                |
| Ulysses         | 3648  | Ambient     | Phase multiplexer switch module inoperative               | CMOS switch shorted due to ESD.                |
| WFFC 11         | 53937 | Ambient     | CCD failed to image properly.                             | ESD damage causing short in output gate region |
| Cassini         | D0436 | Ambient     | Gates of GaAs FETs were shorted                           | ESD damage                                     |

### 3.0 Tradeoffs

The ESD control program tradeoff considers the cost of implementing the program versus the cost of incurring ground based (catastrophic and parametric) and flight (latent) failures. Ground based failures result in increased costs for troubleshooting, part isolation, part removal, and schedule slips. Relating a cost to latent failures is dependent upon the amount of mission objective lost and the monetary value of lost spacecraft science data.

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