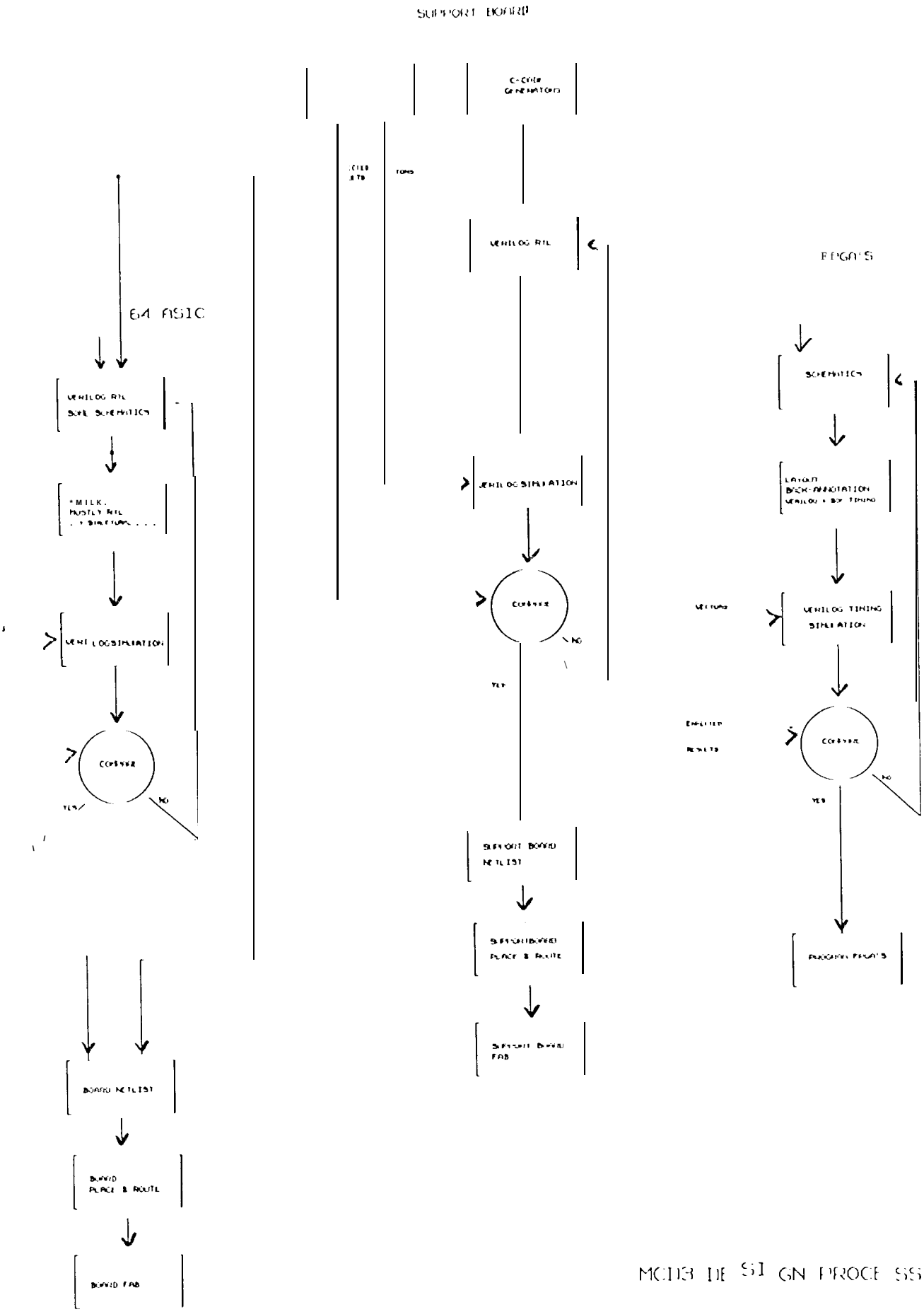
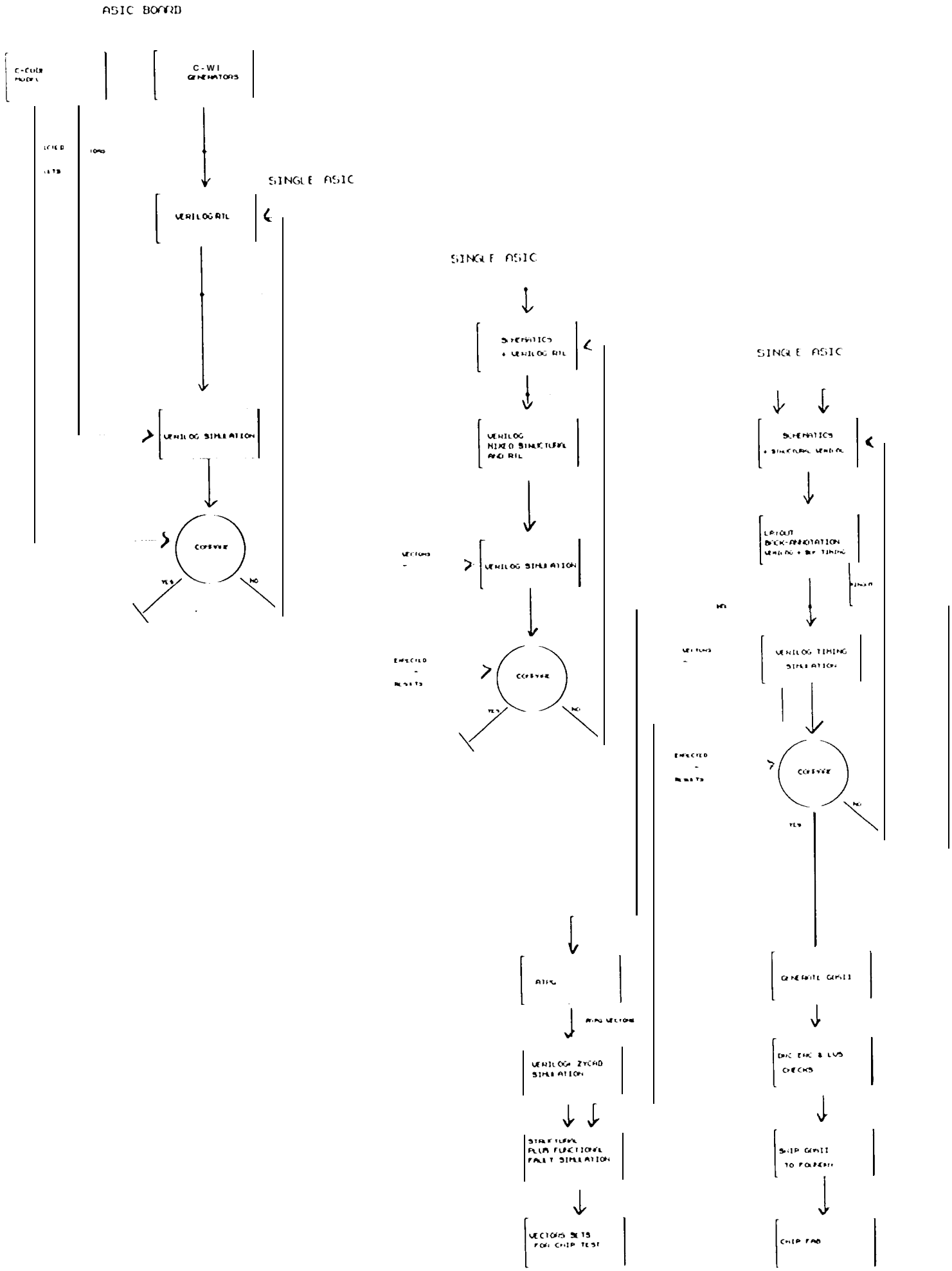
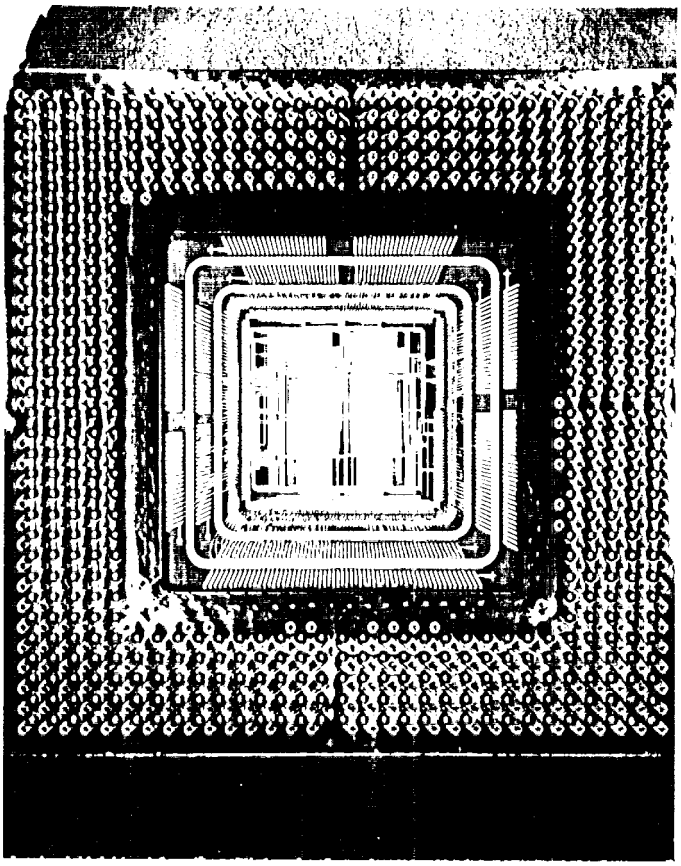

SUPPORT BOARD
C-CODE GENERATORS
VERILOG RTL
FPGA'S
64 ASIC
VERILOG RTL
SCHEMATICS
VERILOG SIMULATION
SCHEMATICS
LAYOUT
VERILOG TIMING
SIMULATION
CORNER
NO
YES
SUPPORT BOARD
NETLIST
BOARD NETLIST
BOARD
PLACE & ROUTE
BOARD FAB
MCM3 DESIGN PROCESS


ASIC BOARD
C-CODE MODEL
C-WI GENERATORS
SINGLE ASIC
VERILOG RTL
VERILOG SIMULATION
COMPARE
YES
NO
SINGLE ASIC
SCHEMATICS + VERILOG RTL
VERILOG MIXED STRUCTURAL AND RTL
VERILOG SIMULATION
COMPARE
YES
NO
ATPG
ATPG VECTORS
VERILOG ZYCAD SIMULATION
STRUCTURAL PLUS FUNCTIONAL FAULT SIMULATION
VECTORS SETS FOR CHIP TEST
SINGLE ASIC
SCHEMATICS + STRUCTURAL VERILOG
LAYOUT BACK-ANNOTATION VERILOG + SDF TIMING
VERILOG TIMING SIMULATION
COMPARE
YES
NO
GENERATE GDSII
DRC ERC & LVS CHECKS
SKIP GDSII TO FOUNDRY
CHIP FAB



DESIGN TOOLS

C/Pascal	Behavioral model Data (labels) generation Test Vector generation Netlist generation
Veri og	RTL simulation of ASIC Structural design (high level) of ASIC Structural simulation of ASIC Timing simulation of ASIC FPGA simulation End-to-end simulation
Hspice	I/O cell simulation
Epoch	Physica ASIC Design
Concept	ASIC schematics FPGA schematics Board schematics
Sunrise	ATPG
Zycad	Simulation acceleration Fault grading
Xact	FPGA Des gn
Allegro	PC Board Layout
Dracular	ASIC verification

PI C 9

MCD3 Design Process

CAE Tools

ASIC in BGA Package
JPL number to be assigned

ASIC layout

PIC 6

System Board
JPL file no 1996 JPL-27864 AC

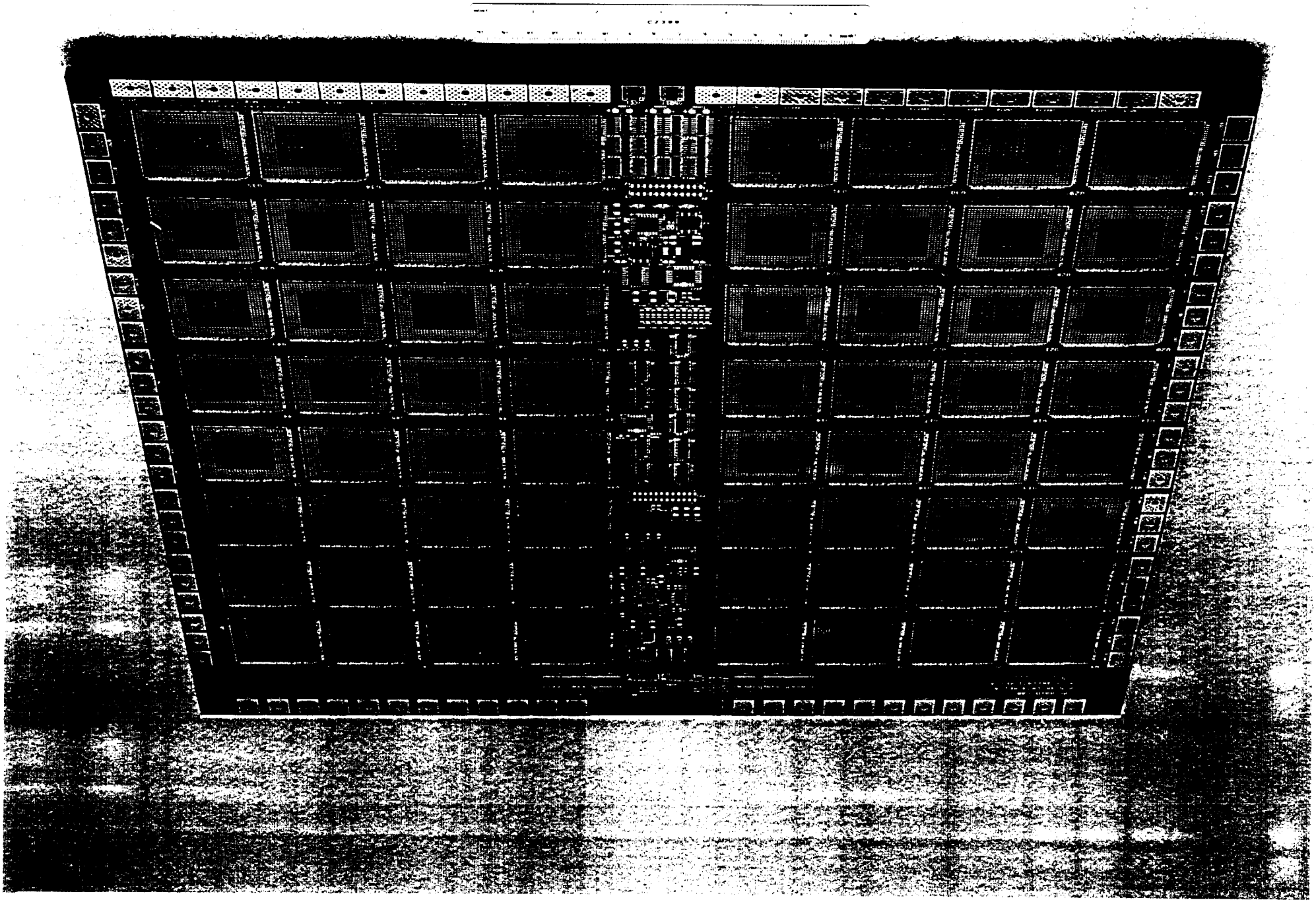
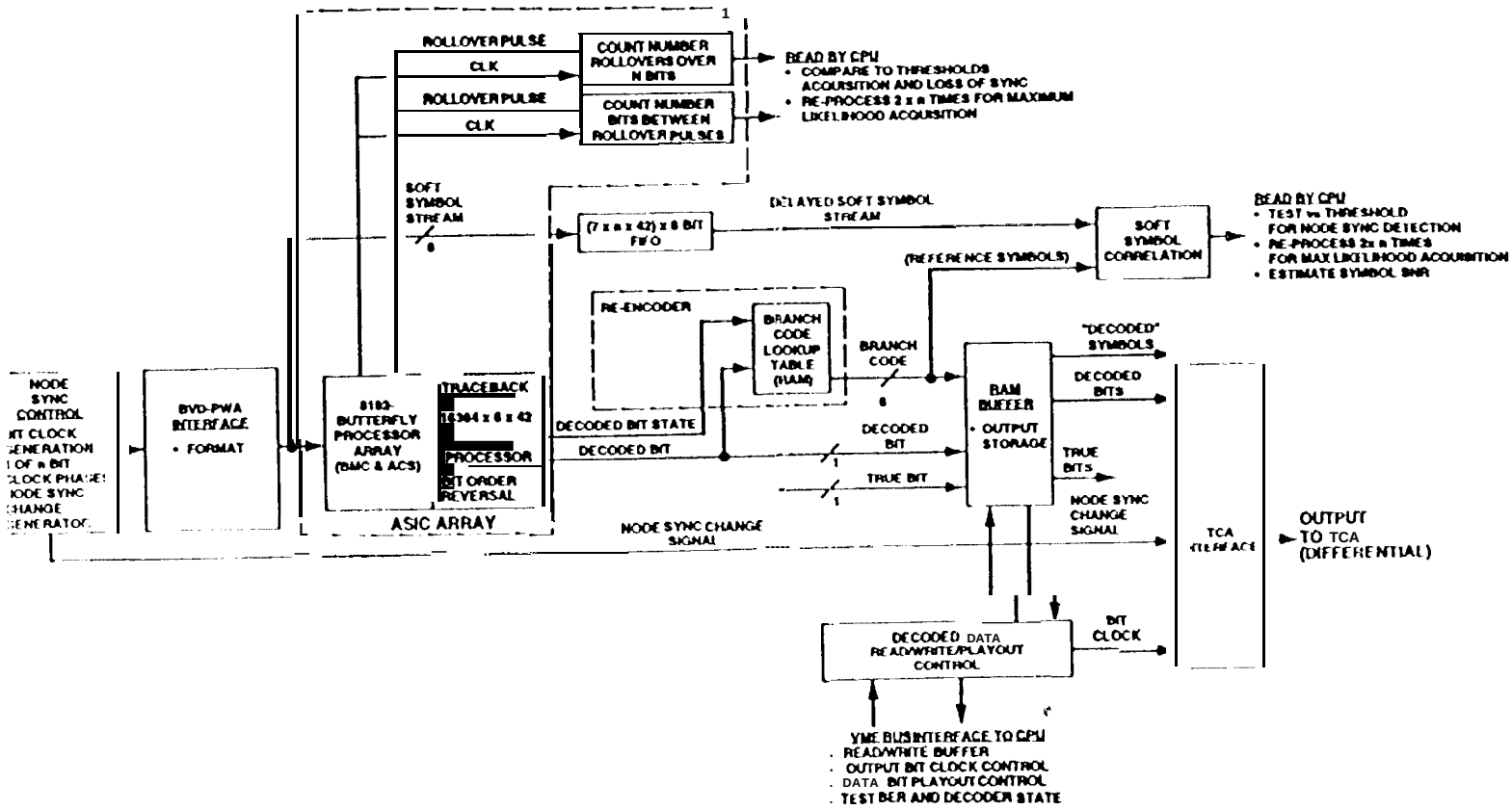


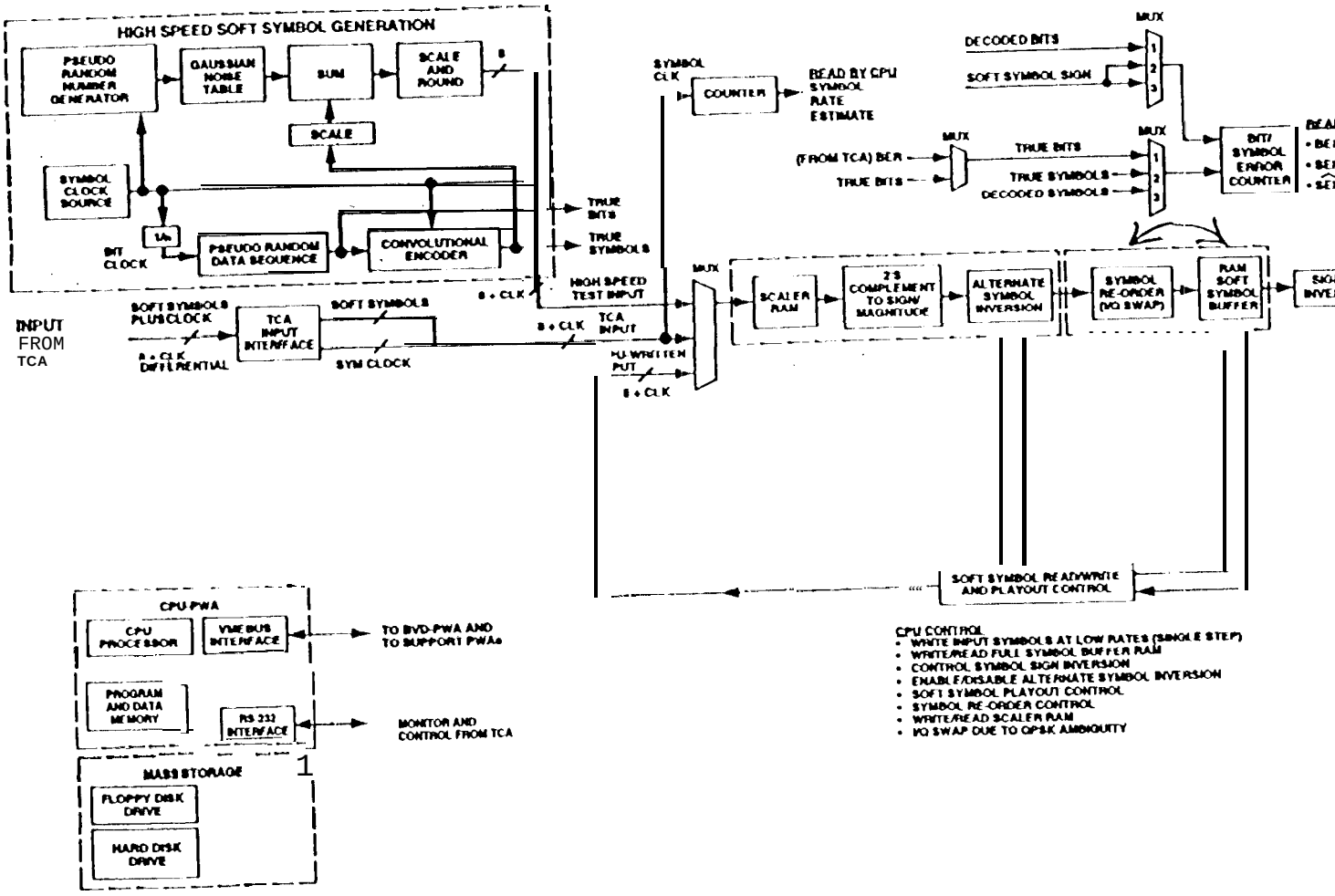
FIG 4

MCD3 Block Diagram

_OCK DIAGRAM


ROLLOVER PULSE
CLK
ROLLOVER PULSE
CLK
COUNT NUMBER ROLLOVERS OVER N BITS
COUNT NUMBER BITS BETWEEN ROLLOVER PULSES
READ BY CPU
• COMPARE TO THRESHOLDS ACQUISITION AND LOSS OF SYNC
• RE-PROCESS 2 x n TIMES FOR MAXIMUM LIKELIHOOD ACQUISITION
SOFT SYMBOL STREAM
(7 x n x 42) x 8 BIT FIFO
DELAYED SOFT SYMBOL STREAM
SOFT SYMBOL CORRELATION
READ BY CPU
• TEST vs THRESHOLD FOR NODE SYNC DETECTION
• RE-PROCESS 2x n TIMES FOR MAX LIKELIHOOD ACQUISITION
• ESTIMATE SYMBOL SNR
(REFERENCE SYMBOLS)
RE-ENCODER
BRANCH CODE LOOKUP TABLE (RAM)
BRANCH CODE
"DECODED" SYMBOLS
DECODED BITS
RAM BUFFER
• OUTPUT STORAGE
NODE SYNC CONTROL
BIT CLOCK GENERATION
BVD-PWA INTERFACE
• FORMAT
8192-BUTTERFLY PROCESSOR ARRAY (BMC & ACS)
TRACEBACK
16384 x 6 x 42
PROCESSOR
BIT ORDER REVERSAL
ASIC ARRAY
DECODED BIT STATE
DECODED BIT
DECODED BIT
TRUE BIT
TRUE BITS
NODE SYNC CHANGE SIGNAL
NODE SYNC CHANGE SIGNAL
TCA INTERFACE
OUTPUT TO TCA (DIFFERENTIAL)
BIT CLOCK
DECODED DATA READ/WRITE/PLAYOUT CONTROL
VME BUS INTERFACE TO CPU
. READ/WRITE BUFFER
. OUTPUT BIT CLOCK CONTROL
. DATA BIT PLAYOUT CONTROL
. TEST BER AND DECODER STATE

B3MCD FUNCTIONAL



Main title:

MCD3 - A Constraint Length 15 Viterbi Decoder

Jet Propulsion Laboratory
California Institute of Technology
Pasadena
California

Caption 1:
Decoding Signals From Distant Space-craft

Caption 2:
Signals arrive with poor SNR - Viterbi Decoding used to improve BER

Caption 3:
Constraint Length 15 gives better BER, but Decoder is complex

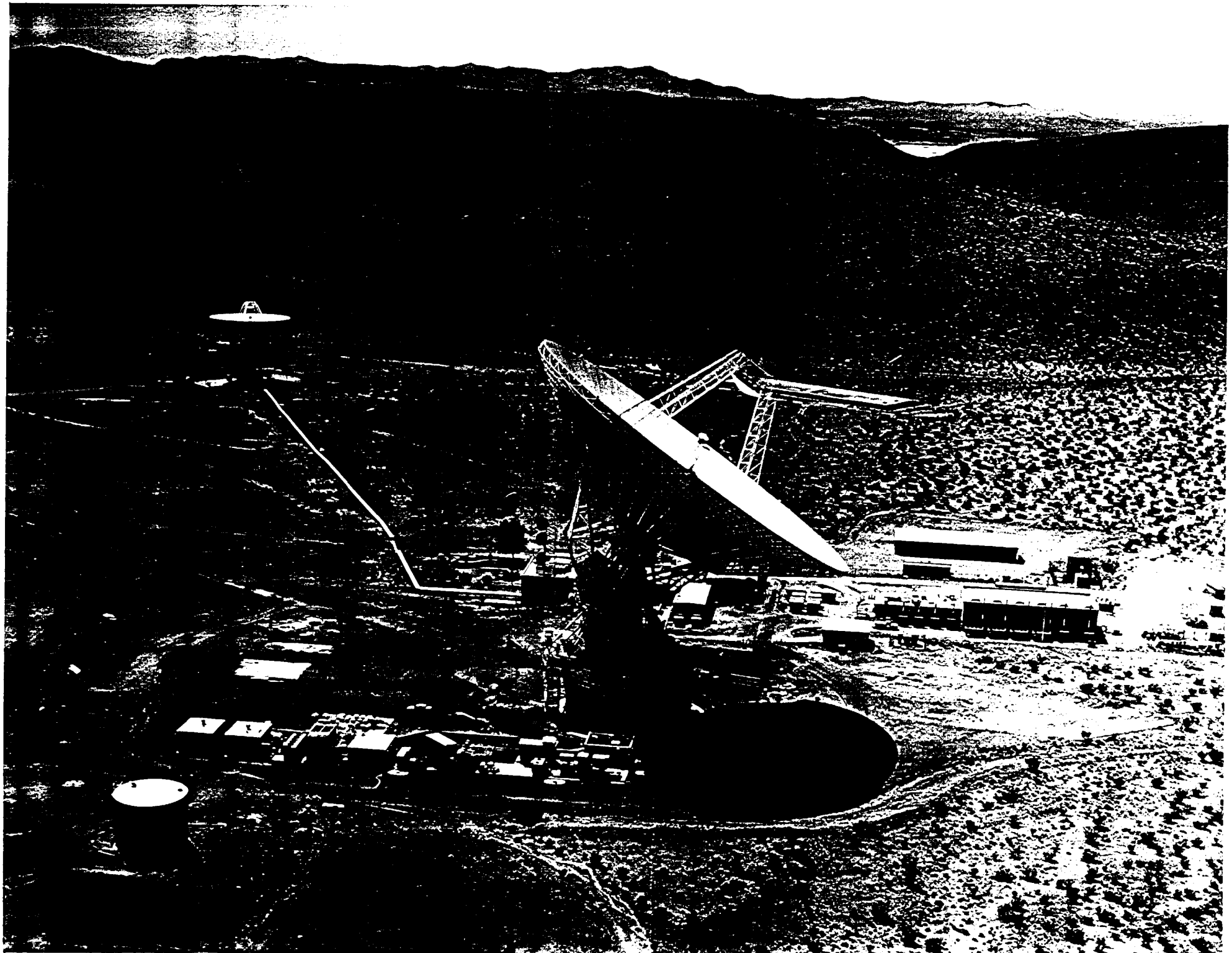
Caption 4:
Complex Design Requires Good CAE Tools

caption 5
MCD3 Group - Jeff Buchanan, Gary Burke, Scott Graham, Robert Johnson, Jim Kowalski, Sho Nakahira, Ernest Stone, Ramona Tung, Bill Whitaker

Acknowledgement: The work described was performed at the Jet Propulsion Laboratory California Institute of Technology under contract with the National Aeronautics an Space Administration.

PIC 1 Space Craft
JPL file no P34311 or equivalent

PIC 2 DSN site
JPL file no JPI 9018AC



5 ft

MAIN TITLE

CAPTION 1

SPACE CRAFT 1

DSN 2

CAPTION 2

S/N chart 3

MCD3 BLOCK DIAGRAM 4

5

CAPTION 3

chip layout 5

board picture. 6

chip picture. 7

CAPTION 4

CAE TOOLS 8

MCD3 - Design Process 9

CAPTION 5