Tit le: MCD3 - A Constraint 1 ength 15 Viterbi decoder

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JPL is responsible for many space missions, as part of NASA's continuing unmanned exploration of the solar system. Signals from spacecraft at planetary distances arrive at 1 arth with poor S/N ratio. To reduce errors, the signals are encoded with an inner code of Viterbi encoding. One of key parameters of Viterbi encoding is the constraint length. Previous spare missions have used a constraint length of 7. Newer missions use 15, to give a considerably improved error correction ability. 1 lowever, the complexity of the Viterbi decoder is increased by '2^(15--/), ie 256X more complex.

At J]']. we have designed a Viterbi decoding with a constraint length of 15 and a speed of 4.4Mb/s. This poster session describes the architecture of the MCD3. The MCD3 uses a large PWB containing 64 AS ICs. There are over 8000 interconnections on this board. The challenges in this design are the large number of interconnections, the high decoding speed, and the complexity.

The ASIC contains 970K transistors. As well as logic it contains 64K bits of RAM. The majority of the ASIC consists of 6 64-bit data paths. There are an additional '/ logic blocks. The ASIC was manufactured by National semiconductor using their 0.55 micron process. It was packaged in a 512 pin super BGA (Amkor).

W c used a combination of design tools for the ASIC. The ASIC was modeled at a behavioral level in c-code. We used Verilog to model at the RTL level. Schematics were drawn in Concept and were converted to Verilog for simulation. 1 Higher level connections were made using Verilog. i Decoding logic was synthesized. Gate level simulation was performed using Verilog and Zycad. Test vectors were generated using ATPG .

Support logic is mostly contained in 3 Xilinx XC4003 PGA's. These were modeled in Verilog, at a high level, then schematics were drawn using Concept. The design was Place and Routed, and converted to verilog for timing simulation.

The poster board will contain:

* Graphical representations of the transmission path from space-craft to ground based decoder
* Graphs showing benefit of 15 1 /6 Viterbi 1 Decoder
* Block diagram of MCD3 system
* Block diagram of JETBVD AS](
* Pictures of ASIC and System Board
* Flow diagrams of Design process
* Text Captions

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