Cascade Helps JPL Explore The Solar System

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At Jet Propulsion Laboratories (JPL), we are involved with the unmanned exploration of the solar system. Unmanned probes observe the planet surfaces using radar and optical cameras to take a variety of measurements. Currently Galileo is orbiting Jupiter; Cassini, due for launch in 1997, will observe Saturn. Upcoming missions include probes planned for Mars, Pluto, a comet, and various other missions. The Mars probe (Pathfinder) includes a small Mars Rover for exploring the Martian surface.

The probes send pictures and data to ground stations which form the Deep Space Network (DSN). Due to the long distances involved and the low transmit power, the signals are difficult to receive and decode , there is more noise received than data.

One method used for signal processing is Viterbi encoding. A set of k bits is encoded to form a group of r symbols which is transmitted to the ground station. The k bits form a shift register. New data is put into one end of the shift register,resulting in a new set of symbols. So the values of the symbols represent not only the new data bit, but also the value of the last kb its. This reduces the effect of random noise on the data. A decoder at the ground station receives these symbols and calculates the most likely value of the data bit. The Viterbi decoder is also called a Maximum Likelihood Decoder (MCD). Although the encoding is simple, the decoding is difficult and increases as 2^k. The decoder consists of 2^(k-2) processors. We split this into 64 ASICs with 128 processors on each ASIC.

Designing this chip was quite a challenge. First pass success was crucial since a low-cost launch window opens only once every 2 years. If we don't hit the window when the Mars Pathfinder is scheduled to launch, it may be 2 years before conditions are right to try again. To ensure we could manage the design's complexity, meet performance goals, and finish the design on schedule, we chose Cascade's Epoch physical design tools and libraries.

Because the design required a large amount (64K) of high speed on-chip memory, we used Cascade's high speed memory generators. Each of our 128 processors is only 1 bit wide. We used (on Cascade's suggestion) the data path compiler to make an efficient layout, using 2, 64-bit wide datapaths. Using Concept (schematics) and Verilog for design entry, Epoch was able to read these without any problem. We also used verilog for simulations. Again, with no major problem.

Epoch's automation greatly accelerated the physical design flow. Its integration between timing and power analysis tools and placement-and-routing let the tools create designs that met our performance goals.

As I mentioned there are 64 ASICs in the design; each ASIC communicates with every other ASIC at the clock speed (60Mhz). Since we couldn't assume all these ASICs had identical delays, there had to be a way to minimize clock skew between ASICs. In discussions with Cascade engineers, we came up with the idea of a 'delay locked loop' for the clock. This solves the clock slew problem, but we also had a major 'ground bounce' problem with 4000 signals switching simultaneously on the board. To reduce ground bounce, we developed a special I/O scheme (SCL) which required the use of a custom input pad cell. Cascade's engineers built both the delay locked loop and the SCL input cell for us.

We also used Cascade for final design verification; DRC and LVS. This step was tricky, and Cascade worked with us to ensure we met our schedule.

The final chip has more than 900,000 transistors. The design only took about 9 months. It was fabricated on National's .5bu process. At the time of writing we have wafers back from fabrication which pass our entire vector

set. This was a tricky design, and getting it right took a lot of simulation time. The ability of the Cascade Epoch tool to quickly generate a design complete with back-annotation timing, was a major factor in the success of this project.

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