

## Progress in GaAs JFETs for 4-Kelvin IR readout applications

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### ABSTRACT

Gallium arsenide junction field-effect transistors (GaAs JFETs) can be made immune to carrier freeze-out, allowing them to operate normally from room temperature down to 4 K. This makes GaAs JFETs attractive for the readout of detector arrays that operate at deep cryogenic temperatures (<10 K). Typical IR readout applications, however, require transistors with very low noise and extremely low input leakage current, and until recently the leakage current of cryogenic GaAs devices was too high for many IR readout applications. By using a recently developed HF-based etchant for GaAs that is highly isotropic, etched GaAs JFETs have been fabricated that have a gently tapered edge. This reduces edge fields, which consequently reduces the edge tunneling current, the dominant source of leakage current at 4 K. JFETs with gate leakage currents below  $10^{-15}$  amps at 4K have been fabricated. The fabrication technique, including the isotropic etchant, is discussed. The leakage current and noise of these JFETs are presented and compared with previous devices using a conventional etch.

**Keywords:** GaAs JFET, deep cryogenic, low temperature, infrared detectors, readout electronics, carrier freeze-out, low frequency noise, leakage current, HF etchant.

### 1 INTRODUCTION

Future ground-based, space-based, and balloon-borne telescopes for infrared astronomy will employ detectors cooled to below 4 K. This includes photovoltaic and photoconductive detectors for the very long wavelength infrared (VJ, VII, approximately 50  $\mu\text{m}$  to 200  $\mu\text{m}$  wavelength), as well as bolometers for 100  $\mu\text{m}$  to millimeter-wave radiation. For small arrays of such detectors consisting of less than ten pixels or so, it previously had been adequate to cool only the detector array to 4 K, and to run a wire from each pixel to a warmer compartment containing the readout electronics. These wires carry heat to the cold head, however, and they are susceptible to noise pickup, which makes this approach impractical for larger arrays or for ultra-low noise levels envisioned for future IR instruments.

Therefore, several different groups have been exploring readout electronics that can operate at 4 K and below, and that can be placed on the cold head immediately adjacent to the detector array<sup>1-6</sup>. Clearly such electronics must circumvent carrier freeze-out and be functional at 4 K. They must also dissipate low power, and have low noise and input current. For the Space Infrared Telescope Facility (SIRTF), for example, the readout electronics are required to dissipate less than 10  $\mu\text{W}$  per channel, have less than 100 electrons per second input current, and have an input-referred voltage noise of less than 1  $\mu\text{V}/\text{Hz}^{1/2}$  at 1 Hz.

JPL has been exploring GaAs JFET-based electronics for such applications for the past several years<sup>7,8</sup>. Because of the very small electron effective mass in GaAs, moderately doped n-type GaAs can be made immune to carrier freeze-out, and a p-n JFET can be made that will operate normally from room temperature down to 4 K. We have concentrated on JFETs rather than MESFETs because the higher gate barrier provided by the p-n junction in the JFET reduces the gate leakage current relative to metal Schottky gate in a MESFET. The principal challenge has been to reduce the noise and gate leakage current to acceptable levels.

## 2. THE DEVICE STRUCTURE.

The device structure is shown in Fig. 1. The device consists of a p-type gate over n-type channel, an undoped spacer, and a semi-insulating substrate. The layer structure is grown by MBE, and wet chemical etching is used to etch back the layers. Details have been previously discussed<sup>8</sup>.

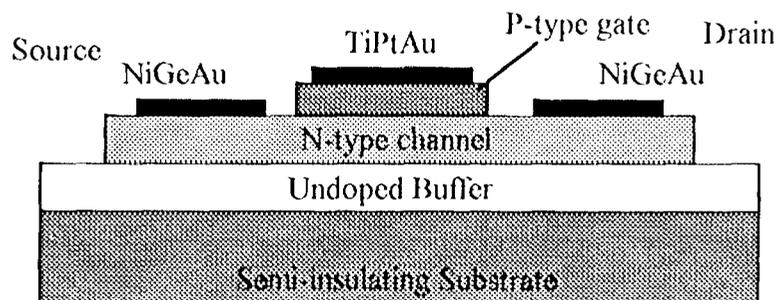


Fig. 1: The structure of the GaAs JFET produced by MBE growth and etch-back. The undoped buffer is approximately  $1\ \mu\text{m}$  thick. The n-type channel is  $3750\ \text{\AA}$  thick and doped with silicon to  $5 \times 10^{16}\ \text{cm}^{-3}$ . The p-type gate is  $500\ \text{\AA}$  thick and is doped to greater than  $5 \times 10^{18}\ \text{cm}^{-3}$ .

## 3. OLD AND NEW GATE ETCH PROCEDURES.

Previously devices were made using a self-aligned gate etch with an ammonium hydroxide based etch. That is, the Ti-Pt-Au gate metalization was patterned by lift-off, during which the photoresist was removed. This Ti-Pt-Au metal contact was then used as the mask for etching away the p GaAs to define the gate. The etchant was a mixture of ammonium hydroxide, hydrogen peroxide and water (11:4:550 by volume). The same etchant was used with a photoresist mask to etch down to the semi-insulating substrate, to electrically isolate one JFET from another. For the remainder of the paper, this procedure will be referred to as the "old process."

Using the gate metal as a mask requires only one mask level to create the entire gate structure, and it resulted in functional devices. Nevertheless, there were several problems with this procedure. First, there is some edge roughness in the gate metalization due to the nature of the lift-off process. This edge roughness is duplicated by the etch in the self-aligned process. This surface roughness tends to enhance the field in localized spots. There is also some undercut, and metal filaments can fall over the edge of the gate, forming a small Schottky barrier diodes between the gate metalization and the n-type channel. Both the field enhancement and the parasitic Schottky contacts tend to increase the leakage current.

For this reason, we began fabricating devices using a second procedure. In this procedure, a photoresist mask is used for the gate etch. The gate metalization is still done using lift-off, but in a separate step rather than self-aligned as in the previous procedure. The mask set is designed so that the gate metal edge falls by several microns inside the edge of the p-type GaAs formed by the gate etch, eliminating any chance of metal overhanging onto the n-type GaAs.

Additionally, the chemistry of the wet chemical etchant was changed. Mixtures of hydrogen peroxide and an acid or base all work by using the hydrogen peroxide to oxidize the GaAs to form gallium oxide and arsenic oxide. These oxides are then dissolved by the acid or base. Even in dilute mixtures, however, most of these etches are not perfectly isotropic, and can result in a retrograde etch wall profile on the 110 faces,

A new, more isotropic etchant has recently been developed based on an hydrofluoric acid/ hydrogen peroxide/ water system<sup>9</sup>. The peroxide oxidizes the GaAs as before. Ordinarily, arsenic oxides dissolve more rapidly in acid/peroxide solutions. In fact, arsenic oxide has some solubility in pure water. It is believed, however, that HF naturally has more of an affinity for gallium oxide. In a dilute solution, this counters the natural tendency for the arsenic oxide to dissolve faster, making the dissolution rates roughly equal. This keeps the etch diffusion limited and consequently isotropic,

The concentration of 2:10:1000" HF:H<sub>2</sub>O<sub>2</sub>:H<sub>2</sub>O was used for the gate etch. The etch rate is approximately 200 Å/min. A slightly less dilute concentration of 2:10:200 was used for the mesa etch, The etch rate of (his solution is approximately 2000 Å/min. For the remainder of the paper, this procedure using a separate gate etch and metalization with the } IF-based etchant will be referred to as the "new process,"

#### 4. A COMPARISON OF GATE CURRENT IN JFETS FABRICATED BY THE OLD AND NEW PROCESSES.

The gate leakage current vs. gate voltage of JFETs fabricated using the old process were measured using the circuit shown in Fig. 2. The resulting leakage current for a typical JFET, in this case ring geometry JFET (l μm long and 125(l μm in circumference, is shown in Fig. 3. The current rises above the 1 pA noise floor at a Gate voltage of approximately -6.5 V, and increases to almost-] nA at a gate voltage of -10 V.

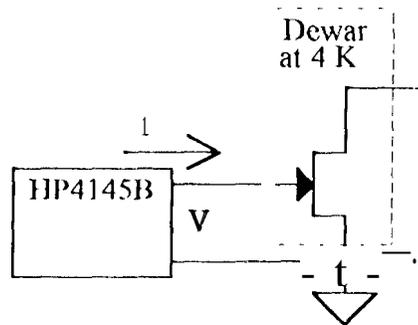


Fig. 2: The circuit used to measure the gate leakage current, An HP4145B semiconductor parameter analyzer is used as an ammeter to measure gate leakage vs. voltage down to a noise floor of approximately 1 pA

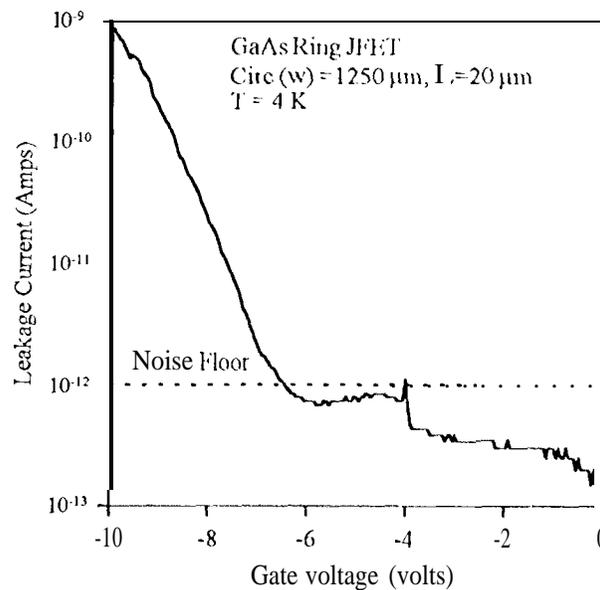
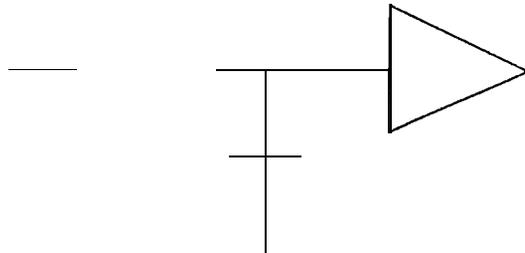
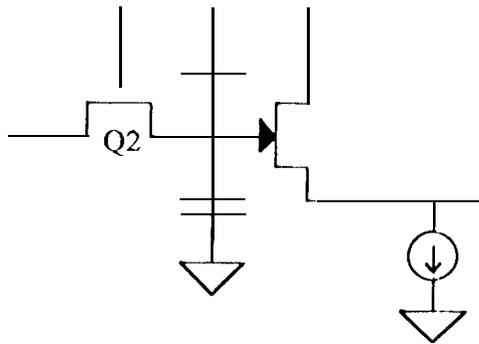


Fig. 3: The gate leakage current as a function of voltage measured using the circuit shown in Fig. 2, for a ring JFET 1250 μm in circumference and 20 μm long made using the old process, The noise floor is approximately 1 pA.

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By comparing the output voltage vs. the injected signal, and knowing  $A_v$  and the capacitance  $C_2$ , it is possible to calculate the remaining capacitance  $C_x$ .

For the measurements reported below, the JFET under test was a rectangular structure  $20\ \mu\text{m}$  wide and  $25\ \mu\text{m}$  long.  $V_{DD}$  was set 103 V, and the load bias current on the source of the JFET was  $10\ \mu\text{A}$ .  $C_2$  was a discrete 1 pF capacitor,

For the gain measurement, the output varied linearly from 1.21 to 3.10 V as the reset voltage was swept from 0 to 2 V, implying a gain of  $A_v=0.94$ . For the capacitance measurement, the circuit was first DC biased by setting the reset voltage to 1 V and toggling Q2 on and then off. Because of the leakage is so small when the circuit is cold, this bias remains essentially unchanged during the duration of the AC measurement. A 1-kHz signal of 1 V amplitude was then injected onto the test point. The resulting output voltage amplitude was 40 mV. The capacitance can be calculated using Eq. 2, below

$$C_x = \frac{A_v \cdot V_{in} - V_o}{V_o} C_2 \quad \text{Eq. 2}$$

The capacitance  $C_x$  calculated using Eq. 2 and the measured values was 22.6 pF. This indicates that there is a great deal of stray capacitance, since the capacitance of the discrete capacitor  $C_1$  was 1 pF, and the capacitance of the JFET was only 0.35 pF. Probably the stray capacitance comes mainly from the drain and package capacitance of Q2, together with trace-to-ground plane capacitance on the circuit board. For the leakage test, the injection test point connected to  $C_2$  is grounded, so the total capacitance  $C_1$  is the sum of  $C_2$  and  $C_x$ , or  $C_1 = 23.6\ \text{pF}$ .

For the actual leakage test, the reset was set to 1 V and Q2 was then toggled on and off as described above. The reset voltage was then returned to 0 V after Q2 was off. The output voltage  $V_o$  was then recorded as a function of time. The resulting  $V_o$  vs. time for the JFET is shown in Fig. 6. The output voltage varies by approximately 41 mV over the 29 minute integration time. Using the calculated gain and capacitance with Eq. 1, the calculated leakage current is:

$$I_{leakage} = 0.59\ \text{fA} \quad \text{Eq. 3}$$

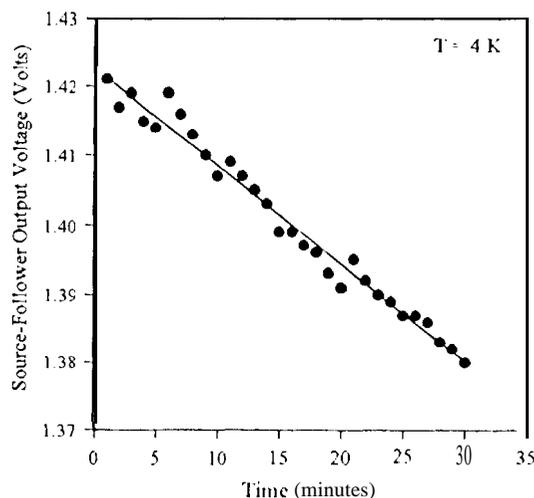


Fig. 6: The source-follower output voltage  $V_o$  as a function of time, from the leakage current integrator shown in Fig. 4, for a rectangular JFET fabricated using the new process. The entire circuit was held at 4 K. The total integration capacitance was measured as 23.6 pF.

## 5. THE TRANSISTOR NOISE FOR THE OLD AND NEW PROCEDURES

The input-referred voltage noise for a JFET fabricated using the old process and a JFET fabricated using the new process are compared in Fig. 7. The old JFET was a ring structure 1250  $\mu\text{m}$  in diameter and 20  $\mu\text{m}$  long, with a capacitance of approximately 18 pF. The new JFETs is a rectangular structure 300  $\mu\text{m}$  wide and 100  $\mu\text{m}$  long with a capacitance of 21 pF. Both JFETs were biased at 1  $\mu\text{A}$  drain current; the drain voltage was 1.0 V for the old JFET and 0.6 V for the new JFET. Both curves are characteristic of  $1/f$  noise.

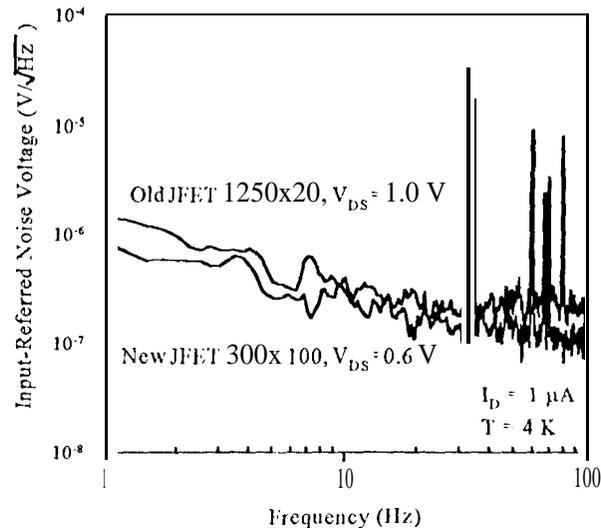


Fig. 7: The input-referred voltage noise at 4 K for a ring JFET (1250  $\mu\text{m}$  circumference by 20  $\mu\text{m}$  long) fabricated with the old process, and the comparable noise for a rectangular JFET (300  $\mu\text{m}$  wide by 100  $\mu\text{m}$  long) fabricated with the new process. The noise spike at 60 Hz is due to pickup of line frequency noise. The spikes at 35 Hz and 80 Hz are signals injected to calibrate the gain, and the spike at 70 Hz is a harmonic of the 35 Hz fundamental.

## 6. SUMMARY

A new gate etch process has been developed that substantially improves the performance of JFETs intended for deep cryogenic operation. Where before the etch was done using an ammonium hydroxide-based etchant and using the gate metalization as a mask, the new procedure separates the photolithography for the gate etch and the gate metalization into two steps. In addition, a more isotropic HF-based etch is used. The new procedure reduced the gate leakage by many orders of magnitude, from leakage on the order of a pA to less than one fA. The noise is also reduced somewhat.

The noise and leakage performance are closing in on those required for deep cryogenic space astronomy missions such as SIRTf. Further work is presently underway including the fabrication of more discrete JFETs using the new procedure, and characterization of their gate leakage current and noise, as well as the construction of small scale integrated multiplexers.

## 7. ACKNOWLEDGMENTS

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