Non-destructive measurements for CMOS devices using charge collection techniques

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ABSTRACT

Results of an experiment providing initial validation of the use of charge collection spectroscopy to measure the overlayer and epitaxial thickness and substrate diffusion length are given for two CMOS SRAM test devices.

The research described in this paper was carried out by the Jet Propulsion Laboratory, California Institute of Technology, under a contract with the National Aeronautics and Space Administration.

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INTRODUCTION

The accelerating use of commercial parts in space applications increases the necessary, but expensive radiation testing for several reasons. For example, identifying a "fortuitously bard or tolerant" process or build requires a test survey of manufacturers or lots. Also, because commercial processes undergo continual change (to increase yield, for example), flight lot testing is needed to confirm that the radiation response is consistent with design-case results from earlier testing. Further contributing to the need for testing is the reluctance of commercial manufacturers to disclose basic construction information for a device, such as whether it's On bulk silicon or has an epitaxial layer. This paper will tend to validate a simple test method, based on charge collection techniques and performable on the benchtop, that will augment (and may reduce the need for) accelc.rater-based heavy ion testing, by accurately measuring three key physical parameters, epi-thickness, average overlayer thickness, and substrate diffusion length.

Epi thickness is an important parameter contributing, for example, to susceptibility to latchup. The overlayer thickness is less important, except for ions with rapidly changing LET. Because a significant amount of the collected charge can come from outside the epi layer [1] [2], the substrate diffusion length controls the "excess" collected [3].

EXPERIMENTAL DATA

Total collected charge is easily measured using the techniques pioneered by P. McNulty and his students, e.g. [4] [5] : a charge sensitive pre-amp is connected in the supply line of a static biased DUT (device under test) and a histogram of the resulting pulse distribution is collected on a multi-channel analyzer (MCA).

The test devices were drawn from a set of devices used in a previous study of latchup vs. epi thickness [6]. These devices are special versions of the Harris 11S6516 CMOS (p-well) 16Kb SRAMs. Two samples with a grown epi thickness of 9 pm (reduced to 501 6 by plot.cssil~~ [7]) were irradiated with four energies of alpha particles produced by the Caltech van de Graaff accelerator. One (denoted by IRRAD) had been irradiated in the previous study with various heavy ions while the other (denoted by UNIRR) was previously unirradiated. Collected charge measurements, taken from the MCA peak centers and calibrated using a surface barrier detector (SBD), for two devices are summarized in "J'able I.

TABLE I. Measured Collected Charge for Two 11s6516 Devices \ ,

Alpha energy (MeV)	range in Si (microns)	initial LET - MeV per mg/cm^2	Q (fC) UNIRR device	Q (fC) IRRAD device
2.0	7.2	"1.04	43.9	39.2
2.93	11.3	0.86	87.2	74.7
4.0	17.3	0.-/1	116	71.8
6.1	32.0	0.s5	114	49.1

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For the 2 MeV cases, the peaks are fairly broad due to localized variations in over-layer stopping thickness. Higher energies are less sensitive to these variations and the peaks are quite sharp. Peak centers were determined by center-of-mass type calculations on the measured spectra. During the calibration it was noted that the ratio of SBD response to initial particle energy was constant (accurate to 2 digits), indicating that it is unnecessary to distinguish ionization stopping power from total stopping power for the energies considered here.

At the lowest energies, the ion stops in (or close to) the epi layer, so collected charge is approximately proportional to the ion energy as it enters the epi. Therefore collected charge increases with increasing initial ion energy at the lowest energies. At the higher energies, the alpha particle goes through the epi and collected charge decreases with increasing energy because incident LET decreases with increasing energy, compensated to some extent by charge diffusing in from the substrate. Note that the IRRAD device collects much less charge at the higher energies than UNIRR, consistent with less charge from the substrate. Displacement damage from the earlier latchup testing reduced the (already small) IRRAD substrate lifetime to the extent that little charge is collected from outside the epi layer.

DATA ANALYSIS

A simple quantitative model, verified by computer simulation [3], is sufficient to analyze the raw data. The model is based on the assumption that collected charge is the sum of the charge liberated in the epi, Q_{epi}, plus another contribution, Q_{diff}, that diffuses from the substrate to the epi. Q_{diff} is composed of contributions from many small ion track sections. These $\delta_i Q_{diff}$ are the amount of charge that diffuses to the epi when $\delta_i Q$ is liberated a perpendicular distance y_i below the epi. When the substrate diffusion length or L_D is small compared to substrate dimensions (almost always true), simple diffusion theory produces the equation:

$$Q_{diff} = \sum \delta_i Q_{diff} = \sum \exp(-y_i/L_D) \cdot \delta_i Q$$

Q_{epi} depends not only on epi thickness, but also on overlayer thickness because some ions stop in the epi and also because ion LET varies with penetration depth. The deposited charge $\delta_i Q$ in all three layers was derived from the range-energy tables of the TRIM code (version 95.0?). A simple computer code automates these calculations.

Estimates of overlayer thickness, epi thickness, and substrate diffusion length are obtained by analyzing the experimental data with the model. Overlayer thickness and epi thickness should be consistent for both devices, but substrate diffusion length is different for the two. More weight is given to the UNIRR device because there is likely to be some recombination loss in the IRRAD epi which reduces model accuracy. Excellent agreement between the model and data was produced by the following parameters:

average over-layer thickness =	4 μm (both devices)
epi thickness =	5 μm (both devices)
diffusion length =	11.5 μm for the UNIRR device
	2.5 μm for IRRAD

Note that overlayer thickness includes all dead layers and is a Si equivalent, which will be larger than actual physical dimensions if there are any very dense structures. Furthermore, the devices tested were planarized, which also tends to increase overlayer thickness. Therefore the 4 μm estimate is credible, as are the fitted epi thickness and diffusion lengths.

Model predictions derived form the above data are compared to the measurements in Figure 1. Forcing the epi thickness equal to 9 μm (the pre-processing, value) dots not agree very well as seen in Figure 2. Similar comparison show that 4 pm is too small and 6 μm is too large.

The substrate contribution to total collected charge can be more clearly seen in Figure 3 where the model curve of Figure 1 is plotted normalized to Q_{epi}. It is most informative to plot this against ion penetration depth below the over-layer, and the result is shown in Figure 3. It is clear that the substrate supplies a significant amount of charge for the UNIRR device,

FUTURE WORK

The full paper will present a larger, fuller test matrix including results on a modern commercial p-substrate SRAM using the benchtop test method with naturally occurring, alpha sources.

CONCLUSION

The technique discussed in this paper provides a convenient, inexpensive approach to determine the effective charge collection depth of integrated circuits. It can not only distinguish between devices fabricated on bulk and epitaxial substrates, but allows the actual effective epitaxial thickness to be determined. It is potentially useful as a hardness assurance tool to track the consistency of charge collection between different production runs and may also be useful for initial evaluations of similar devices from different manufacturers.

The initial experiments were done on devices with n-substrates, for which the underlying substrate contribution is smaller because of the lower can ier lifetime. However, the technique is even more significant for p-substrates, which not only have longer lifetimes, but have more uncertainty (and potential variability) in the effective epi-layer thickness because of boron diffusion from the highly doped Substrate in the epi.

REFERENCES

[1] P.E. Dodd, F.W. Sexton, and P.S. Winokur, "Three-Dimensional Simulation of Charge Collection and Multiple-Bit Upset in Si Devices," *IEEE Trans. Nucl. Sci., vol.-l* 1,110.6, pp.? 005-20 17, December 1994.

[2] H. Dussault, J.W. Howard Jr., R.C. Block, M.R. Pinto, W.J. Stapor, and A.R. Knudson, "High Energy Heavy-Ion-Induced Single Event Transients in Epitaxial Structures," *IEEE Trans. Nucl. Sci.,* vol.41, no.6, pp.2018-2025, December 1994.

[3] L. Edmonds, "Charge Collection in Simple Epi Diodes," to be submitted to the *Journal of Applied Physics*.

[4] P.J. McNulty, D.R. Roth, W.J. Beauvais, W.G. Abdel-Kader, and D.C. Dinge, "Comparison of the Charge Collecting Properties of Junctions and the SEU Response of Microelectronic Circuits," *Nucl. Tracks and Radiat. Mess.,* vol. 19, nos. 1-4, pp.929-938, 1991.

[5] P. J. McNulty, W. J. Beavais, and D. R. Roth, "Determination of SEU Parameters of NMOS and CMOS SRAMS," *IEEE Trans. Nucl. Sci.,* vol.38, 110.6, pp. 1463-1470, December 1991.

[6] L. S. Smith, D. K. Nichols, J. R, Coss, W. E. Price, and D. Binder, "Temperature and Epi Thickness Dependence of the Heavy Ion Induced Latchup Threshold for a CMOS/EPI 16K Static RAM," *IEEE Trans. Nucl. Sci.,* VOl.34, no.6, pp. 1800-1802, December 19987

[7] D. Takacs, J. Harter, E.P. Jacobs, C. Werner, U. Schwabe, J. Winnerl, and E. Lange, "Comparison of Latch-Up in P- and N-Well CMOS Circuits," *IEDM Technical Digest,* pp. 159-163, 1983.

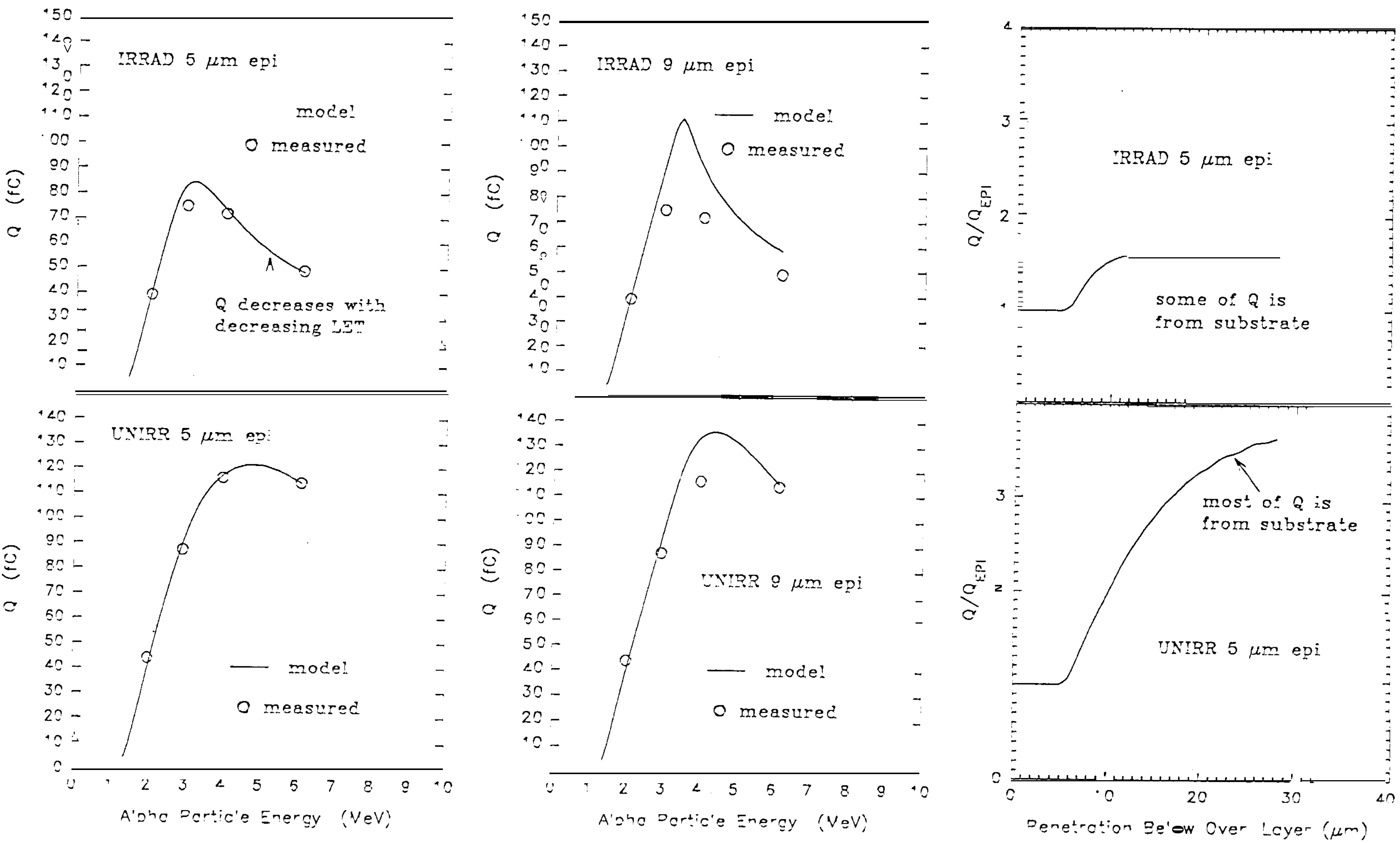

Figure 1: Selecting all parameters for a best fit results in a $4\mu m$ over-layer, $5\mu m$ epi, and diff. length=$2.5\mu m$ (IRRAD) and $11.5\mu m$ (UNIRR).

Figure 2: Using a $9\mu m$ epi but selecting other parameters for a best fit, given epi thickness, results in a $4\mu m$ over-layer and diff. length= 0 (IRRAD) and $7\mu m$ (UNIRR).

Figure 3: Same data as Figure 1 but plotted with different units.