# Progress in voltage and current mode on-chip analog-to-digital converters for CMOS image sensors

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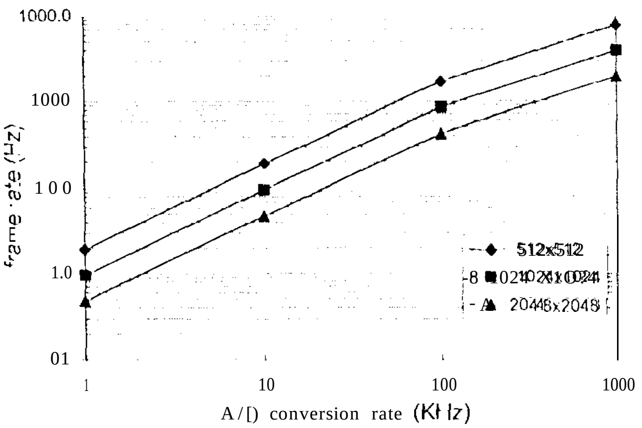
## ABSTRACT

Two 8 bit successive approximation analog-to-digital converter (ADC) designs and a 12 bit current mode incremental sigma delta (Σ-Δ) ADC have been designed, fabricated, and tested. The successive approximation test chip designs are compatible with active pixel sensor (APS) column parallel architectures with a 20.4 μm pitch in a 1.2 μm n-well CMOS process and a 40 μm pitch in a 2 μm n-well CMOS process. The successive approximation designs consume as little as 49 μW at a 500 KHz conversion rate meeting the low power requirements inherent in column parallel architectures. The current mode incremental Σ-Δ ADC test chip is designed to be multiplexed among 8 columns in a semi-column parallel current mode APS architecture. The higher accuracy ADC consumes 800 μW at a 5 KHz conversion rate.

## 1. INTRODUCTION

A key advantage to CMOS image sensors is the ability to integrate readout electronics on the same focal plane as the sensor as shown in figure 1. Through the use of standard CMOS technology there is available a wide variety of approaches to analog to digital conversion[1,2]. Sensor chip architectures placing analog to digital converters (ADC) in each column offer parallel conversion of an entire row of pixel data. This parallelism reduces the requirement for high speed ADCs (figure 1). For example, the minimum conversion speed of an ADC in each column of a 1024 x 1024 image sensor operating at a 30 Hz frame rate is approximately 33 KHz. Overhead for transferring off-chip the resultant digital image data can increase this speed requirement but can be overcome using either pipelined data transfer during the conversion or a high bandwidth digital output port.



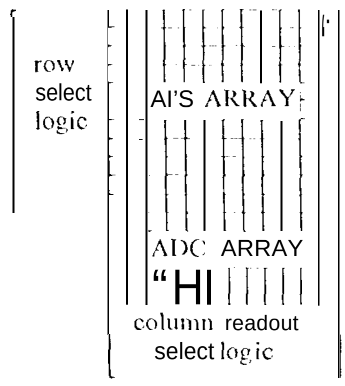




*Figure 1. Frame rate vs. ADC speed for a 512x512, 1024x1024, and 2048x2048 APS with the above column parallel architecture for focal plane A/D conversion (1,5 μsec row access time assumed).*

A design tradeoff in placing an ADC per column is the low power requirement and increased physical size resulting from the small column pitch (10 to 40 μm depending on the process technology). A small pitch can also lead to column to column variations in ADC response because of poor device matching. To minimize these problems a compromise is possible, for example, by multiplexing a single ADC per 8 columns.

Because both voltage mock and current mock active pixel sensors arc used, there is a need for both voltage and current mode ADCs. The two successive approximation ADCs presented below operate in voltage mode and the sigma-delta ADC operates in a current mode. The successive approximation designs physically fit into a per column architecture and the sigma-delta fits onto an 8 column pitch where its operation is multiplexed.

The design and test results for each ADC are presented below. Section 2 describes the operation and test results of a successive approximation ADC approach using switched capacitor op amp integrators. Section 3 presents a successive approximation ADC based on charge redistribution on a network of binary scaled capacitors. Section 4 describes the operation and test results of the current mode sigma-delta ADC. Section S contains a summary of the three design characteristics.

## 2. SWITCHED-CAPACITOR SUCCESSIVE APPROXIMATION ADC

The successive approximation approach to analog-to-digital conversion is essentially a "ranging" algorithm. The new feature in the successive approximation ADCs presented below is the double sided approach to conversion. The ADC attempts to add successive binary fractions of a reference voltage to either the pixel signal or met level until they are equal. in this way if a comparison result is false, the ADC saves a step by not having to remove the previously added reference fraction from the signal. The ADC was designed for an APS sensor with a readout scheme where the pixel reset voltage is greater than the pixel signal level as in [3]. The voltage levels at each step "i" in the conversion arc shown in figure ? and are described by:

$$V_{S,i} = V_{S,i-1} + b_i \cdot \frac{V_{ref}}{2^i}$$

$$V_{R,i} = V_{R,i-1} + \bar{b}_i \cdot \frac{V_{ref}}{2^i}$$

$$b_i = 0 \quad \text{if } V_{R,i-1} < V_{S,i-1}$$
$$= 1 \quad \text{if } V_{R,i-1} > V_{S,i-1}$$

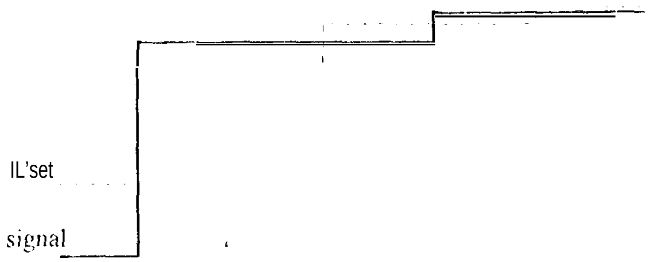



*Figure 2. Internal ADC sampled reset and signal levels during conversion*

### 2.1 Design and operation

The first design approach uses two switched-capacitor integrators to perform the successive approximation analog to digital conversion. This successive approximation method attempts to find the digital representation of the pixel signal relative to the pixel reset level. It does this conversion by successively adding binary scaled fractions of a reference voltage to either the readout pixel signal voltage or pixel reset voltage until the two values are equal to within the desired accuracy or one least significant bit (1 LSB).

The schematic of the ADC is shown in figure 3. The ADC has two inputs for pixel signal and reset levels (VS and VR). There is also an input for the ADC voltage reference range. All input voltages are referenced to V-I . The top op amp integrator stores the pixel signal level and the bottom op amp integrator stores the reset level. Both integrators are inputs to a comparator. During the $\Phi_{ON}$ interval the pixel signal level, reset level, anti ADC reference arc sampled onto the 2.5 pF capacitors C] and (?. The top and bottom integrators are reset to V-I during $\Phi_S$ anti $\Phi_R$, respectively. The signal level, VS-V-1, is sent to the top integrator input daring, the $\Phi_S/\Phi_{IS}$ interval. With a 5 pF op amp feedback capacitor, the integrator gain is -]. "1'bus, the value V-I - VS is added to integrator output voltage. The reset level, V+-VR, is similarly added to the bottom integrator output during the $\Phi_R/\Phi_{IR}$ interval. The reference level (Vref-V+) is stored on C1 and C? during $\Phi_{REF}$.

After the inputs arc read into the ADC, $\Phi_{ON}$ turns off and the first comparison is performed to determine the sign bit (typically 0 for the image sensor). The comparator is activated when the STRB* signal goes low. Otherwise both comparator outputs are O. If the signal side is greater than the reset side, the comparator output into the shift register is a O. In this case, the feedback from the comparator output sets the switches on the front end to steer the reference on C2 to the integrator on the reset side holding the lower output voltage. Because C 1 is cutoff from C2 during this time, the gain of the integrator is -0,5 (= 2.5pF/5pF). Thus, (V+-Vref)/2 is added to the integrator output. For correct operation V+> Vrcf so that the voltage is increased on integrator with the lower output voltage.

During the second comparison, the MSB is determined and stored in the shift register. Before this comparison is performed, the feedback path from the comparator is shot off disconnecting the inputs to the integrator. During the comparison half the charge cm C 1 is transferred to C2. The resulting voltage across on C2 is (Vref-V+ )/2, Subsequently, C1 is cutoff from C2, the comparison is made, and (V-t -Vref)/4 is transferred to the output of the integrator with the lower output voltage (reset side if the original pixel signal is more than 1MSB larger than the met level, otherwise to the signal side).

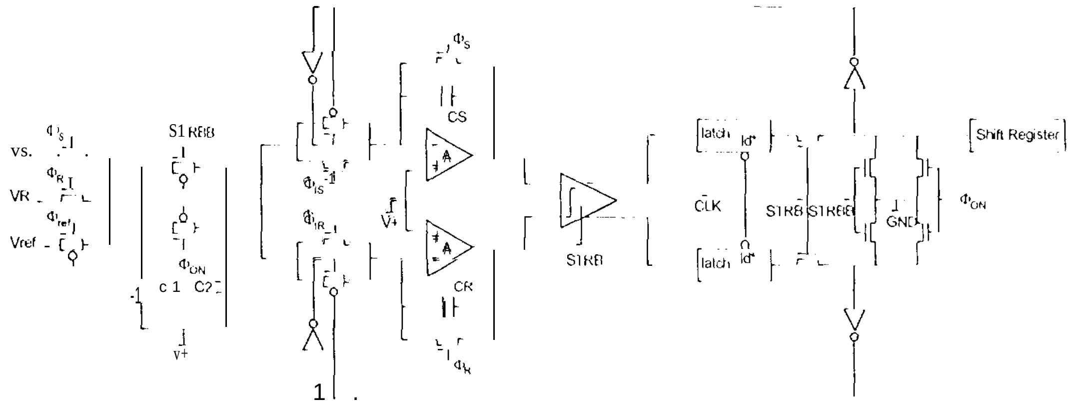



*Figure 3. Successive approximation A IX' circuit using switched capacitor integrators*

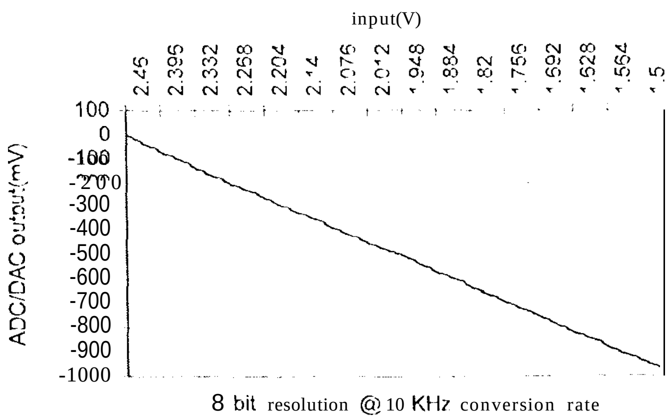
The binary scaled fraction of the reference voltage is always added to the integrator with the lower voltage stored on it. The integration and comparison steps are performed until the desired number of bits is achieved. A shift register per column stores the comparator output for readout of the digital word at the end of the conversion.

One of the key components in this design is the switched capacitor integrator. To achieve at least 8 bit resolution, an 13p amp with a gain of 60 dB (1,000) is required[1]. The op amp used in this design is a single stage folded cascode op amp.

Cascade

## 2.2 Test results

The ADC was characterized using a 1 V ramp to drive the input from a computer controlled data generator/acquisition board. The analog input was incremented in 1mV steps and 500 ADC output samples at each step were acquired. ADC output Was passed through a digital-to-analog converter (DAC). The analog output of the ADC/DAC was connected to the computer acquisition board where it was measured. The DAC has an offset voltage of OV and a -1 V reference.




8 bit resolution @ 10 KHz conversion rate

*Figure 4. Transfer curve for a successive approximation ADC implemented with switched capacitor circuits.*

The ADC was characterized at different speeds and power levels. Because of the application of this ADC to the column parallel architecture of a CMOS image sensor, the maximum power dissipation desirable from the ADC is approximately 150 to 2.00 μW. At these power levels, the ADCs in a 1K x 1K image sensor consume 150 to 200 mW.

For a power dissipation of 175 μW and 8 bit resolution, the maximum conversion rate is 50 KHz or 20 μseconds/conversion. The maximum 1 K x 1 K sensor frame rate for this conversion speed is approximately 451 Hz. Integral non- linearity (INL), differential non-linearity (DNL), and ADC noise *were* measured (Table 2). The ADC noise is determined from the worst case standard deviation calculated from the 500 samples taken at each input step. Based on the non-linearites, the effective ADC accuracy is 5 bits. The ADC operating at a 10 KHz conversion rate worked at a minimum power of 27 μW. Its effective accuracy is also 5 bits. The transfer curve for the ADC operating under best case conditions at 10 KHz and 134 μW power level is shown in figure 4.

Stand alone op amps on the test chip were characterized at various power levels. The op amp had a gain of 74 dB and consumed 70 μW. At a low power dissipation level of 20 μW, the op amp had a gain of 80 dB. However, at the low bias current levels, the op amp slew rate limited the ADC speed.

## 3. BINARY SCALED CAPACITOR SUCCESSIVE APPROXIMATION ADC

This approach to ADC design uses a dual networks of binary scaled capacitors to sample pixel signal and reset voltages. These capacitor networks are connected to the input of a comparator. After clamping these levels on the top plate of the capacitors, the bottom plates are successively connected to the ADC reference voltage. The voltage increase on the top plate is proportional to the relative size of the capacitor to the total capacitance of the network. The comparator output determines which side sees an increase in the top voltage similarly to the switched capacitor integrator approach. This method of using binary scaled capacitors to perform analog to digital conversion is similar to [4]. This ADC uses the same new feature as the switched capacitor design presented in the previous section where a double sided approach is used to increase converter speed.

### 3.1 Design and operation

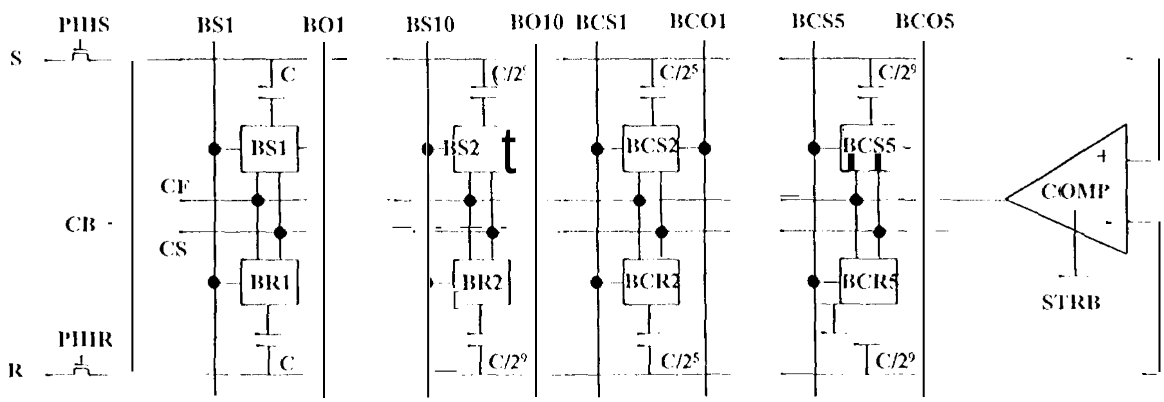



*Figure 5. Binary scaled capacitor successive approximation ADC*

The *block* diagram of the dual sided binary scaled capacitor successive approximation ADC is shown in figure 5. Each of the latches (BS#n-BR#n) contains a switch either to ground or to the ADC voltage reference as shown in figure 6. If the enable to the latch BS#n on the signal side is active and the comparator output is high (reset input > signal input at the comparator), the bottom plate of the capacitor is switched from O to Vreference. If the same enable to the latch BR#n on the reset side is active and the comparator output is low (signal input > reset input at the comparator), the bottom plate of the capacitor is switched from O to Vreference. The latch connected to the largest capacitor C contains the sign bit. When the sign bit is 1, the voltage on the signal side increases by Vref x (C/Ctotal) where:

$$C_{TOTAL} = C + C/2 + C/4 + C/8 + C/16 + C/32 + C/64 + C/128 + C/256 + C/512 = 1.998C.$$

“1'bus, the operation is similar to the integrator approach where Vref/2 is added to the signal side after the first comparison if the signal is greater than the reset level. The value of the largest capacitor used is 4 pF.

The latches on the signal side contain the final binary WOKI at the end of the conversion. Because the charge redistribution 011 the top plates is relatively fast compared to the charge transfer in the switched capacitor integrator approach, the ADC conversion rate is higher. Also, it consumes less power and is less sensitive to process non-uniformities because no op amps arc required. 1 lowever, placing a total of 16 pF of capacitance per column consumes a large amount of silicon area.

Also included in the ADC are 5 capacitor bit cells for storing the comparator offset. This offset is calculated at the end of each conversion by enabling the CB switch. When this switch is enabled both inputs to the comparator are set equal so that the offset can be measured and stored for off chip correction.

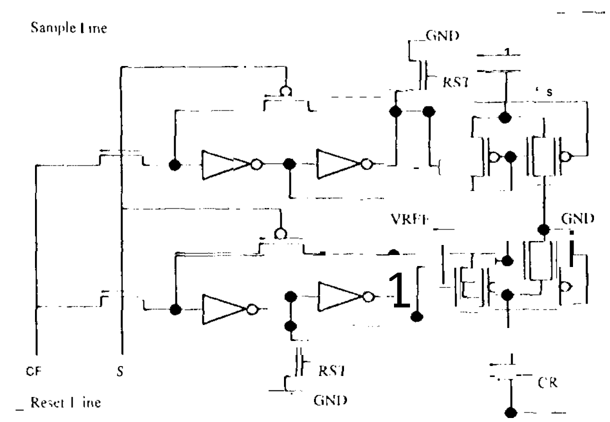



*Figure 6. Bit cell latch/switch to the capacitor bottom plates for the signal and reset sides*

### 3.2 Test results

The ADC was characterized in a similar manner as the op amp integrator successive approximation ADC. A 1.2V input ramp with 256 steps was used to drive the ADC input. Noise measurements were based on 200 samples at each step.

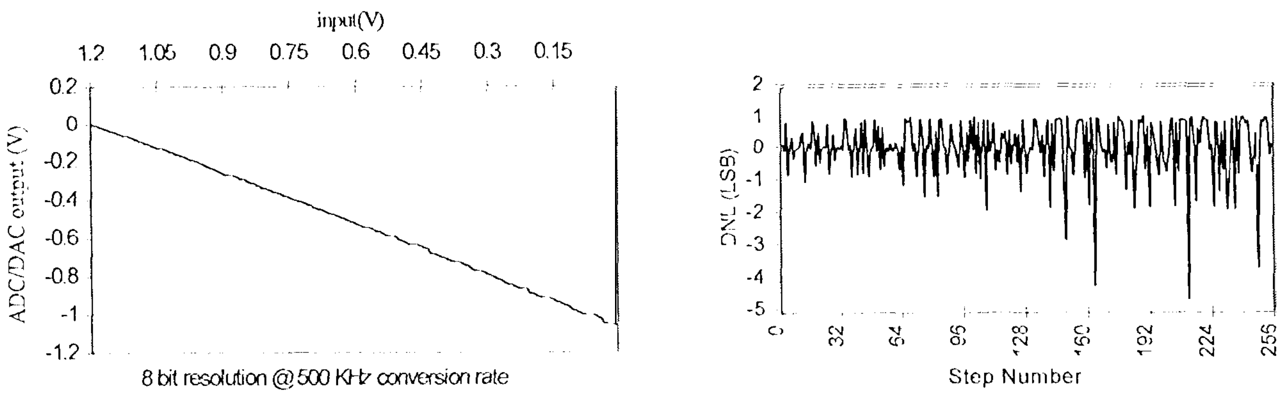



*Figure 7. Transfer curve and DNL error at 500 KHz conversion rate for the successive approximation ADC implemented with a binary scaled capacitor network.*

The transfer curve and the differential non-linearity plot of the ADC at a 500 KHz conversion rate is shown in figure 7. The effective accuracy of the ADC at a 500 KHz rate is 5 bits (Table 2). The ADC operated as high as 833 KHz with the same accuracy except for 4 input levels that generated large DN1, and INL errors. The ADC consumed 49 μW at the 500 KHz speed. The power dissipation is primarily from the comparator and $CV^2f$ component in charging the capacitor network.

The maximum frame rate for a 1K x 1K sensor using this 500KHz ADC conversion rate is 279Hz. The frame rate will be less depending on the bandwidth and timing of the sensor's digital output port.

## 4. CURRENT MODE SECOND ORDER INCREMENTAL SIGMA DELTA ADC

Oversampling methods for ADC design are attractive because they avoid many of the difficulties with conventional methods for A/D and D/A conversion, Conventional converters require high precision analog circuits. On the other hand oversampling converters, can use simple and relatively low precision analog, components. This current-mode approach uses no MOS op-amps or linear capacitors. The main building block is a current copier cell. Though they require fast and complex digital signal processing stages, their robustness is suited for fast growing VLSI technology.

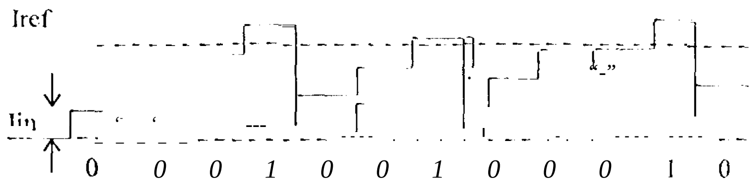



*Figure 8. Typical Σ-Δ event sequence*

A first-order Σ-Δ ADC requires $2^n$ cycles to perform a n-bit A/D conversion. The accumulator and comparator output levels are shown in figure 8. Typically the comparator output is used to increment a counter that at the end of the conversion contains the digital number representation of the analog input. Conversion speed can by significantly increased by cascading two first order stages, resulting in an incremental Σ-Δ ADC topology. The architecture of the current-mode second-order incremental Σ-Δ modulator is based on the one reported in [5].

### 4.1 Design Overview

Figure 9 shows a block diagram of the current-mode second-order incremental Σ-Δ modulator. The three main building blocks are the current integrator, current comparator, and the digital to analog current converter. There are two loops, connected in cascade. Output of the comparator, "a" for the first comparator and "b" for the second one, becomes "1" if the output of the integrator, I, is greater than the reference current $I_{ref}$. Otherwise it is "0". A D/A converter in the feedback loop outputs $-I_{ref}$ if the output of the comparator is "1", otherwise it outputs no current.

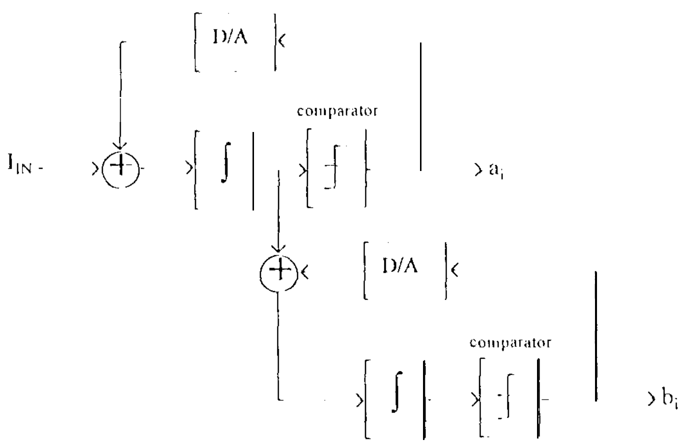



*Figure 9. Block diagram of the second order sigma-delta ADC*

The basic building block of these components is the current copier Cell. The principle of a current copier cell, also called a dynamic current mirror, is shown in figure 10. A single transistor $M_m$ is combined with 3 switches $S_X$, $S_Y$, and $S_Z$ that are implemented by means of additional transistors, and a capacitor C. In the first phase (phase 0), $M_m$ operates as the input device of a mirror, with its gate and drain connected to the input current source. When equilibrium is reached, capacitor C at the gate is charged to the gate voltage V required to obtain $I_D = I_0$. The value of $I_0$ is thus stored as a voltage across C. In the second phase (phase 1), $M_m$ operates as the output device of a mirror, with its drain disconnected from the gate and connected to the output node. It sinks an output current $I_1$, that is controlled by the same gate voltage V and thus is equal to $I_0$.

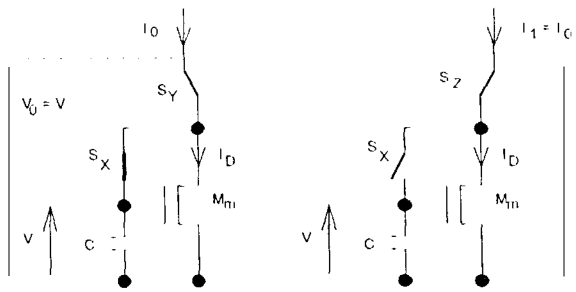



*Figure 10. Current copier cell in memorize mode (left) and output mode (right).*

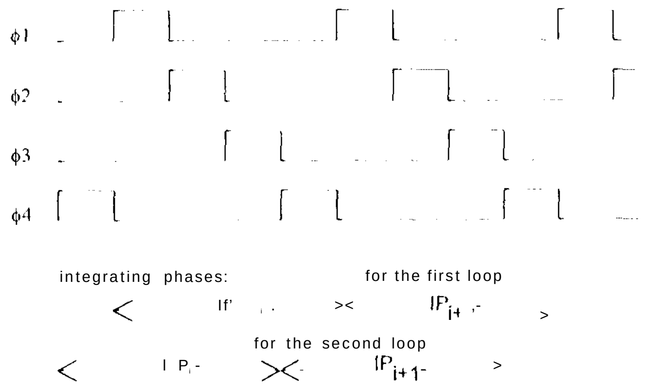



*Figure 11. Sigma delta timing*

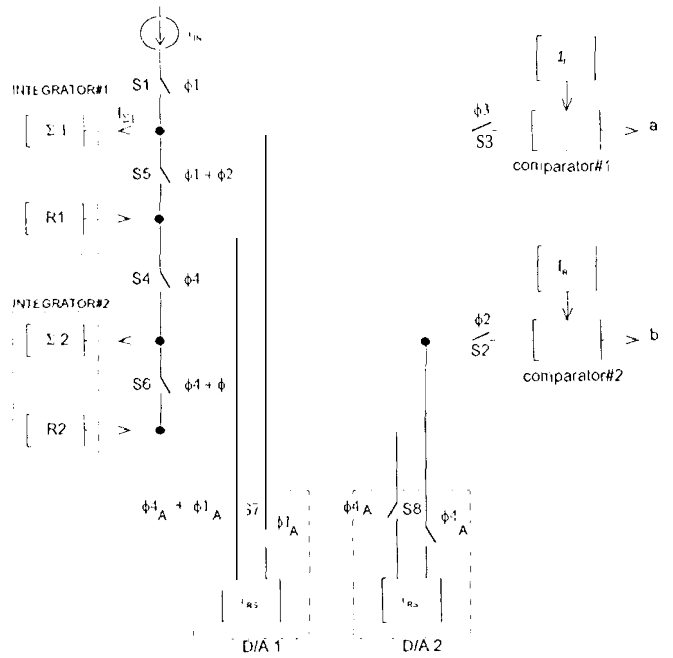



*Figure 12. Current mode sigma-delta ADC*

## 4.2 Operation

The de.tailed operation of the converter based on the block diagram in figure 12 is as follows: Each integration period consists of 4 phases (figure 1 1). Phase 1 is used to sample the input current. For the first integration period "i", the register in the first integrator is zero. Thus, during phase 1 only the input current is memorized at integrator# 1's summing current copier. During phase 2, the output of the summer is copied to integrator# 1's register. Phase 3 is used to compare the summing current copier to the reference current. If this copier cell current is gt-eater than the reference, al is a " 1". in phase 4 the output of the integrator# 1's register is memorized by integrator#2's summing current copier. If $a_1$ is a "l" the reference current is subtracted from the output of the first integrator's register. During the beginning of integration period "i+1" starting with phase 1, integrator# 1 memorizes the sum of the output of its register and the input current. If $a_1$ is a "l" the reference current is also subtracted from this sum.

The timing for the second integrator is the same as the first integrator except the above operations are offset by one phase. During phase 1 (following the phase 4 cycle during which integrator# 1's register output was memorize) the current from integrator#2's summing current copier is copied to integrator#2's register. During phase 2, the comparison takes place between the summing current Copier and tile reference current. No events occur during phase 3. During the beginning of the next integration period for the second integrator starting with phase 4, the summing copier memorizes the sum of the output of its register and the output of integrator# 1's register. in addition, the reference current is subtracted if tile output of the comparison during phase 2 was resulted in b, equal to "1".

The expressions for two integrator's summing current copier cells at the end of "p" integration cycles arc:

$$I_{\Sigma 1}[p,3] = p \cdot I_{in} - \sum_{i=1}^{p-1} a_i \cdot I_{ref}$$

$$I_{\Sigma 2}[p,2] = \frac{(p-1)\cdot p}{2} \cdot I_{in} - \sum_{i=1}^{p-1} a_i \cdot (p-i) \cdot I_{ref} - \sum_{i=1}^{p-1} b_i \cdot I_{ref}$$

At the end of p integration cycles the digital representation of the signs delta output is determined by:

$$DN = \sum_{i=1}^{p-1} a_i \cdot (p-i) + \sum_{i=2}^{p-1} b_i$$

The digital filter consisting of a counter and accumulator is used to generate the digital number. The relationship between resolution of the ADC and number of integration cycles p (number of times the input current is sampled) is shown in table 1. The digital filter for the test chip was implemented off-chip.

### 4.3 Test results

The ADC was tested using a computer controlled current source and the output data from the off-chip digital filter was read by the computer data acquisition board. The input current ramp consisted of 4096 steps of 4nA each. At each input step 20 samples were acquired. The DC current bias was 40 μA. The transfer curve is shown in figure 13.

The 12 bit ADC consumed a total of 800 μW when operating at a 5 KHz conversion rate. From differential non-linearity measurements the accuracy of the ADC is 10 bits.

| resolution n (bits) | p (oversampling ratio) |
|---|---|
| 6 | 12 |
| 7 | 17 |
| 8 | 24 |
| 9 | 33 |
| 10 | 46 |
| 11 | 65 |
| 12 | 92 |
| 13 | 129 |
| 14 | 182 |

*Table 1. Relationship between ADC resolution and integration cycles "p"*

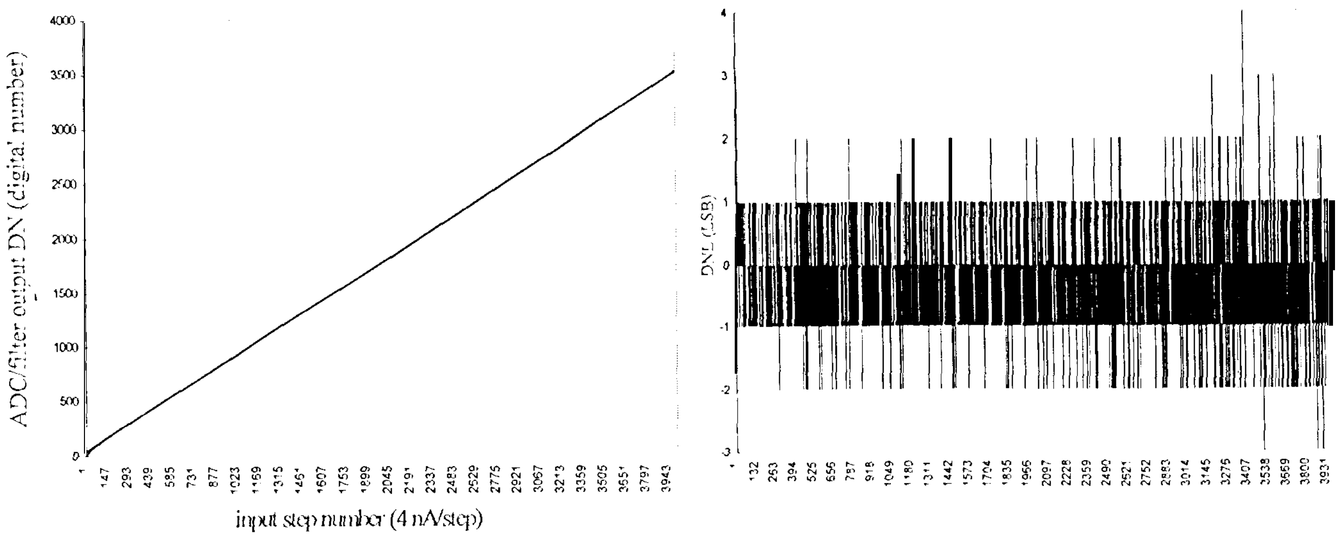



*Figure 13. Transfer curve and DNL error at 5 KHz conversion rate for 12 bit incremental sigma delta ADC.*

## 5. SUMMARY

Column parallel architectures of CMOS active pixel sensors require low power compact analog-to-digital converters. Two types of successive approximation ADC designs and a current mode sigma delta ADC design for integration into CMOS active pixel sensors were demonstrated. Table 2 lists their characteristics. For voltage mode APS sensors, the 8 bit successive approximation ADC using binary scaled capacitors achieves the highest speed and accuracy. This ADC's new feature of using dual capacitor banks to achieve high speed enables the development of high frame rate sensors. The current mode sigma delta converter has the highest accuracy of the ADC designs. Its inherent robustness makes it ideal for application in high accuracy CMOS image sensors.

| ADC TYPE | Resolution units= Bits | Accuracy units= #LSBs DNL[+] | INL[+] | NOISE | conversion rate KHz | power dissipation μW | size |
|---|---|---|---|---|---|---|---|
| op-amp S.A. | 8 | 3 | 6.5 | 2 | 50 | 175 | 20.4 μm x 1.94 mm |
| | 8 | 3 | 5.9" | ?.9 " | 10 | 134 | (without shift reg.) |
| | 8 | 2 | 5 | 2.25 | 10 | 27 | |
| binary scaled | 8 | 5 | 3.5 | 1.9 | 500 | 49 | 40 μm x 4.2 mm |
| capacitor S.A. | 8 | 4* | 5* | 21* | 833 | 55 | |
| current mode incremental Σ-Δ | 12 | 2 | 10 | 2.5 | 5 | 800 | 80 μm x 3.6 mm |

* removing selected non-linear data points

[+] units are +/-

*Table 2. Summary of ADC designs and test results*

## 6. ACKNOWLEDGMENTS

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