CMOS Active Pixel Sensor Star Tracker with Regional Electronic Shutter

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Abstract

A 64x64 element CMOS active pixel sensor (APS) for star tracker applications is reported. The chip features an innovative regional electronic shutter through the use of an individual pixel reset architecture. Using the regional electronic shutter, each star in the field of view can have its own integration period. This way, simultaneous capture of bright stars with dim stars is accommodated, enabling a large increase in tracker capability). The chip achieves 80 dB dynamic range, 50 e- r.m.s. read noise, low dark current, and excellent electronic shutter linearity.

1. Introduction

The guidance system in a spacecraft determines spacecraft attitude by matching an observed star field to a star catalog. Future celestial star tracker systems for space applications should be small in mass and power consumption, be radiation hard, have a high fill factor, and high sampling resolution. In addition they need to accommodate a wide dynamic range of illumination levels. Since a star tracker centroids an intentionally blurred star image, the effect of' pixel geometry on the centroiding algorithm should be minimal. An AJ'S-based system can reduce mass and power consumption and radiation effects compared to a CCD-based system[1]. An important feature of the AI'S is the potential to have different integration times in different regions of interest. 'I'his allows the simultaneous capture of bright stars with dim stars. With a CCD system, a single integration period for the entire sensor is necessitated. This means that either the bright star is properly exposed but the dim star is lost in the noise, or that the dim star is properly exposed but the bright star is saturated and useless for centroiding. A different integration period for each star is much better suited for the star tracker application. 'J 'ypically only a few stars are used for tracking in a given field of view. 'I'his paper reports an APS with locally variable integration times, achieved through individual pixel reset (IPR).

2. Individual pixel reset (IPR)

A traditional AP'S pixel [1] includes a detector, a single reset transistor and readout scmrcc-follower circuitry, as shown in Fig. 1a. The detector photogate is labeled PG, the transfer gate TX, the reset

transistor RST, and the row selection transistor RS. A photodiode-type APS does not use a photogate, as shown in Fig. 1 b, and has been previously used for random access image sensors [?.]. Since all reset transistor gates in a given row are connected in parallel, the entire row is reset when the reset line is activated. The integration period is the time from pixel reset to pixel readout. In order that pixels cm the same row can have different integration periods and do not saturate, individual pixel reset (IPR) is required. Circuitry at the bottom of the column (e.g. load transistor, sample and hold circuitry') is not shown for simplicity, and has been well reported previously[3].

A simple way to implement IPR would be to put a second transistor in series with the row reset transistor, activated by a vertical column reset signal. Unfortunately, this has been shown to introduce reset anomal i es when it has been used in CMOS readout circuits for infrared focal-plane arrays for astronomy[4]. This is believed to be due to charge pumping from the output node to the reset drain.

In our work, IPR is implemented via a simple configuration of two reset transistors as illustrated below in Fig. 2. The column reset (C ST) and row reset (RRST) lines must both be at a logical high voltage to activate the reset transistor. While not a major advance in itself', the simple configuration allow low noise, anomaly-free readout, ant] permits the implementation of a smaller pixel with higher fill factor compared to previously reported efforts for 10CMI exposure control [5]. T 'he IPR allows the user to select a small region of interest in the image and adjust the integration time for that region. It is noted that non-destruct ive readout of the pixel can be performed at any time during the integration period by

activating the row select Transistor RS and reading the voltage on the column bus. Non-destructive readout can be used to determine the optimum exposure period for a given region of interest.

3. Chip Architecture

The proposed chip has an architecture generally similar to former CMOS APS designs[6]. However, to accommodate full random access control, i.e. independent reset and readout per pixel, two sets of row and column controls are provided (Fig. 3). The left and bottom set of row and column decoders, respectively, are similar to those in former APS designs and used for readout. The right and top set of row and column decoders, respectively, are provided for independently resetting any pixel address within the array, without interfering with the readout process.

The chip was implemented as an array of 64 x 64 photodiode-type APS elements using the HP 1.2 μm n-well process available through the MOSIS service. The pixel pitch was 20.4 μm (V) x 20.4 μm (H) resulting in a die size of 2.5 mm x 2.6 mm.

Since the modulation transfer function, or MTF, of the sensor is critical for star tracker applications, several different variations of the pixel design were explored. The 64 x 64 element array was divided into 6 regions, each with its own pixel design, as seen in Fig. 4. An L-shaped photodiode pixel (32 x 32

elements) with maximum designed fill factor (28.9%) occupied the upper eft portion of the chip. The same pixel with a second level metal light shi el d covering the entire pixel except the 1,-shaped photodiode occupied the upper right hand portion of the chip and was also sized at 32x32 elements. A square pixel with a lower designed fill factor (14 .6°/0) occupied a sub array of size 16 x 32 elements. The same pixel but with a light shield cover ing the entire pixel except the square photodiode occupied the same array size. The fifth design was a rectangular pixel with slightly higher fill factor (15.7VO) than lhc square pixel, and it also occupied a 16 x 32 elem ent subarray, ant] the 'same pixel with a light shield like that above occupied the remaining 16x32 element subarray. The expectation was that the 1 -shaped pixel would have maximum response due to its higher fill factor, but that perhaps the square or rectangular pixels would be easier to use In a centroiding algorithm due to their more regular shape. The light shield helps separate response from the nominally "dead" regions of the pixel containing the readout circuitry from that of the defined photodiode.

4. Experimental result s

'J he chip was successfully fabricated and tested. T he sensor was operated at 5V. Only the RRST signal was driven at 7\J to improve the reset of the floating diffusion node. Initial testing focussed on operating the chip in a normal imaging mode, where the total chip readout time was also the integrati on time. The 64 x 64 element output image was displayed on a monitor using a commercial scan converter. From the visual image, the effect of the light shield was apparent, indicating that

signifi cant response is obtained from the "dead" readout region of the pixel. 'l-his effect had been previously known from laser spot scanning measurements of intra pixel response[7].

A second visual observation was that the square pixels without a light shield had the greatest responsivit y (volts/watt). The responsivity is related to designed fill-factor, "dead" region response, and capacitance. in general, without dead area response, photodiode-type .4PS pixels have constant responsivity, independent of pixel size or fill factor. 'l 'his is because the area of the photodiode contributes both detector area (more respon sivity) and capacitance (less responsivity), anti these effects cancel. Ilowever, the response of the "dead" area increases the signal but does not increase the detector capacitance. '1'bus, the square pixels, with response in the dead area, had a greater total responsivity.

'1 'he sensor was quant itati vely tested for relat i ve responsi vity, conversion gain, sat urat ion 1 me.], input refer ed noise, dynamic range, dark current and fixed patten noise. The results are presented below in table 1. 'l 'he conversion gain was in general agree.mc.nt with the design estimate of capacitance of the photodiode. The sat uration level was approximately 2 volts. Read noise of light shielded pixels was typically measured to be higher than that of the non-light shielded pixels, perhaps because the d.c.-biased light shield is capactively coupling in noise to the floating node. The input referred read noise is less than that predicted by simple kTC noise models, as has been observed in other photodiode-type APS arrays. Separate Monte-Carlo model ling work at JPL suggests a reduction of the order of $\sqrt{2}$, a

result not far from these experimental results. Fixed pattern noise (FPN), not suppressed by on-chip circuitry, was measured to be approximately 0.5% saturation, or 10 mV peak-lo-pcalc. The FPN results from non-uniformity in the threshold voltages of source-follower circuits at the bottom of each column, since the standard APS sampling of the pixel before and after reset suppresses FPN from pixel-lo-pixc] thi eshold variations. 1)ark current was measured to be of the order of 400-800 pA/cm^2 at room temperature, or 10-20 m\~/see, output referred. A star tracker would typically be. cooled to further reduce dark current for 1 onger integration periods. No smear or blooming was observed due to the lateral overflow drain inherent in the. APS design.

Functional testing of the pixel resetting circuitry confirmed the operability of the individual pixel reset operation. An area of' the chip spanning 16 columns from 16 rows was selected for additional reset, T 'his resulted in a region less-exposed. An output image example is shown in Fig. 5. The darker region across the image represents pixels that were reset during the nominal integration time, so that they had a shorter effective integration t imc. Some pixels in the majority of the image appear saturated, or white.

The linearity of the "electroni c shut ter" operation was measured by measuring sensor output as a function of integration time for various exposure settings, but with the same scene illuminate. The output as a function of integration time is shown in Fig. 6. The slopes of these curves are plotted as a function of exposure selling in Fig. 7. The linearity of the electronic shutter is quite good.

5. Conclusions

A CMOS AI'S image sensor that permits regional elect] onic shutter ing has been designed, fabricated and tested. T 'he' chip functions as expected, though a great er response was obtained from pi xels with smaller designed fill factor. An innovative approach to implementing individual pixel reset was described and demonstrat ed. The successful implementat ion of this chip paves the way for lower risk implementat ion of larger format sensors (e.g. 1024x1024) *with* the i ndividual pixel reset desi gn. T he design approach is valid for both photodiode-type AI'S pixels, as well as plmk)gate-type APS pixels. The excellent linearity of the electronic shutter operation will al so permit the use of the architecture in detector arrays for mm-imaging appl ications, such as spectroscopy, where very large dynamic. range between nearby channels must be accommodated.

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Figure captions

Fig. 1 a.(Left) Photogate-type AI'S pixel circuitry.

Fig. 1 b (Right) Photodiode-type AJ'S pixel circuitry.

Fig. 2. Photodiode-type AI'S pixel with individual pixel reset circuitry

Fig. 3. Block diagram of implemented image sensor

Fig. 4. Photograph of' fabricated chip. Labels refer to pixel designs described in the text.

Fig. 5. Sensor output with region of short integration time through George Washington's eye.

Fig. 6. Sensor output as a function of integration time for various exposure settings.

Fig. 7. 1 .inearity of exposure control. Absolute vertical values depend on scene illuminance.

	Relative response	Conv. gain [μV/e⁻]	Sat. level [V]	Noise [μV] rms	Input ref. noise [e⁻]	Dyn. range [dB]	Dark rate [mV/sec]	Dark rate [e⁻/msec]	Dark rate [nA/cm²]	FPN
"L" shape	0.74	3.2	1.99	120	38	84	13.6	4.29	0.5	0.45%
Shield. "L"	0.46	3.2	1.91	165	52	81	10.9	3.43	0.4	0.45%
Square	1.00	5.6	1.99	195	35	80	17.7	3.16	0.7	0.45%
Shield. sq.	0.42	4	1.8	205	51	79	15.9	3.97	0.8	0.56%
Rectangular	0.98	4.6	1.99	195	42	80	15.5	3.36	0.7	0.44%
Shield. rect.	0.41	4.6	1.8	225	49	78	16.4	3.56	0.8	0.5%

Table 1. Performance of various sensors.

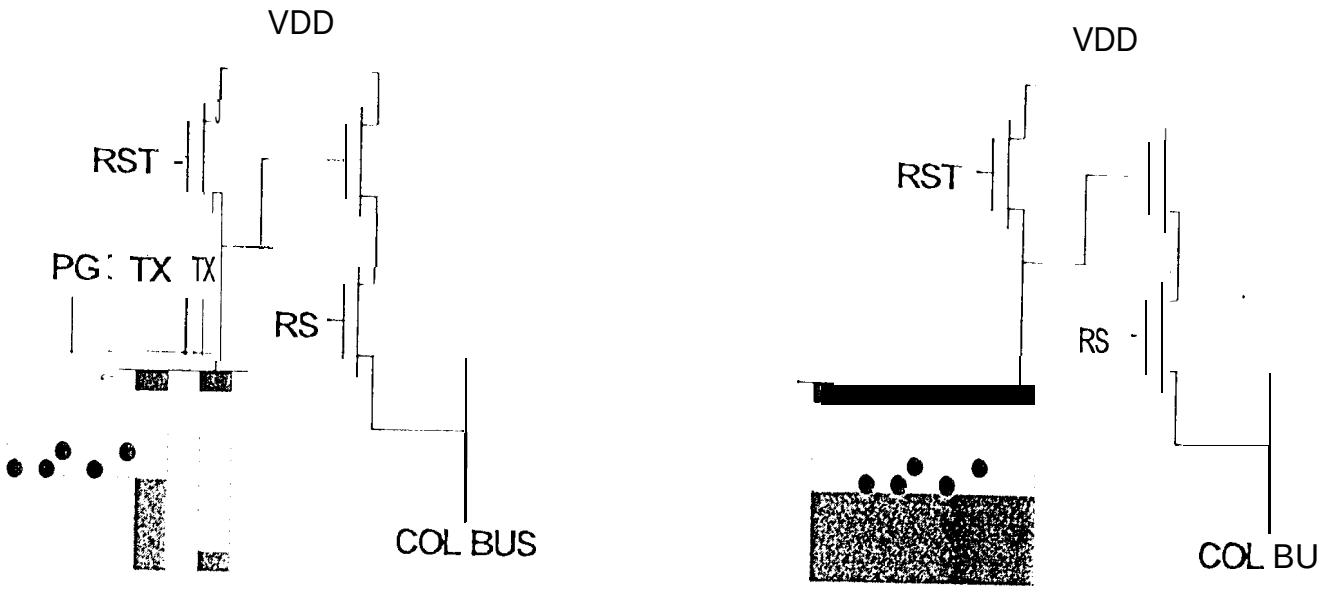

Fig. 1a (Left) Photogate-type APS pixel circuitry.
Fig. 1b (Right) Photodiode-type APS pixel circuitry

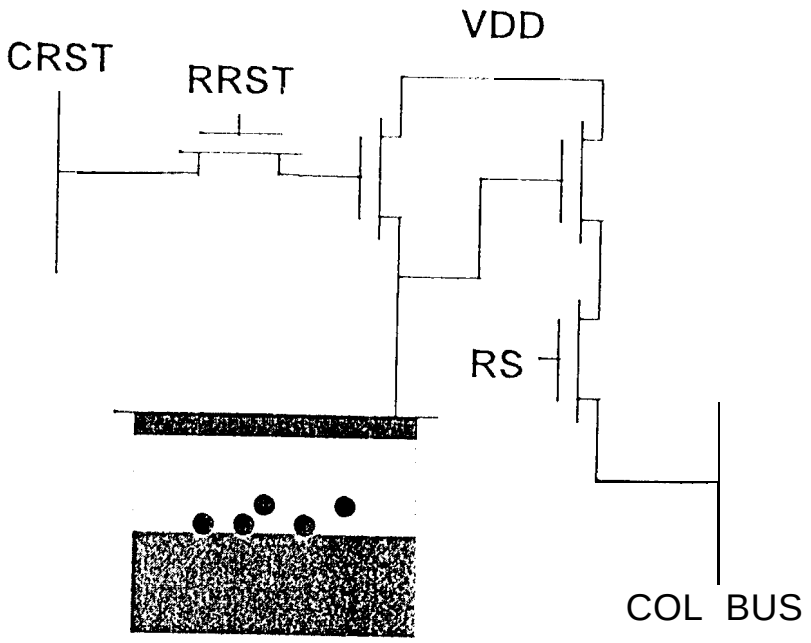

Fig. 2. Photodiode-type APS pixel with individual pixel reset circuitry

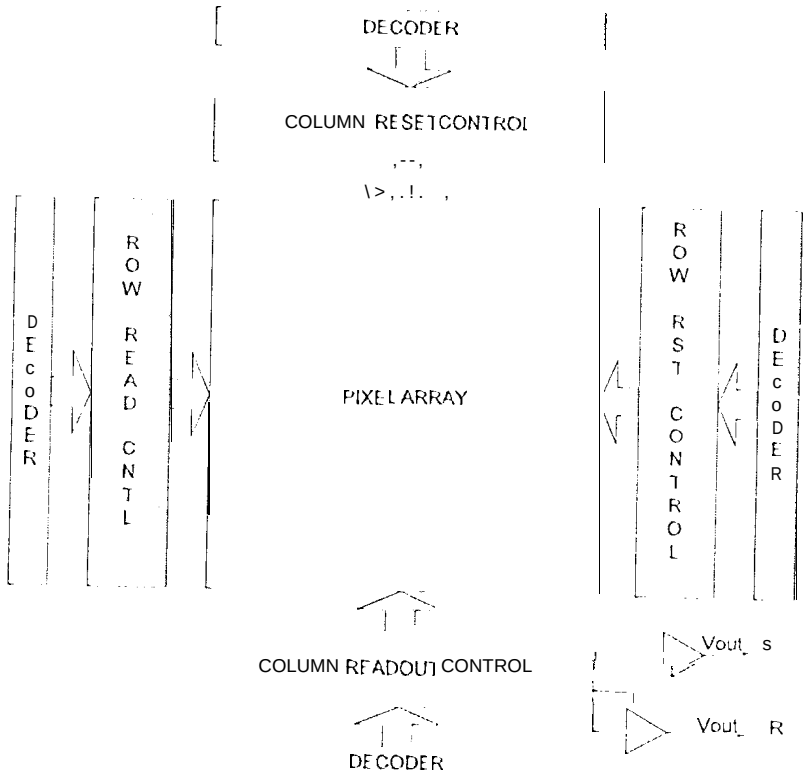

Fig. 3. Block diagram of implemented image sensor

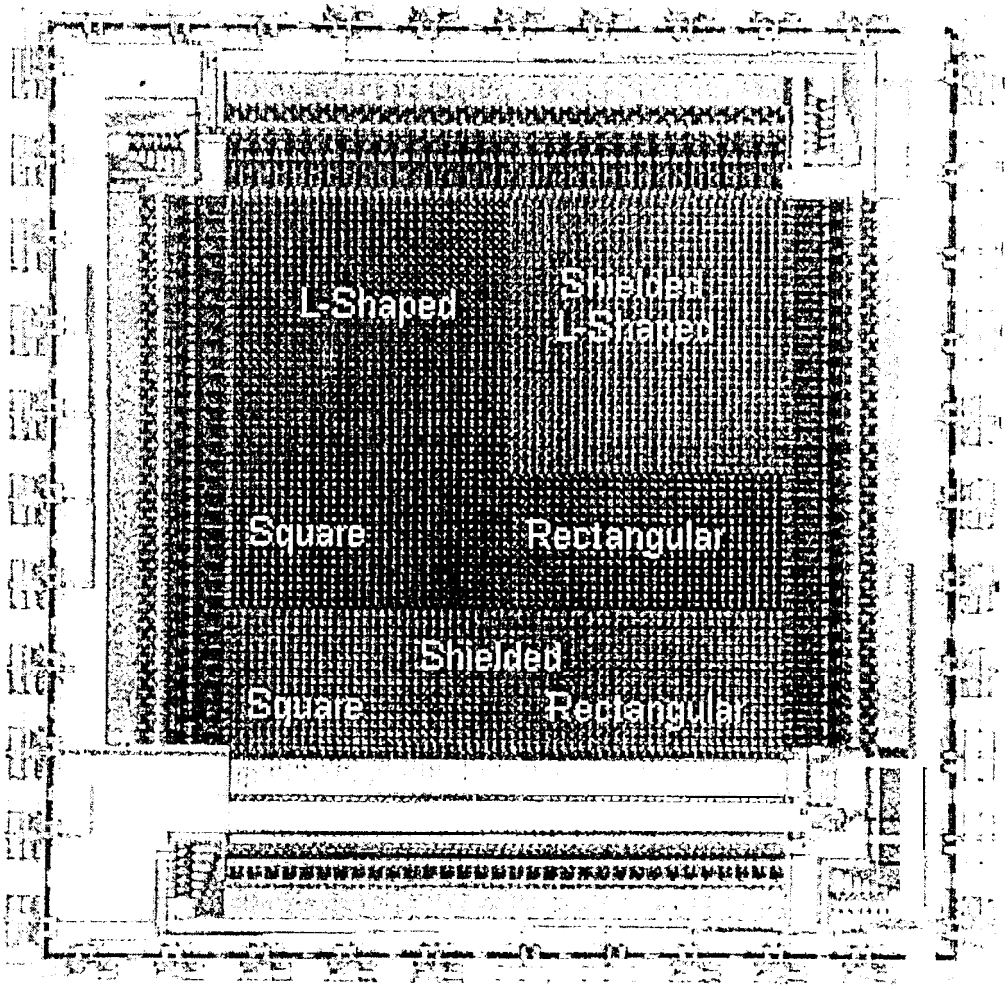

Fig. 4. Photograph of fabricated chip. Labels refer to pixel designs described in the text.

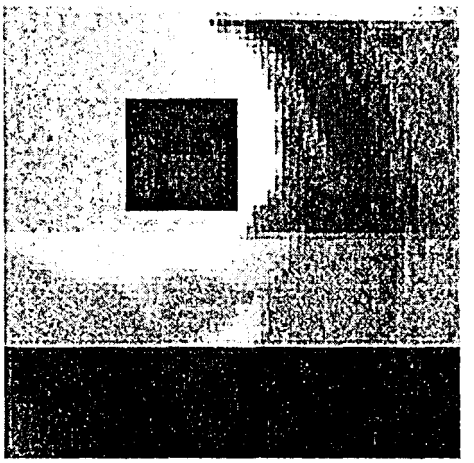

Fig. 5. Sensor output with region of short integration time through George Washington's eye

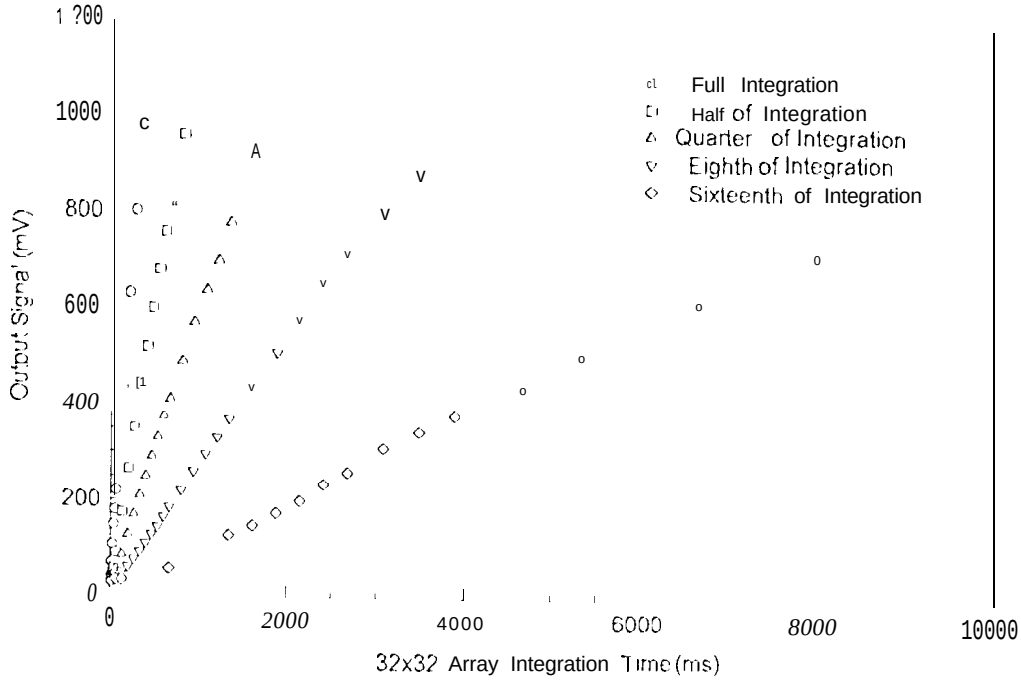

Fig. 6. Sensor output as a function of integration time for various exposure settings.

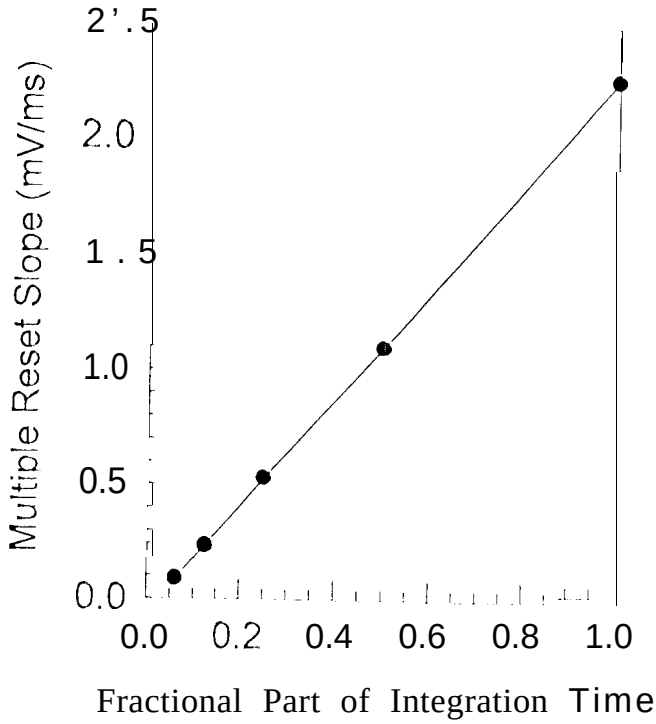

Fig. 7. Linearity of exposure control. Absolute vertical values depend on scene illuminance