THE NEW MILLENNIUM PROGRAM MICROELECTRONICS SYSTEMS ADVANCED TECHNOLOGY DEVELOPMENT

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Abstract

As part of the National Aeronautics and Space Administration's (NASA's) New Millennium Program, the Microelectronics Systems Integrated Product Development Team (11'1)"1) has developed a technology development roadmap for space exploration missions of the 2] st century. The IPDT, which consists of a broad range of government, industry, and university members, has considered the following technology areas: semiconductor technologies, computing technologies, storage technologies, input/output technology, 3D advanced packaging technologies, advanced power electronics technologies, and architectural system design and modeling technologies. The current industry and academia members of the Microelectronics Systems IPDT include Boeing, I Ioneywell, Loral Federal Systems, Lockheed Martin Corporation, Optivision, Space Compute.r Corporation, TRW, Georgia Institute of Technology, University of California-San Diego, ant] University of Southern California Government members include NASA, Massachusetts Institute of Technology Lincoln laboratory, Sandia National laboratories, and the U.S. Air Force. The current plans for a Flight One demonstration in fiscal year 1998 include. the flight of an integrated 3D microavionics set of multichip modules that implements the complete functionality of the spacecraft flight computer, solid-state recorder, high-bandwidth interface, and power electronics modules for the whole spacecraft. This set of modules is expected to weigh about 1 kg, which would represent more than an order of magnitude reduction in spacecraft mass relative to the state of the art.

1. Introduction

"1 he purpose. of the National Aeronautics and Space Administrat ion's (NASA's) Ne w Millenni urn Program (NMP) is to accelerate the. insertion of advanced space-related technologies into missions of the 21 st century, using three deep-space and three Earth-orbiting technology-validation spacecraft. By doing so, NASA is planning to enable a new vision of space exploration based on frequent, low-cost, miniat u rc scientific missions to the outer planets, as well as missions to Earth.[1,2]

The technology development and validation efforts of the N MP arc focused around six technology thrust areas: spacecraft autonomy, telecommunications, multifunctional and modular systems (MAMS), microelectromechanical systems (M EMS), instruments, and microelectronics systems. For each technology area, government- industry - academia learns have been formed, referred to as Integrated Product Development "l-earns (IPDTs). These teams operate in the form of government- industry consortia that develop and valid ate., in a cooperative and collaborative fashion, new enabling space-related technologies.

In Section 2, we introduce the scope of the Microelectronics Systems IPDT as well as its current membership. in Section 3, we summarize the results of the 11'1)-1" technology road mapping process, which will be described in detail in a subsequent publication currently in preparation.[3] in Section 4, wc. describe the technologies selected as well as the avionics architecture chosen for validation on the first NM}' spacecraft, to be launched in January 1998.

2. Microelectronics Systems IPDT Scope and Membership

IPDT Scope

The scope. of the Microelectronics Systems 1 PDT is broad, ranging from the lowest level (such as semiconductor materials, processes, ancl devices), to the highest level (such as spacecraft avionics systems). in between arc electronics circuits, components, functional modules, and subsystems for:

- Storage: static, dynamic, volatile, and nonvolatile.
- Processing: central processing units (CPUs), microcontrollers, special-purpose processors such as digital signal processors (DSPs), neural networks, systolic arrays, and other functional units such as field-programmable gate arrays (1 'PGAs).
- Input/output (1/0): serial and parallel interfaces for communication among components, modules, and subsystems, as well as communication with analog devices, sensors, and actuators.

in common to all of the above listed components is the need for a dramatic reduction in electronics mass, volume, and power dissipation, while maintaining the same growth trend towards higher functional density. That is, the NASA vision for space exploration in the 21st century requires the use. of low-power, miniaturized, highly capable, reliable, and yet low-cost space avionics systems.

IPDT Membership

In order to meet this formidable technological challenge, NASA has formed the.Microelectronics Systems government-irrdus[ry team. The government members arc. not only from NASA Centers (Goddard Space. Flight Center, Jet Propulsion Laboratory, and Lewis Research Center), but also from the Department of Defense U.S. Air Force Phillips Laboratory, Massachusetts Institute of Technology (MIT) Lincoln Laboratory, and Sandia National Laboratories. The industry partners include Boeing, 1 loneywell, Loral Federal Systems, Lockheed Martin, Optivision, Space Computer Corporation, and TRW. in addition, three university collaborators were chosen: Georgia Institute 01 Technology, University of California-San Diego (UCSD), and University of Southern California (USC). 'l-able 1 lists the names of the IPDT members, the organizations they represent, and the technology areas they were chosen 10 represent during the technology road mapping phase of the program development.

The following section summarizes the technology development roadmap that the IPDT developed during the six-month period May- November 1995. This technology roadmap will be published as a separate. document in the immediate future.

.3, The Microelectronics Systems Technology Roadmap

Before wc summarize the results of the roadmap, it is useful to discuss what is meant hereby a "roadmap" as well as the assumptions made during the road mapping process. A technology roadmap, according to the Microelectronics IPDT, consists of two parts:

- A proposed technology vision in terms of a set of enabling capabilities and associated metrics.
- A time-series of data points originating with today's state of the art, leading to the envisioned] capabilities of the future.

'1'here are many reasons for questioning the rationale, objectivity, and assumptions behind a roadmapping process performed by a selected few. It is therefore perhaps more appropriate to refer to the technology roadmap asa strategy for achieving a proposed vision. An excellent example of a recent road mapping activity, completed by the Semiconductor Industry Association (SIA), is documented as the 1995 *National Technology Roadmap for Semiconductors*.[4] This document was therefore used as a starling point for the Microelectronics Systems I }'1]"1' technology roadmap, which was divided into seven different categories, summarized as follows:

1. *Semiconductor* technology. The main goal here is to follow the impressive progress that commercial complementary metal- oxide semiconductor (CMOS) technology has been making with regard to the reduction of semiconductor feature size, density of integration, and power dissipation. In particular, the. usc of silicon-on-insulator (SOI) CMOS technology holds the potential for both low operating voltage (and thus low power) and radiation tolerance. For the purpose of roadmapping the. commercial semiconductor technology develop- rncnt, the SIA 1995 National I'ethnology *Roadmap for Semiconductors was* extensively used For example, 'I able 2 summarizes semiconductor technology evolution based on the expected reduction in feature size using advanced lithography processes.

Table 1. Ncw Millennium Program **Microelectronics** Systems **IPDT Membership**

Member	*Representing*	*Technology* Focus
Leon Alkalai, Co-1 .ead	NASA/JPL	Data processing; 3D packaging
Danny Dalton, G-lead	NASA/GSFC	Data processin; optical communication
Craig Keast	MIT Lincoln Laboratory	low-voltage semiconductors
Michael Knoll	Sandia National Laboratories	Semiconductor technology
Ron Marx	USAF Phillips Laboratory	Improved space computing
Jim Seeder	NASA/LeRC	Power electronics
Charles Chalfant	Optivision	Optoelectronic; M(Ms
Robert DeLean	Loral Federal Systems	PowerPC flight computer
Gerhardt Franz	Lockheed Martin Corporation	Power management; 3D packaging
John Samson	Honeywell Corporation	Magneto-re.sis[ivc RAM; RH-AS](; technology
Warren Snapp	Boeing	optics] 1/0; mixed-signal ASICs
Nick Teneketges	Space Computer Corporal ion	3D MCM packaging
Darby Terry	TRW	Solid-state recorders
Abhijit Chaterjee	Georgia Institute of Technology	Design for testability; low-power, low-cost packaging
Volkan Ozguz	UCSD	3D VLSI
Massoud Pedram	USC	Low-power synthesis

Table 2. **SIA** National **Technology Roadmap** for Semiconductors

Year of First DRAM Shipment	1995	1998	2001	2004	200-/	2010
Minimum Feature, µm	0.35	0.25	0.18	0.13	0.10	0.007
Memory —						
Bits/chip, DRAM/flash	64M	256M	1G	4G	16G	64G
Cost/bit @ volume, millicents	0.017	0.007	0.003	0.001	0.0005	0.0002
Logic, high volume: microprocessor --						
logic transistors/cm², packed	4M	7M	13M	25M	50M	90M
Bits/cm², cache SRAM	2M	6M	20M	50M	100M	300M
Cosl/transistor @ vol umc, mill licents	1	0.5	0.2	0.1	o.05	0.02
Logic, low volume: ASIC --						
Transistors/cm², auto layout	2M	4M	7M	12M	25M	4 0M
Nonrecurring engineering cost/transistor, millicents	0.3	0.1	0.05	0.03	0.02	0.01
'On-chip *clock, cost-performance* --	150	200	300	400	500	625
On-chip lock, high-performance	300	150	600	800	1000	1100
Chip-to-board speed, high-performance.	150	200	250	300	375	475
Chip size, *mm²* --						
DRAM	190	280	420	640	960	1400
Microprocessor	250	300	360	430	520	620
ASIC	450	660	750	900	1100	1400
Power supply voltage, V --						
Desktop	3.3	2.5	1.8	1.5	1.2	0.9
Bat tcry	2.5	1.8- 2.5	0.9- 1.8	0.9	0.9	0.9

2. *Processors. in the* area of general-purpose processors, a long-term decision was made to use commercial instruction set architectures for space applications. in particular, the PowerPC architecture was selected because of its widespread use, availability of commercial off-the-shelf (COTS) software, and development tools. For special-purpose processors, digital signal processors were roadmapped for future applications, as well as arrays of DSP for high-performance onboard computing applications.

3. Storage. low-power, high-capacity storage using commercial parts --- such as dynamic random access memory (DRAM) for volatile and flash for nonvolatile memory — was chosen as an enabling technology for future space applications. The roadmap actually includes many other magnetic storage technologies such as VBL, MRAM, FeRAM, etc. Nonvolatile holographic storage is also part of the future roadmap.

4. *I/O.* 1 ligh-bandwidth, low-power I/O technologies were i dent i fied as enabling for both deep-space ancl Earth-orbiting missions. For deep space, 1-20 Mbps fiber-optic networks are envisioned; for Earth-orbiting, missions, 1–2 Gbps fiber-optic data buses using asynchronous transfer mode (ATM) technology arc cons dered d.

5. *Packaging.* Advanced 3D microelectronics packaging is a major enabling technology for the dramatic reduction in spacecraft mass and volume. In this area, 3D multichip module (MCM) stacking technology using vertical elastomeric interconnects is the proposed first step, followed by 3D high-density interconnect (1 IDI) technology, and finally, 3D very large-scale integration (VLSI) technology, which reaches the physical limits of electronics device integration into the third dimension.

6. Engineering *design* automation *(EDA).* In this field, the use of high-level design tools, formal verification methods, and executable design specification were elements of the technology roadmap. Moreover, low-power synthesis tools were chosen as the first step towards using EDA tools to reduce the overall spacecraft electronics power.

7 Power *electronics.* "l-he power electronics technology (which does not include power sources) is divided into two areas: power conversion using DC/DC converters, and power activation and switching modules (PASMs). 'I'he first develops the high-efficiency, highl y i ntegrated power conversion tech - nology, and the second encompasses integrated mixed-signal technology for power switching.

4. NMI' Deep-Space 1 Microavionics Architecture

The proposed spacecraft rnicroavionics architecture for the first NM]' mission (DS1) evolved from the technologies specified in the above summarized roadmap. The architecture is shown in Figure 1. The architecture consists of four avionics modules that communicate over a standard avionics backplane bus, VMI: (VersaModule Eurocard). The first module includes the 32.-bit reduced instruction set computing (RISC) processor, 2 ~;bitsofsolid-slate recorder (SS1<), 160 Mbytes of extended memory using 31) die stacks, and fiber-optic I/O links for communication with the spacecraft. Also shown in Figure l is a separate passive star-coupler used for intermodule communication using fiber-optic links.

The second and the third modules represent the power electronics DC/DC converter and the PASM, and the fourth module contains several microelectronics experiments for both low-power and 3D VLSI validation in space. The principal invest igators of these experiments arc Georgia Institute of Technology, MIT Lincoln Laboratory, UCSD, and USC. A more detailed block diagram of the proposed DS1 microavionics architecture is shown in Figure 2.

Of particular interest to the NMP Microelectronics IPDT was the design of a stand ard, low-cost spacecraft architecture, which is discussed below.

Design for Low Cost

Since an important aspect of the NMP is to develop and accelerate the insertion of advanced space technology for the low-cost exploration of space, it is interesting to note the Microelectronics Systems IPDT approach towards this goal. From Figure 2, it is evident that the proposed architecture will achieve low recurring cost due to the following important attributes, which were set as guiding principles up front:

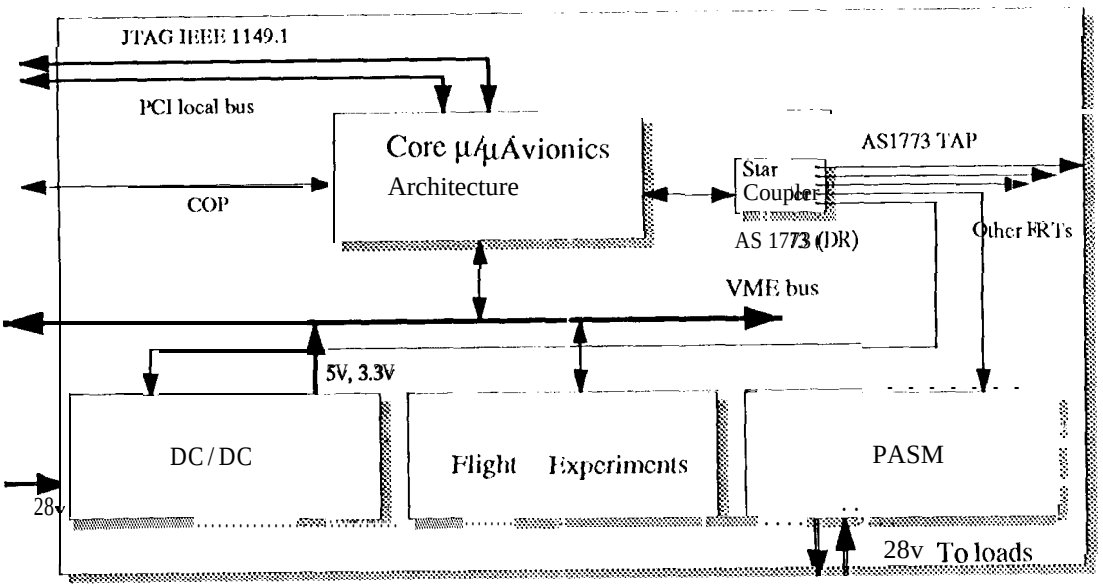

Figure 1. Deep Space Flight 1 Core Microavionics High-Level Architecture

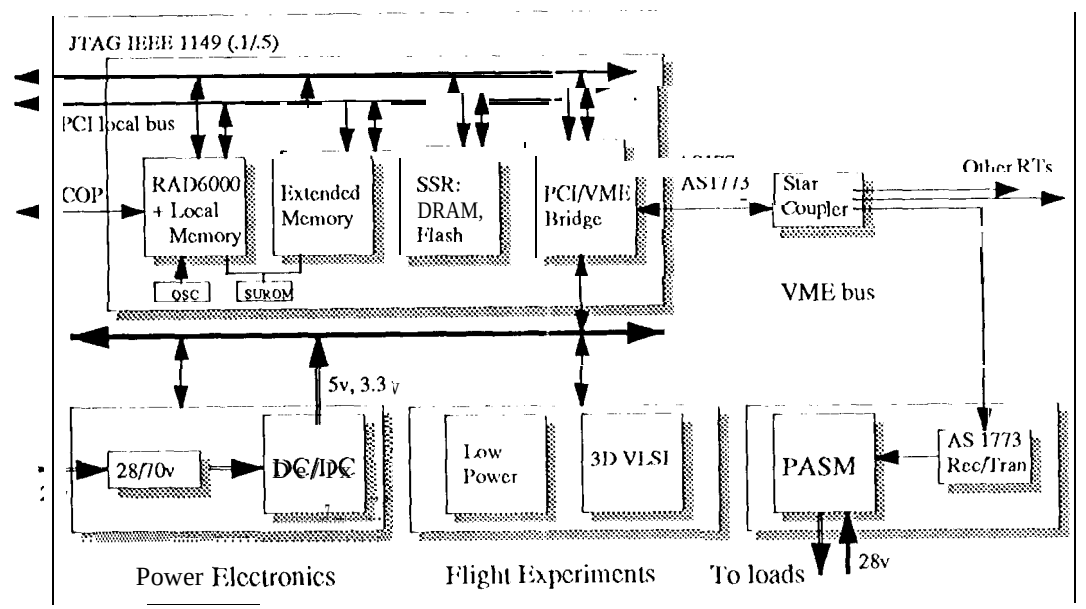

Figure 2. Core Microavionics Architecture — Detail

1. Components with commercial heritage.
2. Standard interfaces.
3. Commercial software development platforms.
4. Scalable architecture.
5. General purpose design.

Commercial heritage. The proposed NMP architecture uses components with commercial heritage as the first choice, rather than space-unique flight hardware or software. This is best illustrated by the following examples. First, the processor selected for the NMP long-term roadmap is the PowerPC architecture (604 in particular), which is widely used in commercial industry. Moreover, NASA is collaborating with the U.S. Air Force Phillips Laboratory to ensure the transfer of the commercial IBM PowerPC fabrication line to a radiation-hardened process at the Loral Federal Systems Division. Second, TRW is developing the SSR module, using exclusively commercial 16-Mbit DRAM and 16-Mbit flash die, stacked in 3D to achieve high volumetric efficiency of silicon.

Standard interfaces. W-haps even more important than the use of commercial components wherever acceptable, it is important to use standard interfaces for intermodule communication, system testing, etc. in the DS1 architecture, the following standard interfaces are being used:

VME	Avionics standard backplane subsystem bus
PCI	Peripheral component interconnect, a commercial local bus standard
JTAG	IEEE 1149.1 Standard Test Access Port architecture
AS 1773	Avionics standard serial fiber-optic bus: dual rate and dual redundant

Commercial software development platform. The runtime environment of the proposed DS1 architecture includes the commercial VxWorks operating system, the C programming language and compiler, and a set of off-the-shelf development tools that operate on Unix workstations. Therefore, many program development and software debugging tools are available for this development environment and prototyping platform.

Scalable, distributed architecture. Having an architecture that scales is attractive since it can potentially address a broader community of users, and thus further reduce the overall recurring cost and further amortize the nonrecurring cost. Moreover, applications such as onboard spacecraft autonomy and onboard science data analysis require higher degrees of onboard computing capabilities than can be offered by any single processor. Therefore, a multiprocessor architecture that can offer higher computation throughput and higher degrees of system reliability (due to redundancy) is extremely attractive.

A simple extension of the proposed DS1 NMP avionics architecture towards a distributed architecture is shown in Figure 3. In this architecture, single avionics nodes like the one previously detailed are connected over a spacecraft local area network (LAN), which can be either the currently used AS 1773 bus or the future roadmapped high-bandwidth fiber-optic data bus **(1'01)11).** An architecture like this is attractive for the following reasons. First, it is simple. It resembles a distributed LAN architecture that most engineers understand and use in their office environments. Second, it is a simple extension of the single-node architecture, where information between nodes is exchanged via message-passing protocols. Third, it enables higher levels of system reliability due to the possibility of system-level redundancy; that is, if one node fails, any other node can pick up the load and continue operating. Finally, this architecture is attractive since it is easy to emulate. In fact, a PowerPC workstation on a LAN is already most of what an engineer needs to start prototyping a target system.

General purpose. The proposed DS1 architecture was not intended to be unique for any specific type of space mission, but in fact general purpose and applicable to deep-space and Earth-orbiting missions, planetary probes, microscience stations, and landers.

5. Detailed Technology Description

In this section, we present a more detailed view of the specific technology slices that are being integrated into the spacecraft 3D microavionics architecture. These slices (a total of four) are:

- Processor module.
- Extended memory module.
- SS1< module.
- I/O module.

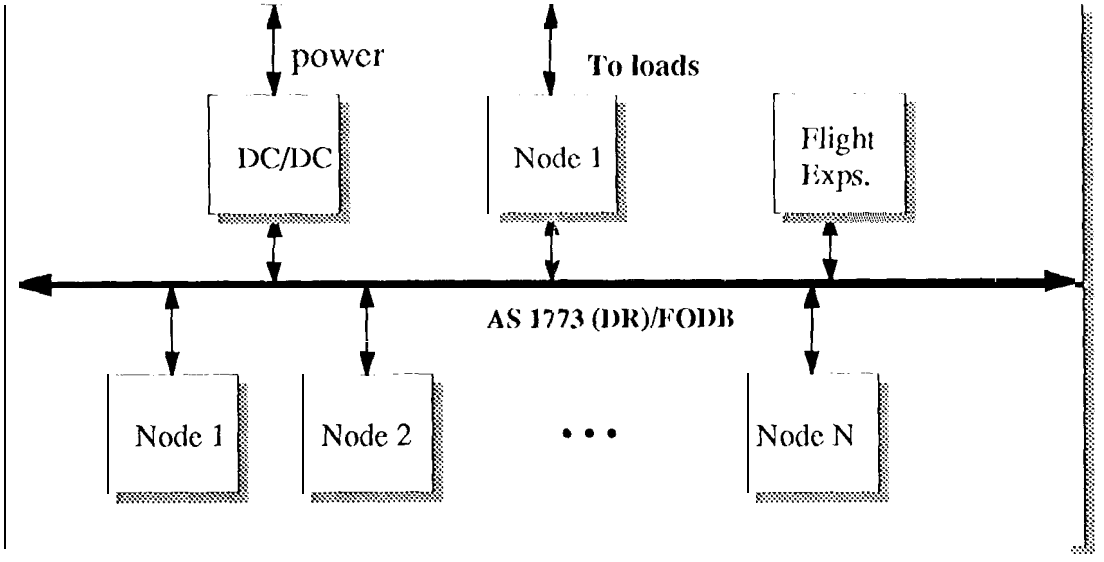

Figure 3. New Millennium Microelectronics Systems Distributed Architecture

All four modules are stacked together using a low-cost, flexible, MCM stacking technology.

Processor Module

The processor slice consists of two MCMs: a RAD6000 I SA processor module designee] for lock-step-compare, and a high-bandwidth memory module.. Both modules use only radiation-harde ned components and arc. packaged in 308-pin CQF packages. The MCM technology used is an MCM-D technology referred to as vertical chip on silicon (VCOS). The die attach process is flip-chip, which has been used extensively by Loral. Both MCMs are shown in Figure 4.

Extended 3D Memory Module

The extended 31) memory module provides 160 Mbytes of directly addressable l) RAM space to the flight computer. This amount of storage is achieved within a very small volume and footprint by using advanced 3D die stacking technology, as shown in Figure 5. Two stacks are actually included in the same MCM together with a D RAM controller module..

I/O Module

The I/O module (Figure 6), designed by Boeing, include.sail the interface logic needed to translate from the VME to the PCI local bus, and from the PCI bus to the spacecraft serial bus, the AS 1773. The. interface logic is packaged in a single MCM without the actual physical t rar isceivers, which arc outside the actual MCM. The MCM technology used is MCM-C (or thick film ceramic technology).

Solid-State Recorder Module

The SSR module (Figure 7) by TRW uses aggressive 3D stacking techniques to achieve high levels of integration. The SSR has a total of 2 Gbits of storage.: half is DRAM-based and half is flash-based. 'l-he proposed combination meets the spacecraft system requirements for nonvolatile and volatile storage.

3D Multichip Module Stacking Technology

The proposed 3D MCM packaging technology has been developed and prototyped by Space Computer [corporation, a small business in Santa Monica, California. As shown in Figure 8, MCMs are mounted on printed circuit boards, which are then stacked in 31), using elastomeric devices with embedded wires for inter–MCM communication.

The four spacecraft avionics slices are. integrated into a single four-layer system, which is then mounted onto a VME board for further integration into the avionics electronics module, and subsequently integrated into the. 1)S1 spacecraft.

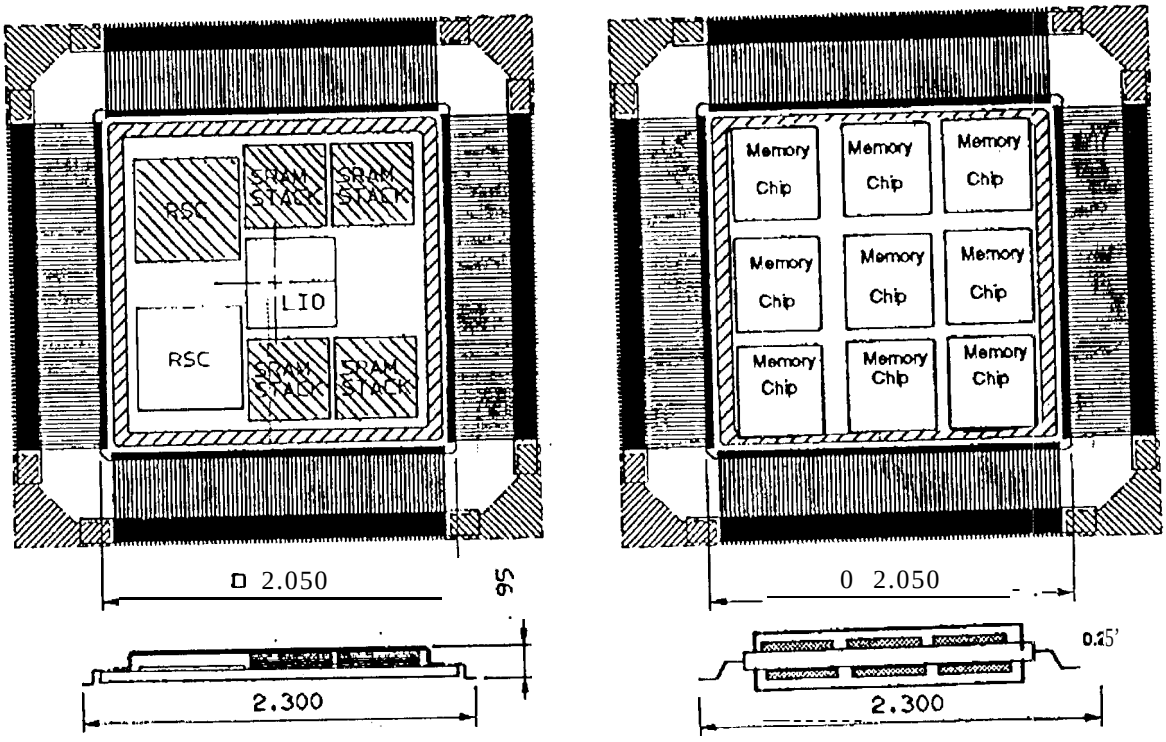

Figure 4. Processor Slice Multichip Modules

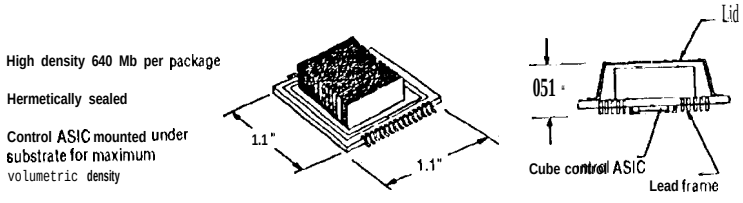

Figure 5. Extended 3D Memory Module

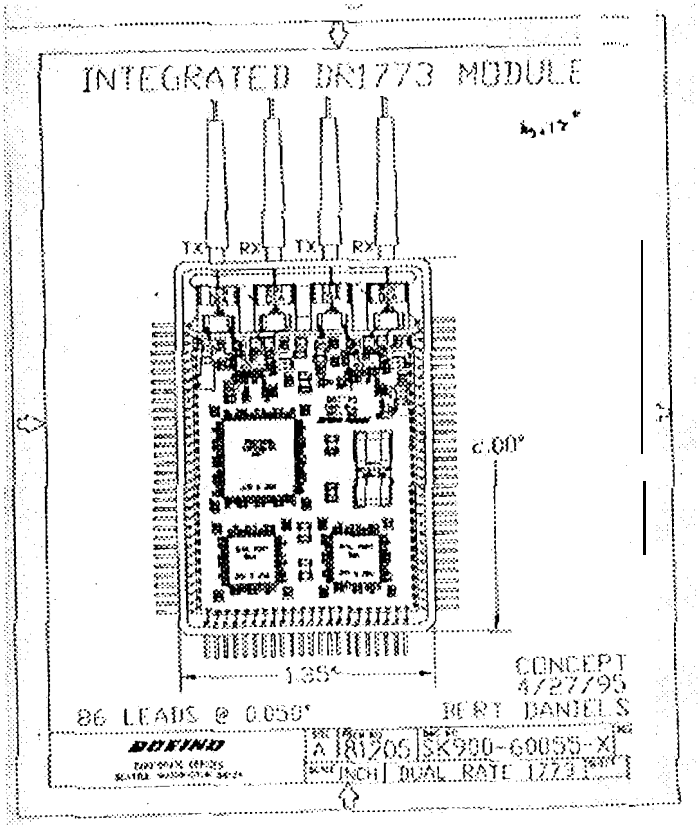

Figure 6. Input/Output Module

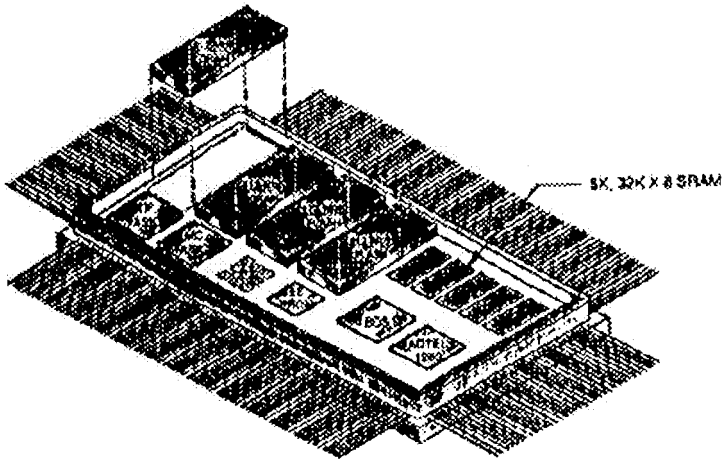

Figure 7. Solid-State Recorder Module

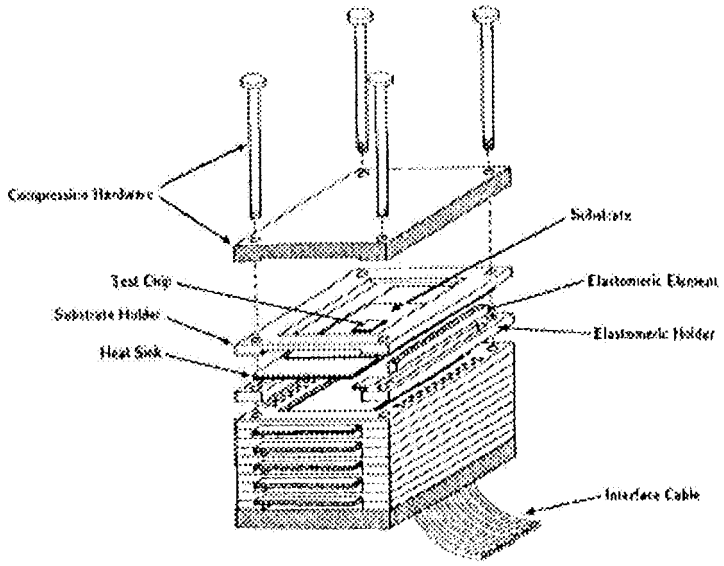

Figure 8. MCM Stacking Technology

6. Conclusions

We have summarized the results of the technology roadmapping effort performed by the NMP Microelectronics IPDT during the five-month period May-November 1995. As a result of this roadmap, a low-cost, 3D microavionics architecture has been proposed that uses only existing and commercially acceptable standards for inter-module interfaces. This highly integrated module will provide the main spacecraft control and data handling functions for the first NMP deep-space mission. Moreover, the architecture is general, and can be used for Earth-orbiting missions as well as for other space-related applications, such as commercial remote. sensing and global communication.

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