

A CMOS IMAGER WITH ON-CHIP VARIABLE RESOLUTION FOR LIGHT ADAPTIVE IMAGING

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ABSTRACT

A variable resolution CMOS active pixel image sensor that enhances S/N ratio at low illumination level is presented. It features column-parallel circuits for signal summation from kernels of programmable size. The 128x128 prototype array consumes only 24 mW at 125 frames/see. and demonstrates more than 10 dB S/N enhancement for 2 x 8 kernel summation. Fixed pattern noise is less than 0.5% of the full well signal.

CMOS active pixel image sensor (APS) has attracted much interest in recent years [1]. In addition to the obvious advantages of lower power consumption and system miniaturization through camera-on-a-chip implementation [2], CMOS APS enables development of smart **imagers** by integrating custom CMOS signal processing circuits on the focal plane. In this paper, we present a CMOS APS **imager** that is capable of enhancing signal to noise ratio (S/N) under low illumination through summation of signals from neighboring pixels. On-chip S/N improvement in CMOS APS has already been demonstrated by pixel averaging [3] or by pixel binning. Pixel binning has been implemented in a CMOS APS primarily designed for **frame-transfer** operation [4]. However, that implementation suffered *from extraneous* noise pick-up and high residual fixed pattern noise (**FPN**) due to the use of single-ended column **integrator** circuit. This paper presents an APS with improved kernel summing circuits implemented in **fully differential** topology. As a result, the **imager** performance is improved by greatly reducing the **FPN** and temporal circuit noise. This multi-resolution APS will find ready applications for light level adaptive imaging.

Figure 1 shows the schematic of the multi-resolution chip. The column integrator array performs parallel signal summation for different rows. The summed signals are stored in the column memory capacitor bank. The global output integrator carries out the column-wise signal summation. Row and column decoders are used for randomly addressing the sensor array and for programming the size of the summation kernels. The schematic circuit diagram of the entire signal chain from the sensor pixel to the output of the chip is shown in Figure 2. The sensor uses a photogate APS pixel design [1]. The column circuits consists of a fully differential switched-capacitor integrator, a pair of

column memory capacitors, **CLR** and **CLS**, and the MOS switches needed for the integration operation. The sample and hold capacitors, **CMR** and **CMS**, for the pixel reset and signal levels serve as the input capacitors for the column integrator. The column memory capacitors, **CLS** and **CLR**, are the input capacitors for the output integrator. The output integrator uses two matched single-ended two-stage opamps. They are designed to drive 30 **pF** and 1 **MΩ** load at above 8 **Mpixels/sec.** required for 30 **frames/sec.** readout of a 512 x 512 element array. The column opamp is a folded cascode opamp with switched capacitor common mode feedback circuit. It operates at much lower speed due to the column parallel readout. The designed 2 MHz unit gain frequency and 60 **dB** DC gain are sufficient for column parallel integrator settling with better than 9-bit accuracy. The amplifier design is optimized to use minimum transistor size and lowest bias current.

For a $n \times m$ (n columns and m rows) kernel summation **readout**, signals from m rows of the sensor pixel are integrated by the column integrators one row at a time. The reset and signal levels of each row are first sampled on the S/H capacitors **CMS** and **CMR** as the integrators are reset. They are then differentially integrated on the integrating capacitors **CIS** and **CIR**. This process continues **until** all the rows in a given kernel are summed. The integrated signals are sampled and held on the column memory capacitors **CLS** and **CLR**. After the row summation is completed, every n consecutive columns are integrated after each reset of the global integrator. The summed signals from $n \times m$ kernels are read out serially from the output of the global integrator. The summation kernel size is programmable according to the illumination condition. By using a square kernel size of $n \times n$, the S/N enhancement is \sqrt{n} . At low illumination, S/N enhancement is greater than \sqrt{n} since the circuit read noise dominates in the **imager** noise.

The column-wise FPN is mostly caused by the column opamp offset. In the **fully** differential readout, the offset is first sampled on the feedback capacitors as the integrator is auto-zeroed. To first order, it is compensated at each step of signal integration. Clock feedthrough appears as common mode pulse to the integrator and does not contribute to FPN. Residual FPN is due to the capacitor ratio mismatch on the two sides of the integrator and is given by,

$$V_{0s,0} = m(\alpha_R - \alpha_S)V_C = m\Delta\alpha V_C \quad (1)$$

where **m** is the number of row summation, $\Delta\alpha$ is the mismatch in capacitor ratio and V_C is the common mode voltage. The temporal read noise consists of noise from the pixel, the detector shot noise, noise associated with switching (**kTC** noise) and noise from the Opamps. The output refined noise for $n \times m$ kernel summation can be approximated by,

$$\langle V_\delta^2 \rangle \approx n \frac{2kT}{C_M} \alpha^2 \{ 2m\alpha^2 + \alpha + 3\beta + 2m(1 + \alpha)\beta + mg^2 \bar{N} \} \quad (2)$$

where $C_{MR} = C_{MS} = C_M$; $C_{IR} = C_{IS} = C_I$; $C_{LR} = C_{LS} = C_L$; $C_{OR} = C_{OS} = C_O$; $\alpha = \frac{C_M}{C_I} = \frac{C_L}{C_O}$;

$\beta = \frac{C_M}{C_L}$; g is the conversion gain measured in volts/electrons; and \bar{N} is the average

number of electrons per pixel during a single exposure. The noise voltage at full resolution readout is estimated to be about 320 μV for 125 frame.skec. image readout rate, which is very close to the measured value.

A 128 x 128 prototype sensor was implemented by using a 1.2 μm single poly, double metal, n-well process with linear capacitor option. The sensor pixel size is 24 μm x 24 μm with an optical fill factor of 29%. The column circuit is laid out in the 24 μm

column pitch and has a total length of about 0.9 mm. The total chip area is about 4.7 mm x 5.2 mm. Figure 3 shows the chip layout.

The fabricated parts were tested up to 125 **frames/sec**. Figure 4 is a **full** resolution image taken at 100 **Kpixels/sec** readout rate. The tested readout speed was limited by the capability of the pulse generator and the data acquisition board used in the test bed. The characterization results are summarized in Table 1. The sensor demonstrates 1.2 V saturation signal, 72 **dB** dynamic range and 8.3 $\mu\text{V}/e^-$ conversion gain. The FPN is about 6 **mV** (0.5% saturation), read noise 300 μV and dark current 0.6 nA/cm^2 . More than 40% of the total 24 **mW** power is consumed by the global integrator opamps due to the required driving capability. Images **shown** in Figure 5 demonstrate the signal enhancement as the summation kernel changes from **1 x 1** (no summation) to 2 x 2 and to 4 x 4. As the summation kernel size increases, both the signal amplitude and the image contrast increase. Figure 6 shows the detailed measurement for the signal and S/N enhancement as the kernel size is increased from 1 x 1 to 2 x 8 at constant illumination and exposure time. The output signal linearity over 1.2 V range indicates good accuracy of the row and column summation. A 11 **dB** S/N improvement is achieved, as expected by the theoretical prediction from Equation 2.

In conclusion, a multi-resolution APS for light adaptive imaging applications has been demonstrated by successfully integrating fully differential opamp based integrator circuits. Good uniformity and low readout noise was achieved. Enhancement of S/N ratio at low light level was demonstrated by programmable multi-resolution readout at constant frame rate.

The research presented in this paper was carried out by the Center for Space Microelectronics Technology, Jet Propulsion Laboratory, California Institute of Technology, and was supported by the National Aeronautics and Space Administration Office of Advanced Concepts and Technology.

Reference:

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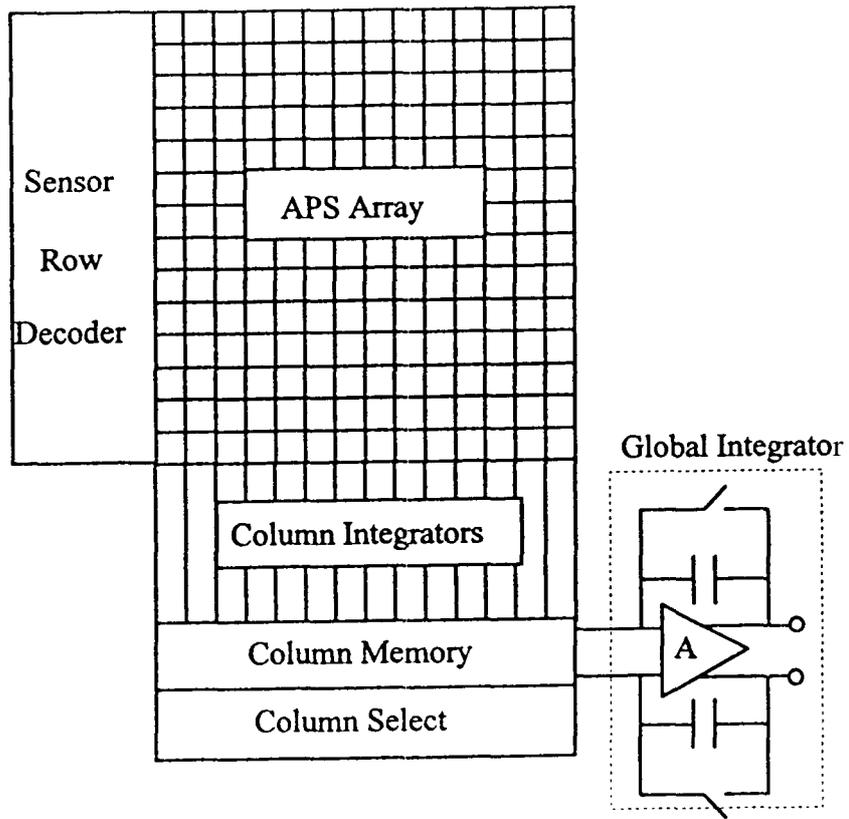


Figure 1- Schematic of the multi-resolution APS imager.

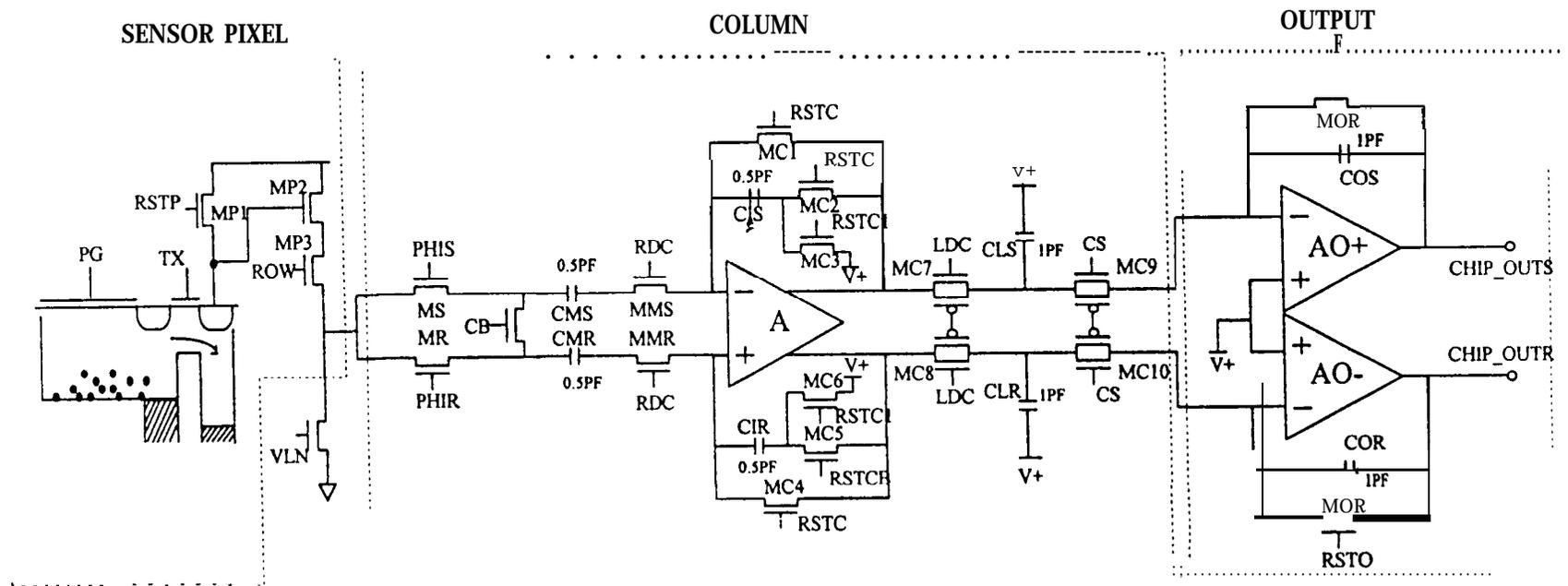


Figure 2- Circuit schematic of the complete signal chain of the image sensor.

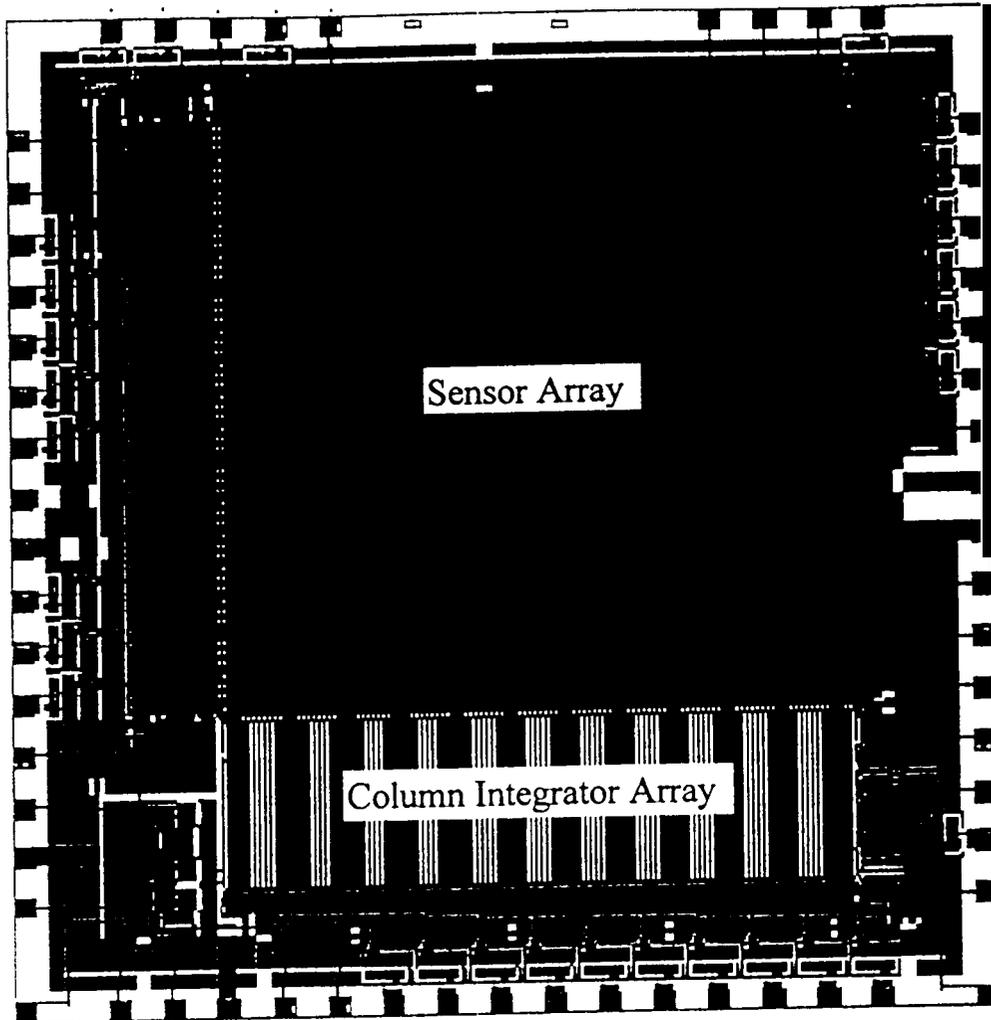


Figure 3 - Sensor chip layout.



Figure 4- Row image at full resolution at 100 kPixels/sec.

Table 1- Summary of the test results.

Imager format	128 X 128
Integrator linearity:	better than 8 bit out of 1.8 V swing
Sensor saturation:	1.2V
Temporal Noise:	303 $\mu\text{V r.m.s.}$
Dynamic range:	72 dB (disregarding FPN)
Conversion gain:	8.3 pV/e ⁻
Power consumption:	24 mW @ 125 frames/sec.
FPN:	6 mV
Dark current:	54 mV/sec. (0.6 nA/cm ²)

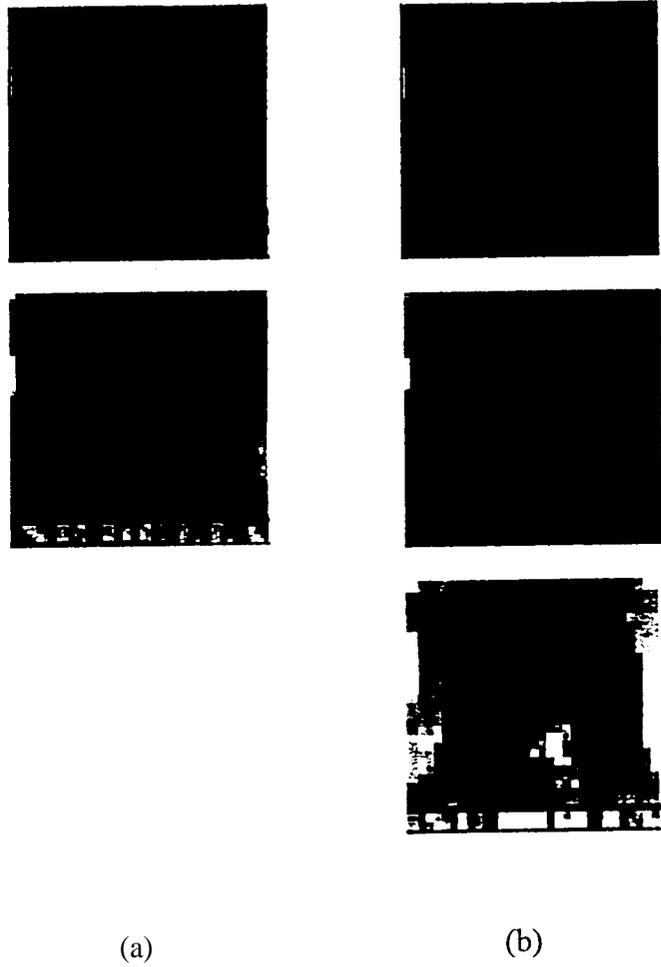
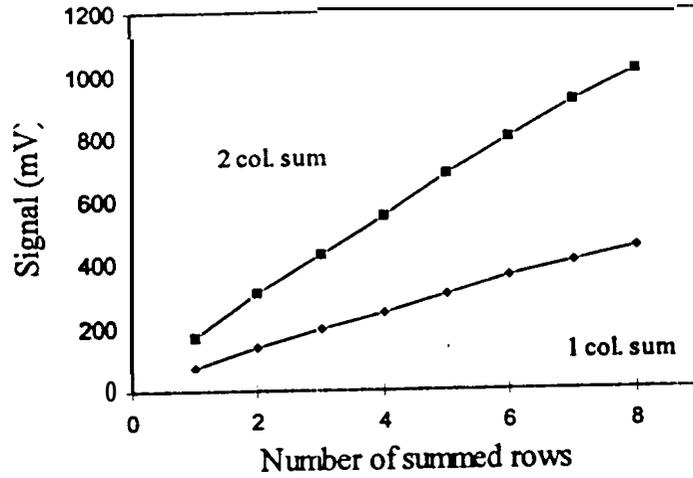
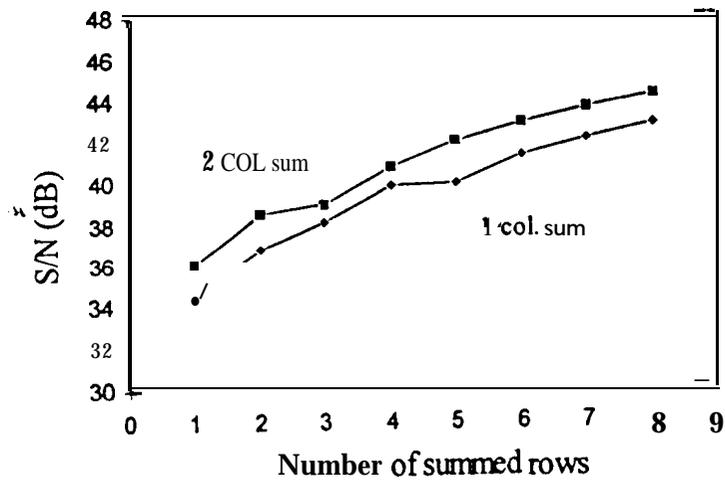


Figure 5- **Image taken** for summation kernel of 1 x 1, 2x2, and 4x4 at two (a and b) different illumination level.



(a)



(b)

Figure 6- (a) Signal, and (b) S/N as a function of column and row summation for constant illumination.