The following is the abstract of my presentation that will be made at the following three professional forums:

1. Presentation to the Los Angeles Chapter of the IEEE Professional Society, November 1997.
2. 3D Packaging Workshop, October 13,1997, Philadelphia, PA
3. SPIE - The International Society for Optical Engineering, January 24-30, 1998, San Jose, CA

Advanced Computing Technologies for Future Deep Space Exploration Missions

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For the past five years, several research and development programs at NASA's Jet Propulsion Laboratory have pursued the goal towards Faster-Better-Cheaper space exploration missions, by attempting an aggressive reduction of the total spacecraft mass, volume, power, as well as system cost, by explicitly targeting the spacecraft's microelectronics and computing systems. A detailed study performed in 1993 for the Mars Pathfinder mission, showed that by reducing the mass, volume, and power of the Attitude and Information Management (AIM) subsystem by a factor of 3x from 42kg to 14kg, using the 1995 technology freeze date, would reduce the total spacecraft mass by 200kg. Such mass savings would reduce the total spacecraft cost, but, would also enable new mission concepts that were being considered for a more comprehensive, and distributed exploration of Mars using multiple science stations, or rovers.

In 1995, as part of NASA's Advanced Flight Computing program (AFC), a highly integrated flight computer was prototype in partnership with industry. This AFC 32-bit computer used advanced microelectronics Multichip Module (MCC), as well as 3D die-stacking technologies to package a total of 33 die in a single package weighing less than 100 grams (89 grams). This module was also delivered as part of the Advanced Packaging Experiment (APEX) to the Lewis Small Satellite Technology Initiative (SSTI)) spacecraft, launched in August 1997.

From 1995-1996, as part of NASA's New Millennium Program to validate advanced technologies for future space missions, a consortium of team members from government, industry, and academia, prototype a highly integrated microelectronics computers system, referred to as the 3D Stack. This effort extended the work of the AFC program towards stacking Multichip Modules (3D) in the Z-axis. Four modules (slices) were stacked: 32-bit RAD6000 processor and PCI bus interface; 320 Mbytes of Local Memory; 128 Mbytes of non-volatile Flash Memory; and a I/O module implementing the PCI to VME bridge, as well as the interface to the 1773 fiber-optic 20 Mbps serial bus. This 3D stack computer can either be used as a stand-alone computer module, or as a node in a distributed architecture. Such an architecture can be used to implement distributed fault tolerance techniques for highly reliable systems.

Finally, throughout 1997, and with a new start in (fiscal) 1998, research at NASA's Jet Propulsion Laboratory plans to integrate the complete spacecraft microelectronics system, into a single integrated 3D architecture that will be based exclusively on advanced microelectronics technologies. This work is being performed at the newly formed Center for Integrated Space

Microsystems (COE), a NASA and JPL Center of Excellence, and within the Advanced Deep Space System Development Program (a.k.a. X2000). The goal of this new program and center is to aggressively pursue the development of a new spacecraft bus architecture that will serve the needs of future low-cost deep space missions. Explicit customers of this program include:

1. Ice and Fire Program: missions to Pluto and Kuiper Belt; Europa Orbiter; and Solar Probe.

2. NMP: Deep-Space 3 mission for space interferometry; Deep-Space 4 mission for a Comet Sample Return.

3. Mars Exploration Program: including the Mars Sample Return.

All of the above missions are looking at launch opportunities in the 2002 (or soon thereafter) time frame.

The explicit charter of both the X2000 Program and the CISM Center of Excellence, is to look at enabling space technologies that also extend beyond the first line of customers and the 2002 time frame. The current portfolio of research elements planned within CISM include (but are not limited to) the following:

- Technologies for the development of highly integrated and modular 3D avionics system.
- Distributed Reliable Computing.
- Improved system reliability using Commercial Off The Shelf (COTS) technologies.
- Systems On A Chip (SOAC) research and development.
- Opto-Electronics, optical storage, processing and communication.
- Nano-technologies: structures and devices
- 3D VLSI technologies for increased volumetric density of computing devices.
- Quantum Functional Devices.
- Reconfigurable Computing.
- Evolvable Computing.
- Biological Computing Concepts.
- Quantum Computing Technologies.