Readout Characteristic of Integrated Monolithic InGaAs Active Pixel Sensor Array

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ABSTRACT

A newly fabricated Monolithic InGaAs Active Pixel Image Sensor[1,2] is presented, and its readout characteristics are described. The sensor is fabricated from InGaAs epitaxially deposited on an InP substrate. It consists of an InGaAs photodiode connected to InP depletion-mode Junction field effect transistors (JFETs) for signal buffering, selection and reset. The monolithic sensor eliminates the need for hybridization with a silicon multiplexer, and in addition, allows the *sensor* to be front illuminated, making it sensitive to visible as well as IR radiation. With further development, the sensor is ideal for dual band (Visible/IR) applications, including optical communication. It is also well suited to applications requiring near room temperature, broad band *response* such as for atmospheric gas sensing and target identification.

Two different types of small 4x 1 test arrays have been fabricated. One is a source follower per detector architecture. Here the signal charge is integrated on the photodiode capacitance. The photodiode is connected to a gate of a JFET configured as a source-follower, which buffers the photodiode voltage. The other test circuit uses a capacitive transimpedance amplifier. This circuit contains an inverter using an input JFET with a passive JFET load. The photodiode is connected to the JFET gate. A feed back capacitor causes the circuit to act as an integrator, while keeping the diode input bias relatively constant. Both circuits atso contain JFET switches for reset and selection. Selection connects the output of the chosen cell onto a common output bus.

The other test circuit uses a source follower per detector architecture. Here the signal charge is integrated on the photodiode capacitance. The photodiode is connected to a gate of a JFET configured as a source-follower, which buffers the photodiode voltage, Both circuits also contain JFET switches for reset and selection. Selection connects the output of the chosen cell onto a common output bus.

In this exploratory development effort, the effectiveness of these two different readout circuits will be discussed in terms of leakage, operating frequency, and temperature. These results then will guide for the second phase demonstration of integrated two dimensional monolithic active pixel sensor arrays for application in transportable shipboard surveillance, night vision and emission spectroscopy.

Keywords: Readout circuits, Dual (Visible/IR) responses, Monolithic, Active pixel sensor.

1. INTRODUCTION

Infrared focal plane arrays (IR FPAs) have a wide range of industrial, scientific and military applications.’’” In general, an IR FPA consists of an array of infrared-sensitive photodiodes and associated readout electronics capable of converting, amplifying, buffering and multiplexing the signal charge from the diode array.

In a typical IR FPA area array, the diode array is fabricated from a narrower bandgap film in the 111-V or II-VI material system such as HgCdTe, InGaAs, or InSb, epitaxially deposited on the front surface of a wider bandgap II I-V or II-VI substrate, such as HgZnTe, GaAs, or InP.

This diode array chip is then "flipped" and bump-bonded with the patterned surface down, substrate up, to a separate readout chip. Ibis readout chip is nearly always formed from silicon CMOS, because of the high maturity of this technology. Silicon circuits of great complexity can easily be designed and simulated, since highly sophisticated tools are available for this purpose. Commercial foundries arc available to produce the chips relatively cheaply, and with high yield. This hybrid structure consisting of a diode array chip bump-bonded to a silicon CMOS readout has worked well, and has been exploited in IR FPAs spanning the wavelength range from 100 to 1 μm.

This approach is not without its problems, however, and especially for special applications, there is a need to explore alternatives. First, the hybridization adds steps to the sensor fabrication sequence that are expensive and can be tricky. Second, the coefficient of thermal expansion (CTE) of silicon is anomalous with respect to virtually every other semiconducting materials system. Since IR FPAs usually must be cooled for optimum performance (in order to reduce dark current), this difference in CTE's causes a mismatch in the thermal expansion between the detector and readout chips, straining the electrical bonds between the chips. While the use of soft iridium bumps has helped accommodate this strain, the CTE mismatch limits array sizes and reduces reliability, especially if thermal cycling is involved.

Perhaps more importantly, the standard hybrid approach is necessarily a back-illuminated design, and incoming optical radiation must pass through the substrate of the detector array. The bandgap of the substrate material then sets the short wavelength cut-off of the detector, unless the substrate can be removed after hybridization, In sensors in which removing the substrate isn't cost-effective or practical, the hybrid approach severely limits the wavelength range of sensitivity.

Several developments in electro-optics have been occurring that can be leveraged to take a new approach to I K-1 ·PA structure. First, InGaAs sensors on InP substrates have been developed as an alternative to shorter wavelength HgCdTe. InGaAs with a cut-off wavelength of 1.7 μm is lattice matched to InP, and has been used to make high quality area arrays. By using superlattice techniques to relieve the strain due to lattice mismatch, strain relaxed detectors of pure In As on InP have also been demonstrated. These extend the cutoff wavelength out to approximately 2.5 pm.
InP JFETs have also been developed, principally for high speed communication applications. The p-n junction of a JFET provides a barrier equal to the full bandgap, as a opposed to the midgap barrier in a metal gate transistor (MESFET).[5,6] This greater barrier provides a wider logic swing for digital logic, as well as reduced gate leakage for analog circuits.

By combining the InGaAs on InP detector technology with the InP JFET technology,[7-11] a monolithic sensor can be developed that eliminates the need for a hybridization to a separate silicon readout chip. The Jet Propulsion Laboratory has been working with Sensors Unlimited of Princeton, Ncw Jersey to produce such a sensor.

This monolithic sensor is front-illuminate providing near-IR to UV response. It largely eliminates the problem of CTE mismatch, allowing the construction of large yet highly reliable IR FPAs. Finally. it can make use of the high electron motility inherent in InP JFETs to enable readout speeds unobtainable in a silicon readout technology. The resulting sensor will have a number of specialty applications in spectrometry such as atmospheric gas sensing and target identification, as well as optical tracking and optical communication.

In this paper we examine the Construction of a monolithic sensor consisting of a lattice-matched InGaAs on InP PIN diode array with integrated readout electronics consisting of JFETs fabricated in the InP substrate. Two separate designs have been. One is a capacitive transimpedance amplifier (c'I''IA) design; the other uses a source-follower per detector (SFD) structure. Individual discrete devices (the InGaAs diodes and InP JFETs) have been fabricated and characterized. These were followed by the development of prototype test cells consisting of the electronics for a single pixel. Finally, very small prototype arrays (1 x 4 format) have been made by combining cells, using integrated select transistors to allow multiplexing. In the remainder of the paper we discuss the design of these sensors, their fabrication, and the results of their characterization.

2. TECHNOLOGIES FOR IR FPA READOUT ELECTRONICS

Silicon complementary metal-oxide semiconductor (CMOS) very large-scale integrated (VLSI) circuits arc the dominant electronic integration technology in usc primarily due to the ease with extremely complex circuits can be readily integrated using a common, well developed fabrication processed to equally sophisticated and accurate computer aided design (CAD) tools. However, the major problem with using silicon CMOS readouts for scientific IR FPAs is that the needs of excellent hybridization technology due to the limited sensing characteristics of silicon and the operating temperature, most often lower than 77 K, making carrier freezeout an issue

InGaAs/InP or InGaAs/GaAs material system is an interesting alternate as a potential FPA readout technology over the wavelength band of 0.8- 2.5pm for three reasons. First, the thermal expansion coefficient of GaAs or InP is a much better match to that of HgCdTe, potentially permitting large IR FPAs to be reliably fabricated. Second, GaAs or InP is a much more radiation-hard technology than silicon. Third, n-type GaAs or InP devices have a donor level closer to the conduction band edge than silicon, making GaAs devices more immune to freeze-out effects at low temperature. There are several GaAs or InP technologies that can be considered for readout application. These include metal semiconductor field effect transistors (MESFETs), junction FETs (JFETs), and two-dimensional electron gas (2DEG) devices, also known as high electron mobility transistors (HEMTs). Due to the relative immaturity of GaAs or InP, the full potent.iat of the readout is impeded by a lack of demonstration of VLSI circuits, and/or a lack of engineers familiarity with the detail circuit design.

Commercially available GaAs MESFETs long wavelength IR have been extensively studied by Kirschman.[13,14] Noise levels of approximately 50 $nV/Hz^{1/2}$ at 10 Hz for 4 K operation were reported. A 2x64 multiplexer was demonstrated by Rockwell [15]. Measured noise at 78 K was approximately 1 $\mu V/Hz^{1/2}$ at 10 Hz. The major problems facing MESFET readout electronics are gate leakage current and power dissipation in integrated circuits. Unlike a silicon device that has a large oxide barrier to gate leakage, GaAs MESFETs have a 0.8 eV barrier that permits some measurable currents even at cryogenic temperatures. However, improvement of the leakage current to levels acceptable for practical application is considered feasible. The lack of a true complementary circuit technology makes power levels *in the* readout circuits an issue for scientific applications though complementary enhancement/depletion mode MESFET circuits are now being explored for readout application [16].

GaAs complementary hetero-structure FET (CHFET) technology is a demonstrated large scale integrated (LSI) circuit technology for high speed digital circuits at 77 K.[17] JPL has explored this technology for possible application to scientific IR FPA readout.[18,19] The CHFET technology has noise levels of the order of 2 $\mu V/Hz^{1/2}$ at 10 Hz, for 4 K operation. However, the noise was too large to be of practical use in low background applications. The CHFET technolog y also has a gate leakage current that is considered still too high for use in the same scientific IR FPA application.

For usc in scientific IR FPAS over the wavelength band of 0.6- 2.5 μm, both large signal performance that is free from kinks and hysteresis, and small signal performance that is free from excess noise (e.g., l/f noise) arc required. Transistor l/f noise is generally inversely related to device area, so that large transistors have better noise performance than small transistors. Scientific IR FPAs with long integration times require low noise at low frequencies, exacerbating the effect of l/f noise. A typical scientific readout electronics input transistor is required to have an input-referred noise less than 100 $nV/Hz^{1/2}$ at 1 Hz.

3. TEST CHIP FOR MONOLITHIC InGaAs P-I-N/InP JFET

Figure 1 shows the test structures of the p-i-n diode, two different JFETs, a capacitor, including un it cells of SFD and CTIA circuits that are described later. The epitaxial structure of the focal plane array was based on InGaAs/InP p-i-n diode and InP junction field effect transistor platforms.[20]

A Be-doped ($10^{18} cm^{-3}$, thickness= 300nm) p-InP JFET backing layer was grown onto the surface of (100) InP:Fe semi-insulating substrate usinsiggs source molecular beam epitaxy. A S-doped (5x $10^{16} cm^{-3}$, thickness= 1.0 μm) n-InP channel and contact layer (10^{17}...cm thickness=100nm) grown for the discrete JFET control. The n-InP contact layer were followed by a thick (1.5 μm) InGaAs detector absorption layer ($n<10^{16} cm^{-3}$) and a thick (300 nm) n-InP cap layer($2x10^{16}$ *cm" 3,* in succession for the completion of the p-i-n photodiode structure. The p^+-InP of the p-i-n photodiode contact layer and the p^+ isolation region around the perimeter of the JFETs were fabricated in a scaled ampoule diffusion at 500 "C using Zn_2As_3 as the *source. An* InP n-channel completely surrounded by a p region formed by a p^+ layer both under the channel and surrounding the device perimeter. In this geometry, the depletion region pinches off the channel from both top and bottom,

thereby decreasing the switching voltage by a factor of two as compared with a conventional JFET with a single gate p-n junction. Also, there were no exposed p-n junction% thus eliminating arty surface leakage from the side-w:lll of the JFET mesa

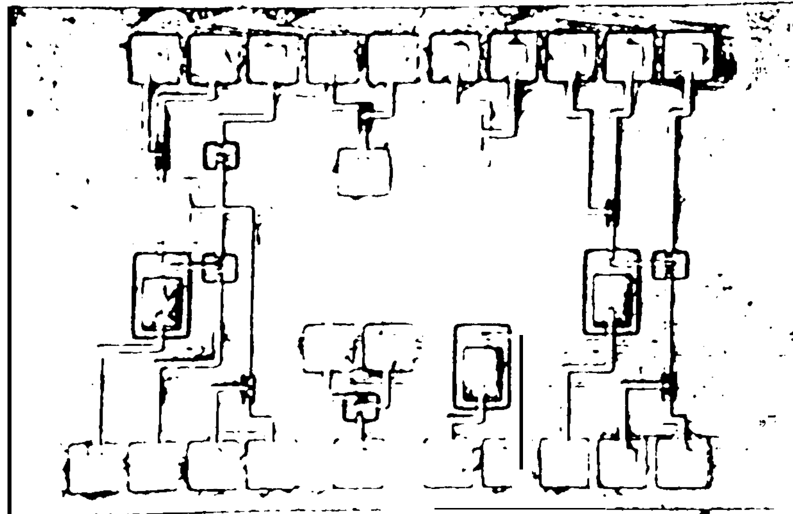
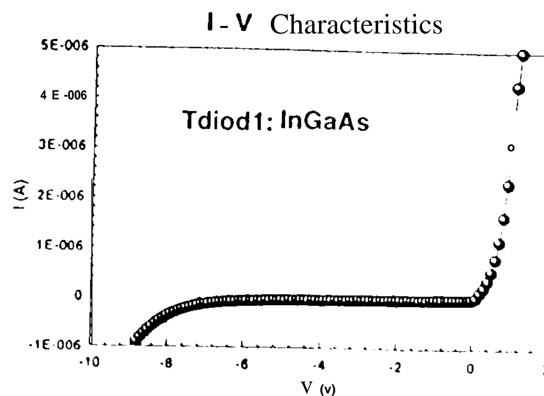
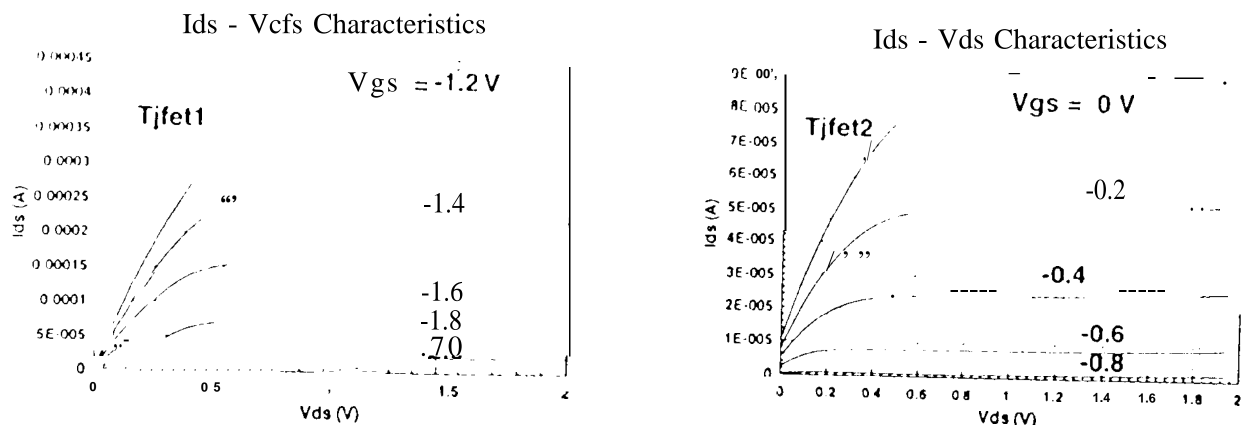


Figure 1. Test Structures fabricated.

Figures 2a -2c show the typical characteristics of the photodiode and JFETs used to apply in signal detecting, amplifying-and switching circuits. The capacitor for the signal-integration was also fabricated with silicon nitride dielectrics and Ti/Au electrodes The capacitance of the typical device were 3.4 pF with $\tan\delta = 0.03$ at 1KHz. The yield of these discrete device fabrication was excellent (>72%) in this lot. Similar results were reported elsewhere in discrete JFETs with drain leakage current as low as 90 pA.[20] These are probably due to several facts of the pinching structures both top and bottom of the n-channel, completely closed side walls of the p^+ isolation layers, and the lightly doped n-channel InP material.



2a. p-i-n Photodiode characteristics at dark room



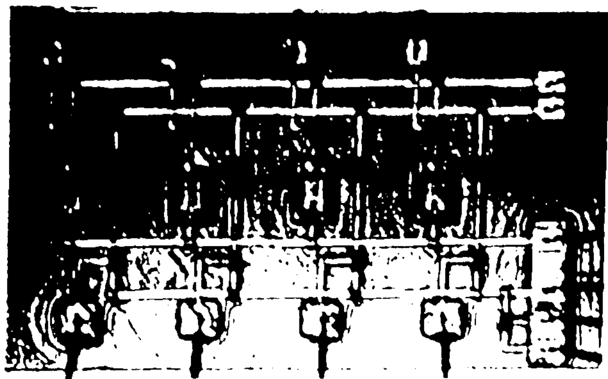
2b. InP JFET for amplifying signal. Gate length: 10 µm, Gate width: 100 pm, n-channel thickness: 1 µm.

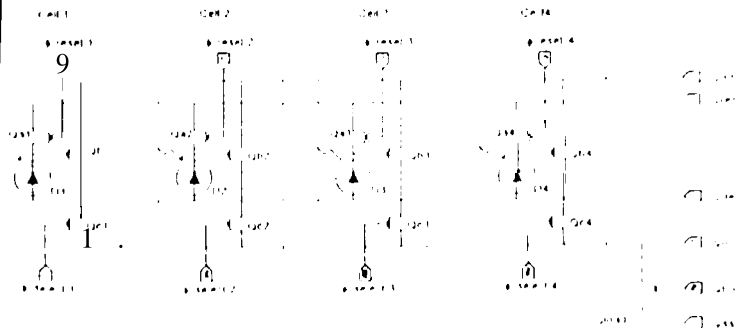
2c. InP JFET for switching control. Gate length: 10 pm, Gate width: **20 pm,** n-channel thickness: 1 µm.

Figure 2. Typical room characteristics of the diode and JFETs.

4. SF-D

Figures 3a and 3b show the 1 x 4 array chip overview and circuit of SFDs constructed using InGaAs photodiodes and InP JFET. The unit cell consists of p-i-n photodiode (D), a reset transistor (Qa) operated as a switch, the source-follower transistor (Qb), and one selection transistor (Qc). The integration capacitance (C_{det}) may just be the detector capacitance and source-follower input capacitance. If A is the gain of the source-follower (A < 1), the photoelectron charge-to-voltage conversion is $A(q/C_{det})$ measured in volts per electron. The cell dissipates little active power during integration. The integration is reset to a reference voltage by pulsing the reset transistor. The photo-current is then integrated on the capacitances during the integration period. As the signal is integrated, the detector bias changes since the signal is integrated directly on the same node as the detector. For large detector capacitance, the voltage-dependent integration capacitance of the detector can result in non-linear charge-to-voltage conversion limiting the usable dynamic range for scientific applications. Readout is achieved by selecting the cell and reading the output of the source-follower.





3a SFD chip overview

3b SFD circuit

Figure 3. 1 x 4 array of the source-follower per detectors (SFD)

The cell is susceptible to threshold voltage non-uniformity leading to fixed-pattern noise (FPN), and to kTC noise unless correlated double sampling (CDS) is used. Since SFD consumes very small real estate, SFD readout is often designed to include a CDS circuit in the unit cell. The main source of white noise in the SFD unit cell is the source-follower transistor itself. The input-referred white noise electrons is given by:

$$\langle N^2 \rangle_{white} = kT/q^2 \, [C_{int}^2/C_{Qc} + 2T_{int}/Ro \,]$$

where C_{Qc} is the load capacitance which the source-follower is required [o drive, T_{int} is the integration time, and the on frequency (f_{sat}) is given by $f_{sat}=1/(2\pi Ro\, C_{int})$. Since SFD is used in applications where the detector resistance (Ro) is extremely small, the detector white noise contribution to the readout noise is negligible. If the load capacitance is much larger than the integration capacitance, low noise performance is possible by allowing the integration capacitance, C_{int}, to be small. However, SFD topology is particularly susceptible to 1/f noise. This is due to the fact that, unlike other unit cell readout circuits, the time period for which the source-follower transistor is turned on during multiplexing is longer than the response time of the source-follower. The effect of this is to enhance the low frequency noise contribution, an effect that has been reported by various authors [21].

An example of the characteristics of output voltage (Vo) with respect to the photo-detector current (Idet) at room temperature for an integrated SFD is shown in Figure 4. By changing the detector current 50 μA, the output voltage was decreased by 2.4 V. It is important that the gate and channel leakage currents of the JFETs should be minimized since the leakage currents from an entire rows were summed at the output, thereby eliminating the ultimate array dimensions and sensitivity of the SFD circuits. Even if the discrete components show their excellent characteristics, the yield of the SDF circuit arrays were low (<24%). The JFET leakage current across the wafer varied, with I_{ds} as high as 1 μA in some cases, and the gate pinch-off voltage varied by* 0.25 V. This lack of uniformity was possibly due to imperfect mask alignment between levels, leakage when summed across the columns for the 1 x 4 array. The typical dark current of the p-i-n diodes of an 16 x 16 imaging arrays was previously reported 2 nA at IV reverse bias, with external quantum efficiencies of $\eta = (0.7 \pm 0.05)$ at λ = 1.3pm were also previously reported in simple imaging arrays.[20]

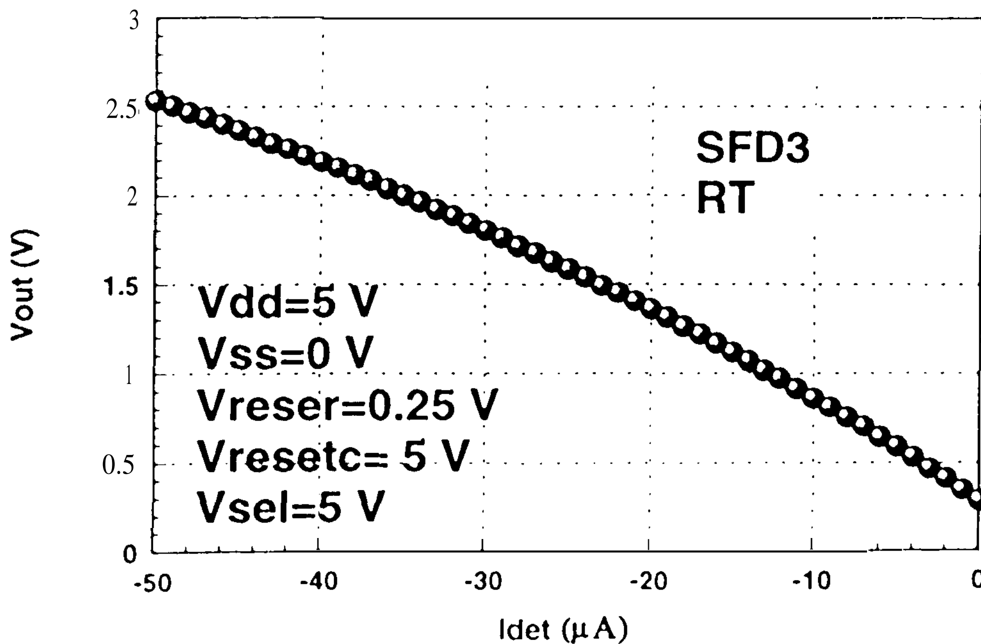
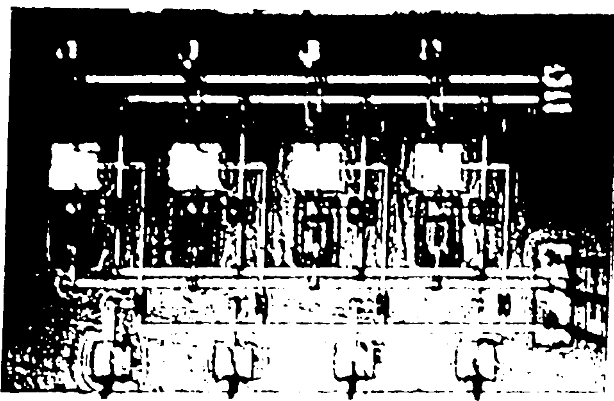
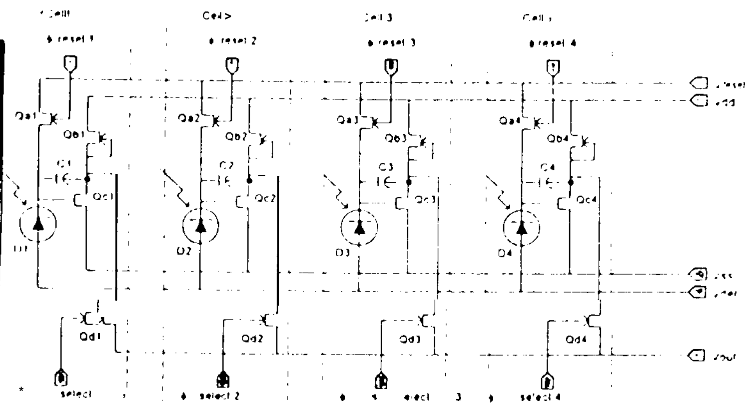


Figure 4. A SFD characteristics of the output voltage with respect to the detector current at room temperature

5. CTIA

Among the many readout techniques, the CTIA and SFD are most often applied for the IR FPAs technology. A 1 x 4 linear capacitive transimpedance amplifier array was designed and fabricated as shown in Figures 5a and 5b. The active pixel sensor in an imager is essentially a single-phase potential well charge-coupled-device (CCD) with a reset transistor (Qa). The CTIA of the sensor consists of a single JFET amplifier with a source-follower with a gain of A, an integration capacitance (C) placed in a feedback loop, and one selection switch (Qd) including a source-follower load (not shown). While a single JFET amplifier is attractive because of real estate reasons the amplifier topology offers superior power supply noise rejection and bandwidth control, which is important for power and noise optimization.





5a, CTIA chip overview. 5b. CTIA circuits.

Figure 5. 1 x 4 array of the capacitive transimpedance amplifier detectors (CTIA)

At the outset of photo-current integration, the integration capacitance **(C)** is reset to a reference voltage (V_{reset}) by pulsing the reset transistor. During the integration mode of operation, the photo-current is integrated almost solely on the integration capacitance, while the feedback and the large gain of the amplifier holds the input at the virtual ground (V_{det}), thereby almost entirely preventing any charge integration on the detector capacitance. Since the input is pinned to the virtual ground a tight control cm the detector bias is mainlined, facilitating its use with detectors having relatively small Ro. Since the output of the unit cell is connected to a low impedance node (the amplifier output), the integration capacitance Or CTIA, unlike other readout techniques, can be made extremely small, yielding excellent low noise performance. However, the high detection sensitivity and low noise is achieved at the cost of increased power dissipation and unit cell pitch. The photoelectron charge-to-voltage conversion is given try:

$q/(C+(C+C_d)/A_{vo})$, where C_d is the detector capacitance,

measured in volts per electron, with A_{vo} being the amplifier gain. As a result of the feedback, the effective saturation tr~.qtl~.[icy of CTIA is decreased compared to that of SFD, and is given by:

$$f_{sat} = 1/(2\pi A_{vo} R_o (C + (C + C_d)/A_{vo}))$$

CTIA is used for low noise, large bandwidth applications since the smallest integration time is limited by the unity gain frequency of the amplifier (Qc). However, there is a trade-off between operating with a small integration time and

focal-plane power dissipation. Combining with other readout technology such as CDS and time delay integration(TDI), IR FPAs can be operated at very low background environment.

An example of the switching characteristics of the CTIA circuits is shown in Figure 6. By changing the reset voltage control less than 0.5 V the output voltage was sharply increased by 0,05 V reaching maximum. The typical characteristics of the detector array can find elsewhere.[20] The detectivity of the hybrid InGaAs FPAS was reported at least two orders of magnitude higher than the HgCdTe FPAs at room temperature. However, due to the large portion of defective fabrication of the JFET (> 32%), only 25% of the array was functional.

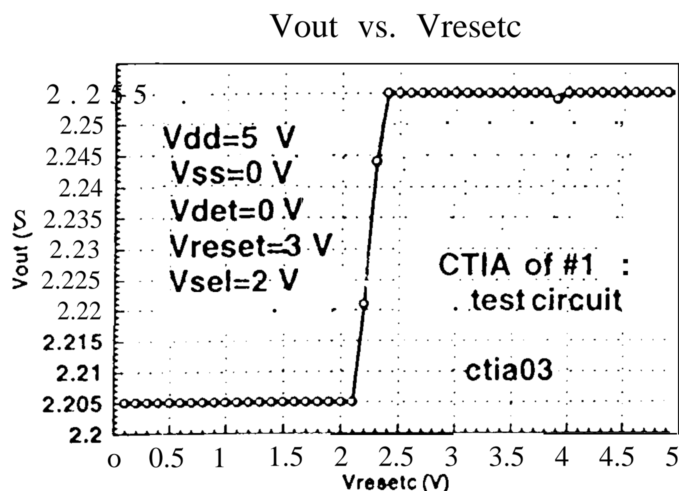


Figure 6. The switching characteristics of the capacitive transimpedance amplifier (CTIA).

6. SUMMARY

Excellent characteristics have been achieved of the individual discrete components needed [o construct the monolithic InGgaAs P-i-n/In p JFET readout circuits. Two fully monolithic visibldnea.r-inbred 1 x 4 active pixel sensor arrays of SFD and CTIA arrays were designed and fabricated. Each InGaAs photodiode detectors can be individually addressed by biasing the gains of the novel, very low leakage InP JFET switching elements at each pixel site. Preliminary results indicate that both SFD and CTIA readout circuits are feasible to eliminate the external multiplexers. However, stability of the circuit contacts should be improved as well as the yielding ratio of the fabrication. More characterization is on the way to optimize the readout circuit construction in improving leakage and response time prior to integrate the readout circuits in two dimensional monolithic active pixel sensor arrays for applications in transportable shipboard surveillance, night vision and emission spectroscopy.

7. FUTURE DIRECTIONS

IR FPA readout electronics will continue to benefit from continued DoD investment in IR FPAS. However, the technology is rapidly reaching a branch point. DoD IR FPAs are clustered in the atmospheric window wavelengths (3-5 µm, 8-12 µm), and are aimed at convenient operating conditions. These include 77-80 K operating temperature and NTSC video

formats such as 640x480 for tactical applications. Some work continues in the longer wavelength, 20 K LWIR detector area for space applications. However, scientific sensors require increasingly lower noise floors, with subelectron read noise desired by the end of this century. The need for large formats with long integration times increases the disparity between DoD-funded development and scientific requirements. To some extent, DoD is becoming more interested in infrared spectroscopy as a surveillance and reconnaissance? technique, so that some leverage might be expected in the future for the development of scientific infrared imaging spectroscopy instruments. These will be low noise, high data bandwidth instruments.

NASA's current needs in sensor electronics were identified. These needs include sub-electron read noise, cryogenic 4 K readout electronics for SIRTF, low noise discrete transistors for 80K, advanced packaging techniques (e.g. thermal compartmentalization), advanced interfaces such as analog-to-digital converters and optical links, and advanced architectures such as event-driven readout. Some technical areas that are emerging as future directions are described briefly below.

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