

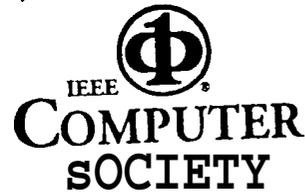
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# A LOW POWER SMART VISION SYSTEM BASED ON ACTIVE PIXEL SENSOR INTEGRATED WITH PROGRAMMABLE NEURAL PROCESSOR

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## Abstract

A low power smart vision system based on a large format (currently **1Kx1K**) active pixel sensor (**APS**) integrated with a programmable neural processor for fast vision applications is presented. The concept of building a **low** power smart vision system is demonstrated by a system design which is composed with an APS sensor, a smart image window handler, and a neural processor. The paper also shows that it is feasible to put the whole smart vision system into a single chip in a standard CMOS technology.

This smart vision system on-a-chip can take the combined advantages of the optics and electronics to **achieve** ultra-high-speed smart sensory information processing and analysis at the **focal** plane. The proposed system **will** enable many applications including robotics and machine vision, guidance and navigation, automotive applications, and consumer electronics. Future applications **will** also include scientific sensors such as those suitable for highly integrated imaging systems used in NASA deep space and planetary spacecraft.

## 1. *Smart Vision System based on APS Integrated with Neural Processor*

Figure 1 shows a system diagram of the proposed smart vision system. The **functional** blocks include: (a) an active pixel sensor. (b) a smart image window handler. (c) a programmable neural processor, and (d) a host interface and timing control card. The APS is used as the optical sensing array in the system. The APS image data is manipulated **by** the smart window handler to provide the input of neural processor. The neural processor is **programmed** to perform various vision tasks in high speed due to its massively parallel computing structures and learning capabilities. The APS sensor, the smart image window **handler, and the programmable neural processor** are controlled by a host computer through host interface and timing control **card**. The output image or vision science data **will** be displayed **by** the host computer.

It is feasible to build the proposed smart vision system in a single CMOS **chip**. This smart vision system on-a-chip **can** take the combined advantages of the optics and electronics to achieve low-power high-speed smart sensory information processing and analysis at the focal plane. The proposed system will enable many applications including robotics and machine vision, guidance and navigation, automotive applications, and consumer electronics. Future applications will also include scientific sensors such as those suitable for highly integrated imaging systems used in NASA deep space and **planetary** spacecraft.

The following sections **describe** technical details of each building block of the proposed smart vision system and also show the feasibility to put the whole system into a single chip in a standard low power CMOS technology.

## 2. *Low Power CMOS Active Pixel Sensor*

The low power CMOS APS camera-on-a-chip has been invented **by** Advanced Imager and Focal Plane Technology group at JPL [1]. APS camera-on-a-chip has great importance for producing imaging systems that can be manufactured with **low** cost, **low** power, and with excellent imaging quality.

Charge-coupled devices (CCDs) are currently the competing technology for image sensors. However, CCDS cannot be easily integrated with CMOS without additional fabrication complexity. In addition, CCDS

require two-order-of-magnitude higher power dissipation than that of APS. The CCD does not have the windowing capability to provide the input data to the neural processor. On the other hand, an APS imager does not have the above limitations and it is the suitable candidate for the proposed smart vision system.

The 1Kx1K APS is used as the optical sensing array and integrated with the neural processor to build the smart vision system for high definition vision applications. A low power 1Kx1K CMOS APS (operate from a +3.3 V Supply) using 0.55 μm n-well process was designed and characterized at JPL. Testing results show that the large format APS with small feature size (10 micron pixel pitch) is capable of excellent imaging performance.

The schematic design of the APS chip's signal chain (for the photogate approach) is shown in Figure 2. It performs correlated double sampling (CDS) to suppress pixel fixed pattern noise, and double delta sampling (DDS) to suppress column dependent fixed pattern noise. It has two separate readout signal chains one analog and the other digital. The digital readout signal chain consists of a 1024 column parallel 10-bit single slope ADCs with built-in CDS.

A block diagram of the 1Kx1K APS chip architecture is shown in Figure 3. It contains a 1024x1024 photodiode or photogate pixel array and 1024 parallel 10-bit singles-slope ADC. The 10-bit decoders are controlled by input clocks to supply the row address and column address for analog or digital mode operation of the chip. The analog outputs are VS\_OUT (signal) and VR\_OUT (reset), and the digital outputs are D\_out0 to D\_out9. The analog and digital readout chains are separated by the pixel array. Each imager can be operated in analog or digital readout mode. Layout of the 1Kx1K CMOS APS with on-chip ADC is shown in Fig. 4.

Testing results measured through the analog signal chain are summarized in Table 1. Figure 5 shows a full 1Kx1K image from the APS sensor operated in analog mode.

Table 1. Summary of testing results measured through the analog signal chain

Parameters	Photodiode APS	Photogate APS
<b>Saturation Level</b>	655 mV (307,000 e-)	570 mV (41,000 e-)
<b>Conversion Gain</b>	2.1 mV/e-	13.9 mV/e-
<b>Linearity</b>	99.9% @ 90% Of Saturation	99.6% @ 90% of Saturation
<b>Peak QE</b>	4 <sub>50%</sub>	18 <sub>70</sub>
<b>Fixed Pattern Noise</b>	0.6% Sat p-p (@ 22.3 °C and 159 msec integration time)	0.6 % Sat p-p (@ 22.5 °C and 39.2 msec integration time)
<b>Dark Current</b>	14.9 mV/Sec	371 mV/Sec
<b>Power Consumption</b>	@ 833 kHz Pixel rate Digital: 5.77 mW Analog: 14.2 mW Total: 20 mW @83.3 kHz Pixel Rate Digital: 2.31 mW Analog: 6.86 mW Total: 9.17 mW	@ 833 kHz Pixel rate Digital: 52.8 mW Analog: 22.3 mW Total: 75 mW @83.3 kHz Pixel Rate Digital: 48.7 mW Analog: 18.2 mW Total: 66.8 mW

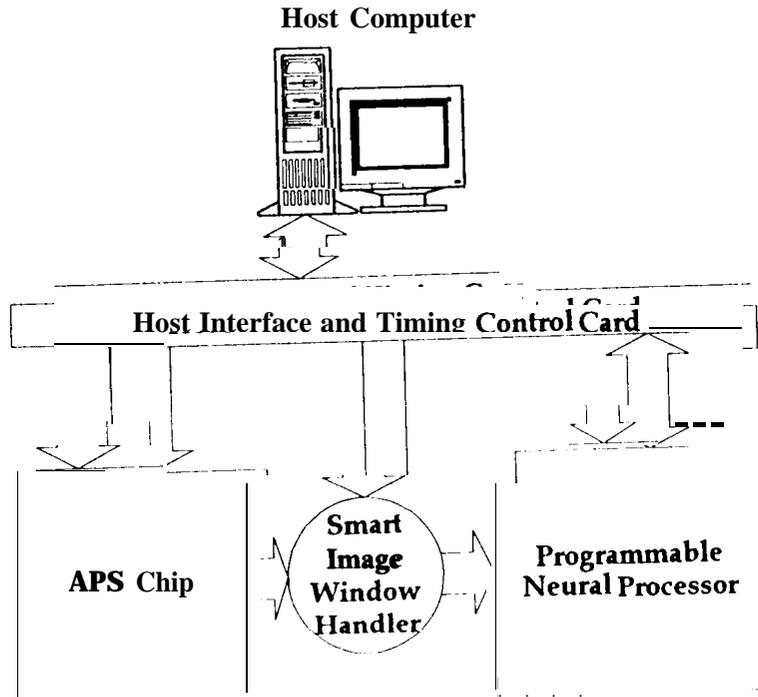


Fig. 1. A system diagram of the smart vision system based on APS integrated with neural processor.

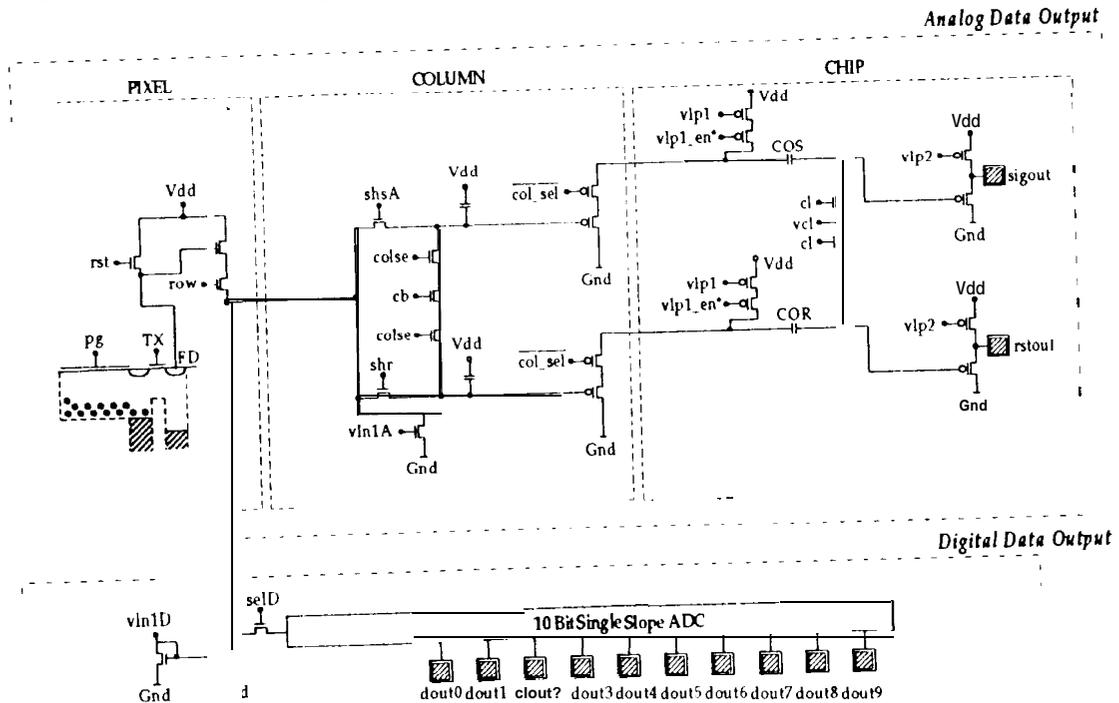


Figure 2. Signal chain of the 1Kx1K CMOS APS chip design.

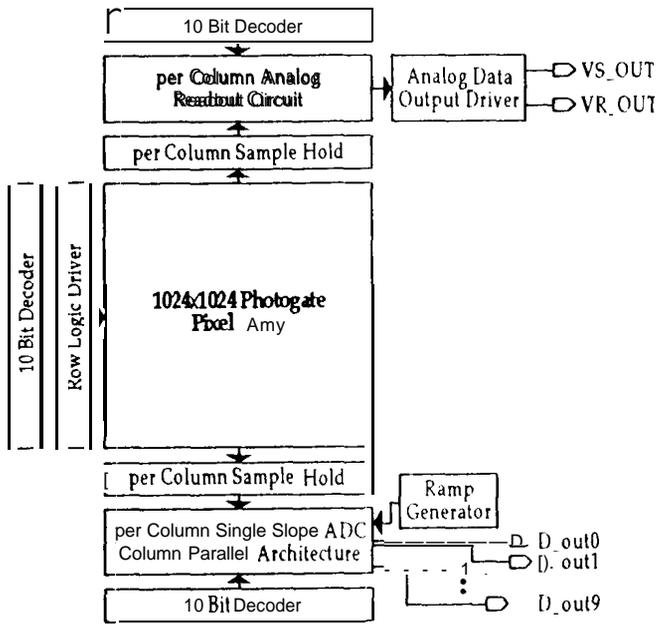


Figure 3. Block diagram of 1Kx1K CMOS APS chip.

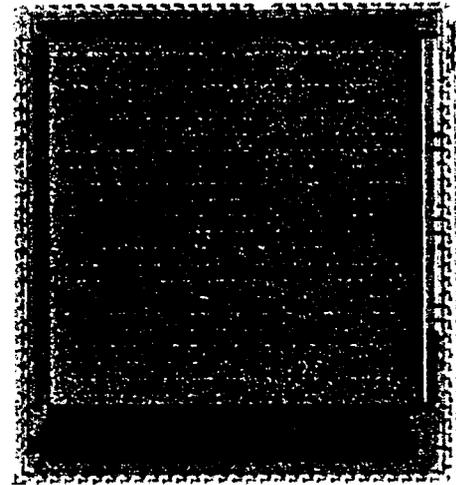


Figure 4. Layout of 1Kx1K CMOS APS with on-chip ADC.



Figure 5. Full Image of 1Kx1K Photodiode CMOS APS from the Analog Output.

### 3. Smart Image Window Handler

The APS images described in the previous section are capable of providing  $m \times m$  sub-window' image data to neural processor. However, the neural processor requires the input data in the format of  $m \times m$  sub-window' which shift in x rows and y columns basis through the whole image, where x and y are integer ranged from 0 to  $n-1$ . Thus,  $(n-m+1) \times (n-m+1)$  sub-windows per frame are required for a  $n \times n$  APS with a window shifting in 1 row and 1 column basis. In this case, the frame time of the APS chip as well as the system will be much longer than the frame time that the APS chip is running in the row by row output mode. This difficulty can be solved by the

smart image window handler. The smart image window handler is designed for the interface between the **APS** chip and neural processor to achieve a fast frame time.

#### **4. Neural processor**

A programmable neural processor based on optimization cellular neural network (**OCNN**) which has been jointly invented by JPL and USC [2]. It can be used as a front-end sensory information processor to provide high throughput real-time computing power at neighborhood of the sensory circuit. The **OCNN** neural processor is programmable and able to perform various vision functions at very high speed in **VLSI**. Moreover, the **OCNN** architecture is a locally connected, massively paralleled computing system with simple synaptic operators so that it is very suitable for **VLSI** implementation. A compact **VLSI OCNN** neural processor is able to provide a powerful computing engine for the smart vision system. Both high data bandwidth and high performance computation are required for various vision **functions**. Incorporating the **OCNN** neural processor into the proposed vision system offers orders-of-magnitude computing performance enhancements for on-board real-time vision tasks.

The **OCNN** proposed for the vision system is an improved version of the **original Cellular Neural Networks (CNN)**. Since its original publication by Chua and Yang [3,4] in 1988, the **CNN** paradigm has evolved rapidly and provides an unified framework for many computation-intensive applications such as signal processing and optimization, **The CNN** has been proved to be universal as the Turing machine [5]. As shown in Figure 7, the **OCNN** is a multi-dimensional array of mainly identical cells which are dynamic systems with continuous state variables and locally connected with their local cells within a finite radius. Figure 8 shows the model of the **OCNN** neuron **C(i,j)**. Many **OCNN** functions have been verified via system simulation. These **functions** include noise filtering, isolated pixel elimination, hole filling, morphological operations, image enhancement, edge detection, connected component detection, feature extraction, motion detection, motion estimation, motion compensation, object counting, size estimation, path **tracking**, collision avoidance, minimal and maximal detection, etc. The operation for different applications depends primarily on the coefficients of the templates and the procedure to apply them. A template includes the information for **synapse** weights, threshold values, and boundary conditions.

Since the **OCNN** design is targeted for smart vision system, it has four more significant features than the basic **CNN**:

*(A) Optimal Solutions of Energy Function:*

Under the mild conditions [3], a **CNN** autonomously finds a stable solution for which the **Lyapunov function** of the network is locally minimized. To improve the local minimized energy function of the basic **CNN**, the **annealing** capability is included to accommodate the applications in which the optimal solutions of energy function are needed. Hardware **annealing** [6] is a highly **efficient** method of finding optimal solutions for cellular **neural** networks.

*@) Multiple Layers with Embedded Maximum Evolution Functions:*

In the **original CNN** every pixel is represented by one neuron. In the **OCNN** every pixel can be represented by multiple neurons which form a **hyperneuron** and execute the maximum evolution data function for various profile selections or the multi-sensor data synergy.

*(c) Digitally Programmable Synapse Weights:*

To improve the fixed synapse weights of the basic **CNN**, the digitally programmable synapse weights are designed for the **OCNN** to accommodate the applications which require programmable **pre-determined** operators.

*(D) High-speed Parallel External Image I/O:*

To improve the data I/O **bandwidth** of the basic **CNN**, a 2-D **array** of optical receivers and transmitters is integrated with the **OCNN** to accommodate the applications which require high-speed parallel image I/O [7].

The **OCNN** can be used as a front-end sensory information processor with the **APS** to provide high throughput real-time computing power at neighborhood of the sensory circuit. The **OCNN** operation theory, architecture, design and implementation, prototype chip, and system applications have been investigated in detail and presented in the references [2,8].

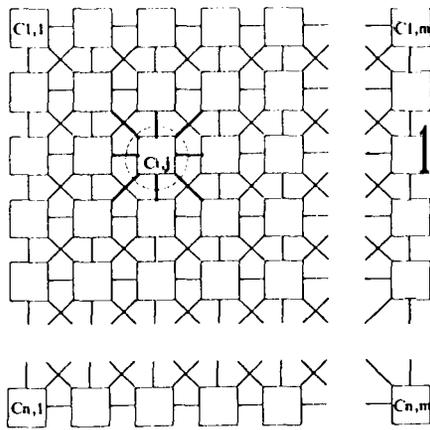


Fig. 7 An n-by-m OCNN on rectangular grid.  
The shaded boxes are the neighborhood cells of  $C(i,j)$ .

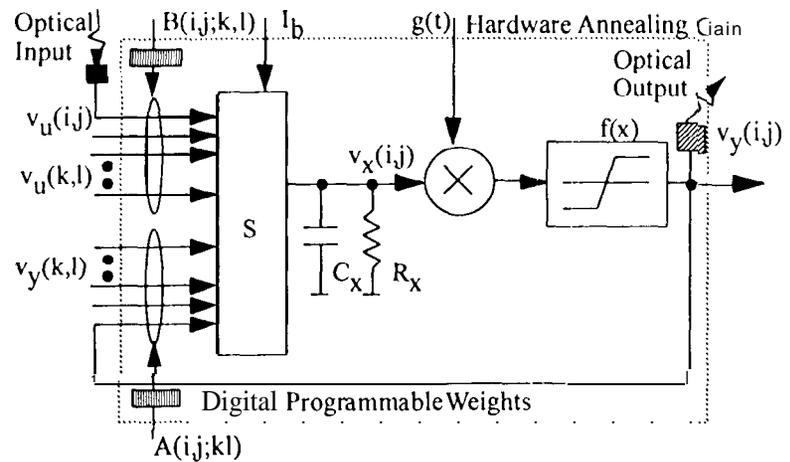


Fig. 8 Functional block diagram of the  
OCNN neuron  $C(i,j)$ .

## 5. Conclusion

Demonstration of the concept of the smart vision system based on APS integrated with programmable neural processor gives the feasibility of design the proposed system on a chip. This highly integrated and ultra-high-speed information processing smart vision system on-a-chip can be used on various NASA scientific missions and other industrial or commercial vision applications.

## Acknowledgments

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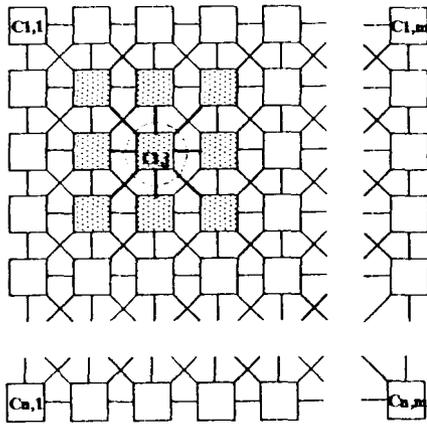


Fig. 7 An  $n$ -by- $m$  OCNN on *rectangular grid*.  
The shaded boxes are the neighborhood cells of  $C(i,j)$ .

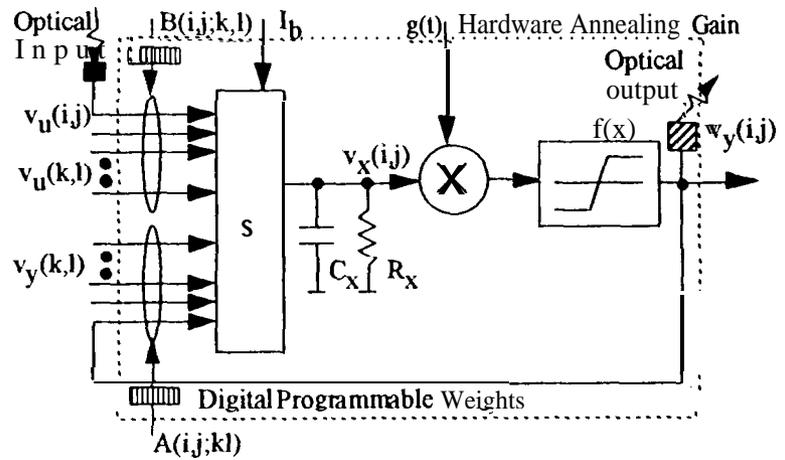


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## Acknowledgments

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