DEEP SPACE ONE BASEBODY CONTROL: VALIDATING THE DATA PATH FROM COMPUTER TO THRUSTER

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ABSTRACT

The Deep Space One Project is the first advanced technology validation mission that is part of the New Millennium Program sponsored by the National Aeronautics and Space Administration (NASA). The Jet Propulsion Laboratory (JPL) and it's industry partner for this endeavor, Spectrum Astro, Inc., are working together with a number of select integrated product development teams, and are tasked with the design, development, and in-flight validation of a chosen suite of advanced technologies.

To verify proper spacecraft function and performance prior to actual launch and in-flight operations, the spacecraft must be subjected to a battery of tests at the assembly, subsystem, and system levels. One facility where much of this testing will performed is the Flight System Testbed for Deep Space One (FST/DS 1). The FST/DS 1 is comprised of flight software test stations and a main integration and test station called the DS 1 Testbed. The latter will assist in providing the necessary visibility to verify and validate the spacecraft avionics systems. One of the key functions of the spacecraft is to provide basebody attitude control to ensure proper spacecraft orientation to adhere to thermal and sun viewing constraints, maintain earth communications, and perform trajectory correction maneuvers.

This paper 'traces' the data path from the computer to the thrusters themselves to illustrate the test and validation process. Along the way, information must be translated and be made compatible with the VMEbus, and MI L-STD-1553B data bus. Test tools such as the computer's RS-232 serial interface, VMEbus analyzer, 1553B bus monitor, Labview, spacecraft simulator "truth" data, and downlinked spacecraft telemetry will provide the necessary visibility to verify and validate the end-to-end data path.

INTRODUCTION

New Millenium Program Overview

The New Millenium Program (NMP) is comprised of a series of advanced technology validation missions defined and implemented as an integrated program for NASA by JPL. A series of deep-space NMP missions (DS 1, DS2, DS3, etc.) are being defined and implemented by JPL concurrently with a series of Earth-orbiting missions (EO1, E02, EO3, etc.) defined and implemented jointly by JPL and NASA Goddard Space Flight Center. NMP is known as the Program, while each mission is called a Project, as in the DS 1 Project.

DS1 Project Overview

Deep Space One (DS 1) is the first NMP deep-space mission. Like all NMP missions, the main objective of DS 1 is to space-validate a suite of advanced technologies - the payload for these missions. The validation of these technologies gives promise to enabling 2 1st century space science missions with low life-cycle mission cost. There are twelve such technologies for DS 1. A mission profile was chosen which serves as an appropriate test track for the selected complement of advanced technologies. The baseline mission profile includes a near-Earth asteroid encounter, a Mars flyby and a comet encounter.

DS1 is being developed and implemented under a technology-driven mission paradigm vs. the typical science-driven paradigm. Validating the twelve advanced technologies is the primary objective of the mission. Returning some science data at appropriate times during the mission -- part of the validation process -- and completing an extended mission are secondary and tertiary objectives, respectively.

DS1 will be the first spacecraft with ion propulsion as its primary propulsion system, which poses new mission design and implementation challenges, addressed prior to this time only by conceptual mission and system studies. The nominal launch date for DS I is July 1, 1998.

Avionics System Overview

The heart of the DS1 Avionics System is the Integrated Electronics Module (IEM). The IEM contains a VME backplane and thirteen integrated avionics boards. Among the thirteen boards is the radiation-hardened RISC6000 (RAD6K) processor which hosts the spacecraft Flight Software (FSW). The Attitude Control Subsystem (ACS), including device drivers and ACS sensors are also a critical part of the Avionics System. The IEM and ACS are integrated and delivered to JPL on the "Partial Bus" Structure by JPL's industry partner, Spectrum Astro, Inc. located in Gilbert, AZ.

Several DS 1 New Technologies are also included in the Avionics System. They include the Multi-Functional Structure (MFS), Low Power Electronics (LPE), Power Actuator and Switch Mechanism (PASM), and the Autonomous Navigation capability.

This paper describes the DS 1 basebody control verification and validation by tracing the tested data path of the RCS thruster. This data path traverses through various areas of the Avionics System.

Basebody Control Overview

The functional requirements of the Reaction Control System (RCS) are that it shall maintain spacecraft attitude, perform spacecraft turns, perform delta-V maneuvers and compensate for launch vehicle tip-off rates. The RCS maintains S/C attitude during sun pointing, optical navigation imaging, camera imaging, and high gain antenna downlink.

The Attitude Control Subsystem (ACS) provides attitude deterrnination using a star tracker or Stellar Reference Unit (SRU) and an Inertial Measurement Unit (IMU). Basebody control and delta-V maneuver execution are performed using the RCS thrusters. This paper discusses the basebody control function of the RCS, and particularly how it's data path is validated in the DS I Testbed.

The hardware managers for the SRU, IMU, SSA and PDE are all part of the ACS FSW. 'l'he ACS FSW operates with VxWorks processes and all ACS H/W managers communicate with the 1553B Bus Manager. Figure 1 shows the ACS software organization for the modules that affect the RCS.

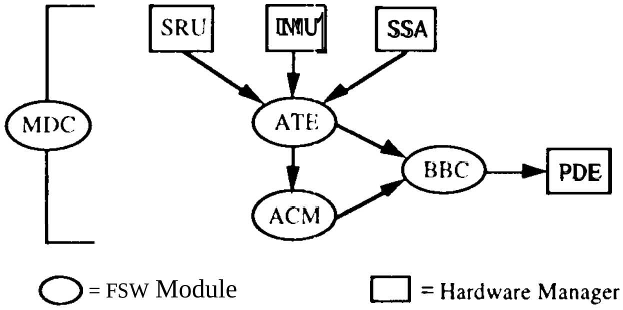

FIGURE 1. DS1 ACS FSW Architecture (for RCS)

The Mode Commander (MDC) runs the other ACS functions. Timing of each control loop is coordinated and the ACS state machine is maintained by the MDC.

The Attitude Estimator (ATE) receives input from the SRU and IMU hardware managers and estimates spacecraft attitude quaternions, spacecraft rates, IMU bias parameters and quaternion/bias estimation error covariances. The SSA hardware manager is used as input to the ATE only in the event of a fatal SRU failure.

The Attitude Commander (ACM) receives input from the FSW Executive, Navigation (NAV) and ATE and provides attitude and rate commands to the basebody controller.

The Basebody Controller (BBC) receives input from the ACM, ATE, Ground Segment and an internal mass property tracker/estimator. The ACM provides the desired attitude and angular velocity. The ATE provides the estimated attitude and angular velocity. The Ground provides the current RCS thrust level. The output of the BBC is thruster commands to the PDE Manager.

It is the verification of the entire hardware and software interaction that is the end goal of testing the RCS function. The testing is performed in increasing complexity, starting with low-level verification of messages to the stand-alone PDE and completing with closed-loop interaction of the Spacecraft Simulator (SIM) with the ACS software controlling the PDE thruster output based on modelled SRU and IMU data. The next section of the paper describes the test approach planned for the DS 1 Testbed to achieve the goal of basebody control verification.

TEST APPROACH

A main objective of the DS1 test program is to subject the Avionics Subsystem to a battery of tests at the assembly and subsystem levels prior to formal system level integration and test. An incremental development approach is followed such that preliminary versions of flight software will be generated and tested before the official flight version is delivered for testing on the spacecraft.

The first level of testing primarily verifies the electrical integration of the Avionics IEM hardware, the Electrical Ground support Equipment (EGSE), and the "test build" flight software. This includes the verification of interfaces between the VME and RAD6K processor, interfaces with EGSE standard interface boards (e.g., MI L-STD-1553B, Serial RS-232, CCSDS), and proper operation of the "test build" flight software. In addition, this set of tests allowed the test team to gain initial hands-on experience with the DS 1 Testbed.

In the next FSW version delivered to the DS I Testbed, the PDE Manager will be incorporated. This will allow software control of 1553 B messages to and from the PDE board. Additionally, the Telemetry managers will provide downlink of PDE status to the Ground Data System (GDS) for verification. Finally, the ACS FSW is delivered to the DS 1 Testbed and the full functionality of the RCS system is integrated.

For each FSW version delivered with ever increasing capability, individual objects or modules will first be unit tested, then integrated at the subsystem level, and finally tested on the DS 1 Testbed with the lEM hardware. To facilitate validation of all required functions, the EGSE which is used for hardware electrical integration and validation, and a LibSim collection of software models will be integrated into a single system known as the SIM. This allows for "closed-loop" spacecraft dynamics simulation with which the RCS functionality can be fully verified. In this test stage, performance verification of the subsystem will also be performed. All commands and telemetry shall be verified using the Ground Data System (GDS) through exhaustive tests across the period of the DS I test program.

The final stage of testing involves exercising select modes in a flight-like scenario where synchronization of spacecraft clock time and execution of activities via command sequence are important aspects. Following the validation of the spacecraft operations in the DS1 Testbed, the command sequences will be executed as part of the formal system level integration and test program on the DS 1 Spacecraft.

WALK-THRU OF THE RCS DATA PATH

In testing the RCS thruster operations, the goal is to verify that the desired thruster is selected and fired for the proper duration. First a test case is developed which defines the commands and parameters needed to properly exercise the thruster interface as well as the telemetry channels that will provide visibility into the expected results. The last page attachment illustrates the details of the RCS data path. Two other figures within the body of the text provide a higher-level view of the segments described.

GDS / EGSE Uplink Segment

Per the test case, commands are generated using a GDS tool on a UNIX platform. Command stems and parameters are selected to produce command files. At the time of test execution, a script takes each command file, generates a Spacecraft Command Message File (SCMF) which is then converted into a Command Link Transmission Unit (CLTU) block. Commands are issued one at a time from the GDS workstation to the EGSE host computer thru the TCP/IP socket connection.

Commands are then sent from the EGSE host across a MXI interface to the EGSE Signal Rack. The MXI connects the external computer (i.e., EGSE Host) to the VME backplane of the CMD/TLM chassis in the EGSE Signal Rack. Similarly, there is a MXI interface between the NT workstation and the Signal Interface chassis in the EGSE Signal Rack. Industry Pack (1P) carriers in the chasses are connected internally via ribbon cables to their associated Transition Modules. The test harness connects the Transition Modules to the front connectors of the Uplink/Downlink (UDL) board residing in the IEM Chassis. Figure 2 illustrates the Ground Data

System and [electrical Ground Support Equipment data paths for the RCS Thruster function.

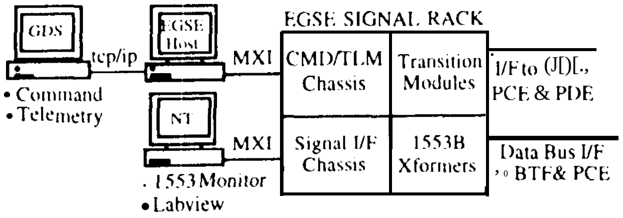

FIGURE 2. DS1 GROUND & EGSE DATA PATHS FOR RCS

Avionics Data Segment

Aboard the DS 1 Spacecraft, the Integrated Electronics Module chassis contains a VME backplane and thirteen avionics electronics boards. The DS 1 Testbed has a functionally identical lEM. The Avionics boards that are critical to the RCS Thruster functionality are the RAD6K computer, the Uplink/Downlink Board (UDL), the Intelligent 1553B Interface Card or Bus Transfer Function (BTF), the Propulsion Control Electronics (PCE), and the Propulsion Drive Electronics (PDE). The RAD6K computer resides in Slot 1 of the VME backplane and is the only VME bus master in the system. The UDL and BTF communicate with the RAD6K over the VME backplane. The PCE is installed into the VME backplane, but only uses it for power. The PDE is not plugged into the VME backplane, but is merely housed in the IEM chassis for mechanical support. Figure 3 shows the data paths of the RCS commands and responses through the FSW and Avionics hardware of the I EM. Each segment of this data path is described in the sections that follow the figure.

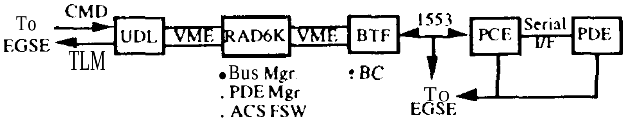

FIGURE 3. DS1 AVIONICS DATA PATH FOR RCS

Uplink/Downlink Board (UDL). The UDL communicates with the FSW resident on the RAD6K computer over the VME bus as a 24-bit address, 16-bit data (A24/D16) slave. When a command is issued at the GDS workstation, the UDL receives the Command Link Transmission Unit (CLTU) from the EGSE, decodes the command, and performs error detection and correction on the command. It then stores the resultant 64 bit (n = 56) codeblocks in 4096 x 16 dual port memory accessible to the flight software over the VME.

On the return data path, the UDL accepts telemetry frames from the flight software over the VME bus. The UDL performs Reed-Solomon Encoding of the data and transmits the serial data to the EGSE where it is provided to the GDS for display.

RAD6K/Flight Software (FSW). Once a command is received over the VME by the RAD6K, the Uplink Manager (software object) of the FSW interprets the command data sent from the UDL and determines which hardware manager the command is intended for. In the DS 1 software system design, there is one hardware manager for each 1553B remote terminal, therefore a command to the PDE is received by the PDE Manager in FSW. All 1553B hardware managers interface to a Bus Manager object which then provides a single interface board for all 1553B transactions to the Bus Controller software resident on the BTF. The 1553B hardware managers are responsible for setting up all input and output transactions for its remote terminal device.

On the downlink side of the data path, the FSW provides a Telemetry Manager which receives telemetry from applications, including 1553B hardware managers, and routes it for transmission or storage and later playback. Each 1553B hardware manager assembles telemetry packets from 1553B data supplied by its remote terminal device.

Intelligent 1553B Interface Card (a.k.a. Bus Transfer Function, BTF). The BTF acts as an A24/D16 VME slave on the VME bus, and as the 1553B bus controller for the spacecraft. As the 1553B bus controller, the BTF takes commands from the FSW Bus Manager over the VME bus, converts them to 1553B format, schedules the commands, and then transmits the commands over the 1553B bus to the remote terminals. The BTF also accepts status and data returned by the remote terminals over the 1553B bus, converts and buffers the data, and makes it available to the flight software over the VME bus.

The Bus Controller software resides in a MI L-STD- 1750A processor on the BTF. The Bus Manager schedules 1553B transactions through VME shared memory using nine basic message formats. The Bus Controller acknowledges receipt of each message and updates each schedule accordingly. '[he Bus Controller also communicates 1553B transaction results to the Bus Manager through VME shared memory.

Propulsion Control Electronics (PCE) & Propulsion Drive Electronics (PDE). The PCE, as a remote terminal, accepts input and transmits output over a MI L- STD-1553B Data Bus. Commands are accepted and translated to energize any of the eight thruster valves for a fixed period of time (< 2 seconds) with a quantization of 1 millisecond. In addition, commanded delay times of up to once second prior to energizing the propulsion valve are accepted and translated by the PCE.

The PCE provides the only data interface to the PDE by sending control signals to, and reading status signals from the board via an opto-isolated serial interface. The PDE is a heritage item from the Mars Pathfinder Valve Driver Board with only minor modifications made to increase timing signal margin for the DS1 application. The control signals from the PCE and the status signals to the PCE are opto-isolated and voltage regulated on the PDE board. The PDE provides drivers for up to eight propulsion thruster valves, eight catalyst bed heaters and two propulsion latch valves. The latch valve functions are not used on DS1.

The PCE is Remote Terminal 5 (RT5) on the 1553B bus. It receives and transmits messages only at Subaddress l (SA l). The PCE receives 17 words on SA 1 with a send receive command. The first 16 words of the receive command are for thruster operation. Words O thru 7 handle on-time of the thrusters, while words 8 thru 15 are for the thruster delay-time operation. Word 16 of the send receive command is used to turn on or off the heaters and latch valves (unused).

The PDE reads the driver output levels at the end of each command and sends this status back to the PCE. The PCE reads this status and translates the information into 1553B status request response format. The PCE sends 2 words on SA 1 with a send transmit command. Word O of the send transmit command contains the thruster and heater status. Word l contains latch valve status (unused).

EGSE / GDS Downlink Segment

The EGSE Signal Rack provides de-coupled interfaces for each IEM board. COTS equipment (i.e., Transition Modules and 1P Carriers) with standardized functions were developed by JPL's industry partner, Spectrum Astro, Inc., to support system integration of the DS1 Avionics hardware and FSW. The EGSE interfaces to the 1)S1 GDS which is part of JPL's Multimission Ground Data System. The GDS downlink provides interfaces and support applications to receive, decode and display spacecraft telemetry. The GDS system used in the DS l Testbed is also used for JPL Spacecraft I&T and Mission Operations, demonstrating that the Avionics System is tested as it will be flown.

UDL Transition Module to CDS. The UDL board is connected by a test harness to the UDL Transition Module. Internal to the EGSE Signal Rack, the transition module is connected to an 1P carrier residing in a VME chassis. A MXI card provides user connection to this VME chassis via an EGSE Host workstation. The EGSE Host is connected to the GDS Workstation via TCP/IP, which is a transmission control protocol that ensures reliable data packet transfer from source to destination.

In a test case scenario, the UDL presents downlink data to the EGSE which is interpreted and routed to the GDS for channelized display of telemetry. Included in this data is status reported from the PCE/PDE. This is the standard validation method used in the DS l Testbed t o exercise the flight-like downlink system.

1553B Bus Monitor. When the GDS telemetry does not provide enough information to verify a 1553B test function, a bus monitor can be used. The BTF Bus Controller and 1553B remote terminals (Rts), such as the PDE, physically connect to the 1553B bus terminals at the back of the EGSE. Also connected to the 1553B terminals, and residing in an EGSE VME chassis, is a commercial DTI card which serves as the bus monitor. A MXI card provides user connection to this VME chassis via an NT. A Labview interface was developed by Spectrum Astro, Inc. for display of the bus monitor activity. Command and status messages on the 1553 B bus are displayed for verification by the test engineer.

In an open-ended test system (i.e., prior to SIM integration), a Labview interface for the PDE output can be used. The thruster output of the PDE front connectors is brought back to the EGSE transition module via the test harness.
In addition to opto-isolation and differential to single-ended TTL signal conversion, the Transition Module for the PDE contains inductive loads that simulate the RCS thruster valves. Internal to the EGSE, the transition module is connected to an 1P carrier and again, the MXI provides the user interface to verify the PDE thruster outputs with Labview.

HK68/V4F, Spacecraft Simulator. The SIM resides on a Heurikon 68040 processor installed in a VME chassis of the EGSE. Integration of the SIM in the DS1 Testbed introduces a thruster state integral, an RCS Hardware Model, and a spacecraft dynamics model, developed through the use of a commercially-available SD/FAST Tool Set. Now the PDE thruster output, driven by the ACS FSW, is received by the SIM in a closed-loop environment. The Thruster State Integral records the thruster state every 1 ms, sums the on/off times for 1 RTI (real-time interrupt: 1RTI = 125 ins), and writes the data to a buffer which is read every RTI. The RCS Thruster Model converts the thruster ID, duration, and delay time to forces and/or torques applied to the spacecraft. The SD/FAST Spacecraft Model responds to these applied forces and/or torques. To close the loop, the IMU model and SRU model within the SIM produce new spacecraft rates and quaternions which are provided back to the ACS FSW.

Test Tools. The following test tools are used in the DS1 Testbed environment to provide low-level diagnostic information, especially during troubleshooting of unexpected results within a test.

RAD6K RS-232 port: All FSW modules are VxWorks tasks. Their activity can be monitored via a "dumb" terminal connection to the RS-232 port of the RAD6K computer.

BTF Serial Port: The Bus Controller software is also a VxWorks task. Its activity can be monitored via a serial connection from the EGSE Host machine to the BTF IP carrier residing in the EGSE Signal Rack. The IP carrier interfaces through the Transition Module and test harness to the front connector of the BTF.

VMETRO: By installing a VMETRO card in the IEM chassis, VME bus activity between the UDL and the RAD6K or the RAD6K and the BTF can be monitored for diagnostics. A VMETRO card installed in the EGSE allows monitoring of VME bus activity between the SIM card and the I P carriers.

TESTING TO DATE& FUTURE WORK

Upon delivery of the IEM hardware from Spectrum Astro, Inc., to the DS 1 Testbed, each board in the chassis, including the PDE, was tested individually using a MXI interface to the IEM backplane. In the first phase of integrated testing in the DS 1 Testbed, hardware managers do not exist in the FSW. Individual "back-door" 1553B messages can be generated and issued by the test engineer to exercise the 1553B interface to the PCE/PDE. As of the writing of this paper, these 1553B commands are not working properly, and the PDE has not been exercised by the FSW in the DS 1 Testbed.

SIM integration in the DS 1 Testbed is underway with IMU, SRU, and PDE models expected in early September. The PDE Manager is to be delivered in the next major FSW version, currently scheduled for mid-August. The ACS Software does not arrive in the Testbed until mid-October. DS 1 closed-loop basebody control will be demonstrated in the Testbed once all components to the system are integrated and verified.

CONCLUSION

In a complex project whose test program is challenged by fixed cost and fixed schedule, DS1 is adopting a 'smart' approach in its development and use of the DS1 Testbed environment. The basebody control example presented in this paper illustrates the multiple data interfaces exercised in the DS 1 design for a standard spacecraft function, and how versatile the testbed is in supporting thorough, integrated testing of this function.

To accomplish the verification and validation of various spacecraft capabilities in the DS1 Testbed, like basebody control, advantage is being taken of tool re-use and adaptation (i.e., we are not re-inventing the wheel). The EGSE provided by Spectrum Astro., Inc. is built on commercial products, adapted for DS1 application. The SIM is built from the commercial tool, SD/Fast. Using JPL's Multimission Ground Data System in the DS1 Testbed assures that the spacecraft is tested as it will be flown. In the faster, better, cheaper atmosphere of the New Millennium projects, the DS 1 Testbed environment is cost sensitive and at the same time provides flexibility in support of the project's critical test phases.

ACKNOWLEDGEMENTS

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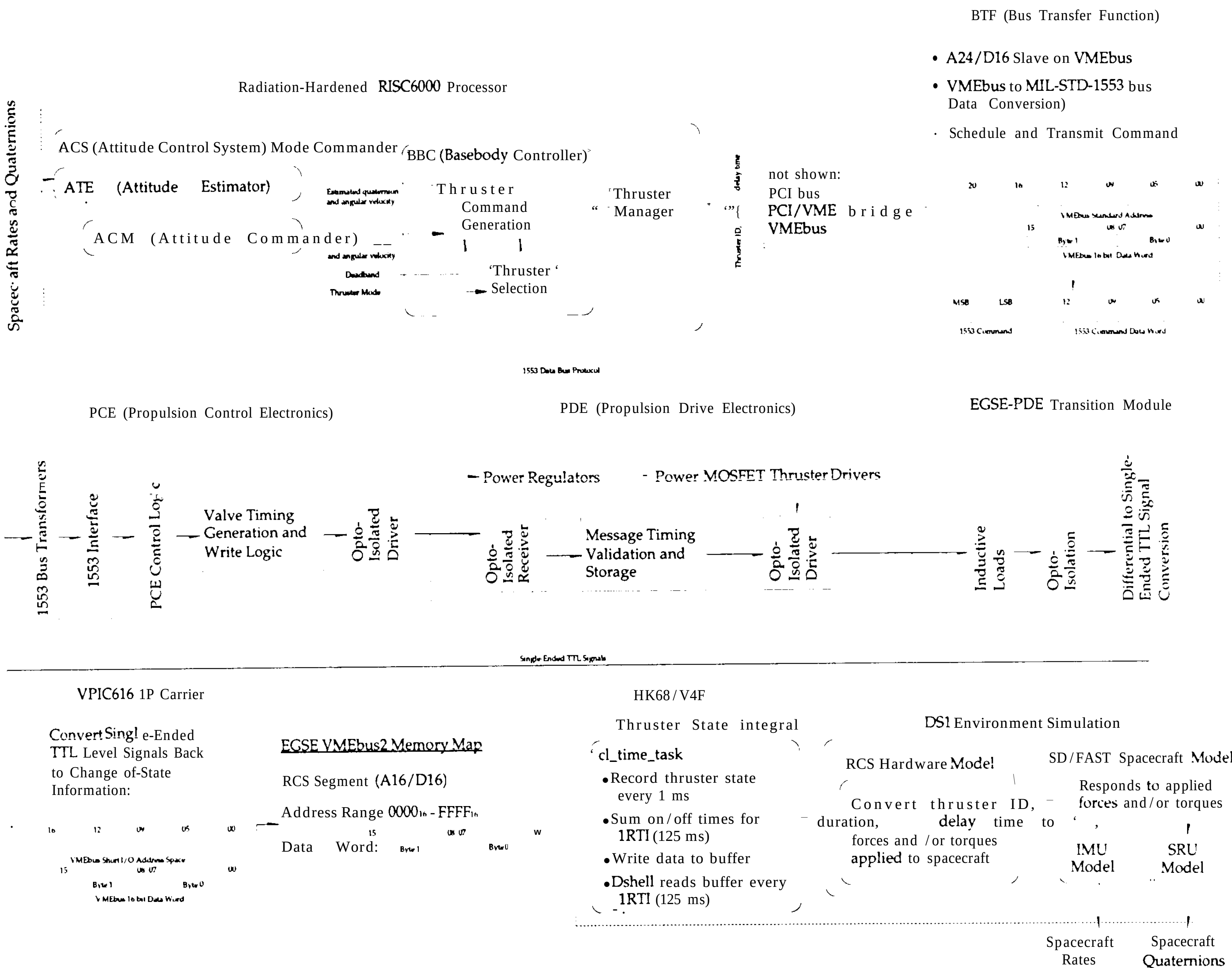

Figure 4. DS1 Closed-Loop Basebody Control Data Path