

Radiation Effects in Advanced Microelectronic Technologies[†]

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Introduction

Several new radiation phenomena have been observed in laboratory testing of advanced microelectronics that are not yet of sufficient importance for typical space applications, but provide insight into the likely effects of scaling and device design on radiation hardness. These effects include hard errors from heavy ions, complex failure modes in advanced memories and gate arrays, and single-event transients. This paper discusses these effects, along with scaling predictions from the electron device community on the future timescale for scaling limits and design feature size. The results predict that hard errors will become a major factor as feature sizes are reduced below 0.25 μm , and that devices optimized for low power will be less sensitive to hard errors than devices that are optimized for speed.

Hard Errors

Microdose Errors. Hard errors due to the local dose (*microdose*) from single or multiple hits of heavy particles was reported by Dufour, et al. in 1992 [1] and modeled by Oldham, et al. in 1993 [2]. They concluded that the effect was only important for a narrow class of devices, such as DRAMs and 4-T cell SRAMs that are strongly affected by changes in subthreshold leakage, which is the main effect of microdose errors on MOS transistors. However, more recent work in the device literature has shown that devices used with lower voltages will be more sensitive to microdose errors because statistical fluctuations in the number of dopant atoms cause a distribution of threshold voltages within large-scale devices. Figure 1 shows a representative example for a 1.5 V process with 0.1 μm feature size [3]. The coefficient of variation (σ/mean) is 0.06, leading to a $4\text{-}\sigma$ range of nearly 25%! Microdose damage on devices with initially low threshold voltage will cause large increases in leakage, far greater than for those with initial values near the mean. For devices with very thin gate regions, doping fluctuations will be the dominant factor. However, as shown in Figure 2, microdose voltage changes on the "ears" of the

threshold voltage distribution will be important for devices that are optimized for power supply voltages above 2 V. Thus, microdose errors are expected to be important for a large class of CMOS devices until scaling allows high performance devices with very low power supply voltages to be used.

Gate-Rupture Errors. A new type of hard error, similar to gate rupture in power MOSFETS, was reported for 4-Mb DRAMs by Swift, et al. in 1994 [4]. Although this class of error only appeared for ions with very high LET, device scaling lowered the threshold, as shown in Figure 3. The curve in the background shows the relative number of ions in the galactic cosmic ray threshold (normalized to 20 $\text{MeV}\cdot\text{cm}^2/\text{mg}$). Once the threshold approaches 30 $\text{MeV}\cdot\text{cm}^2/\text{mg}$, the error rate is expected to rise abruptly. This class of errors has been seen in several additional device technologies, as shown in Table 1. The dependence of this type of error on electric field strength has not been fully determined. Early estimates assumed a square law dependence [5], but recent work on programmable gate arrays (the dielectric is an oxide-nitride-oxide sandwich) suggests a much stronger field dependence, as shown in Figure 4. Note that the cross section increases by several orders of magnitude with very slight increases in applied voltage. More limited results for DRAMs suggest that the error rate scales as the 4th power of the applied field, which is not as severe as the apparent dependence for gate arrays, but much stronger than the square-law dependence.

Gate rupture errors are particularly important for advanced devices because they can potentially occur in random logic as well as in storage cells. Any device with a high electric field on the gate -- which would apply to any individual transistor that is biased positively or negatively -- can potentially be affected. In most cases, random logic errors are not amenable to system solutions, such as error-detection-and-correction, and may produce a wide range of functional failure modes in complex devices. Once the error probability reaches the point

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where significant numbers of errors are predicted on a yearly basis in the galactic cosmic ray environment, it may be impossible to use them in practical space systems. As discussed in the next section, field strengths are expected to increase as devices are scaled to smaller feature sizes, exacerbating the gate-rupture problem.

Scaling Predictions

Devices are expected to scale to much smaller feature sizes during the next decade. Table 2, taken from a report by the Semiconductor Industry Association [6], shows how this is expected to evolve. Although some devices are currently being manufactured with feature sizes that are more aggressive than these predictions, the results in Table 2 are still **expected** to be representative of mainstream technology. Device types with 0.25 μm feature size and power supply voltages of 2.5 volts or less are expected to be widely available before the new Millennium.

Although one might expect that lower electric field strength would occur in the gate regions of devices with lower power supply voltage, scaling predictions from the electron device community predict *higher* field strengths [7- 11]. There are significant advantages to increasing field strength, providing that the quality and defect density of gate oxides can be increased. Earlier scaling predictions were based on the assumption that 2 MV/cm was the maximum practical field strength [12, 13], but advances in fabrication technology have relaxed that limit. Figure 5 shows the predicted evolution of oxide field strength for two scaling algorithms, one based on performance (speed), and the other on devices optimized for low power.

The importance of the gate-rupture mechanism on a particular fabrication technology depends on the oxide field strength and the dependence of the LET threshold on field. Scaling predictions based on a square-law dependence for threshold LET and the predicted field strength increase as technology evolves are shown in Figure 6. This figure shows the number of predicted hard errors per year for a device with one-million transistors (with the gate appropriately biased) due to galactic cosmic rays. The abrupt increase for high-speed scaling at 0.25 μm is due to the nearly step-function dependence of the GCR abundance (see Figure 3), not discontinuities in field strength or scaling. Figure 6 shows that the lower field strength predicted for device technologies that are

optimized for low power is of considerable advantage, resulting in a much lower error rate for scaled technologies. However, even for low-power technologies hard errors are expected to become a dominant problem as feature sizes approach 0.1 μm .

Scaling predictions provide a good starting place to determine the likely effect of future technology changes on radiation hardness, although all such predictions involve assumptions that may not be entirely accurate as real technological improvement are implemented. Results to date suggest that the square-law dependence of threshold LET is too conservative. The accuracy of the electric field strength predictions is more difficult to assess. Past history suggests that the initial generation of devices with 0.25 μm feature size will use field strengths that are somewhat lower than optimized values. There are a number of reasons for this, including the high risk to the manufacturer if the technology cannot be manufactured with sufficient reliability. Thus, actual device technology may lag somewhat from predictions based on optimized values. Nevertheless, the predictions strongly suggest that the next generation of large-scale devices will begin to be susceptible to significant numbers of non-recoverable hard errors, which may be a limiting factor in their applicability in space.

Practical Problems

A number of factors make it difficult to investigate hard errors. The most convenient way is to use a large-scale device that contains many easily tested elements, such as a DRAM. This allows the buildup of errors with different incident ions and/or test conditions to be investigated on a single device, but has the disadvantage of only controlling the field strength within narrow limits. For devices with internal voltage regulation or charge pumps, it may be impossible to significantly change field strength.

Test structures provide an alternative, but relatively large numbers are required because each individual event is destructive. Compounding this difficulty is the fact that most manufacturers of scaled devices are unwilling to provide test structures to outside users.

Device technology is yet another factor. DRAMs have been used as test vehicles primarily because of their uniform structure and testability.

However, DRAM scaling algorithms are more conservative than other device types because of the extreme competitiveness of the market and low margins. Other technologies, such as microprocessors and flash memories, have extremely complex failure modes, making it difficult to use them for studies of hard errors even though they may potentially be more affected by hard errors than DRAMs because of differences in scaling and design.

Finally, many scaled devices are quite sensitive to total dose effects. The total dose produced by large fluences of heavy particles can inadvertently produce errors from total dose or microdose that can be confused with hard errors. This is particularly true for flash memories and DRAMs, but may be a factor for other devices as well. Devices with internal charge pumps are particularly affected by total dose effects, and degradation of the charge pump circuitry can produce large effects on the overall circuit operation as well as on the operating margin of individual devices.

Conclusions

The initial studies on SRAMS and DRAMs that resulted in individual hard errors provide a good starting point for estimating how technology evolution will affect radiation hardness. The evidence to date strongly suggests that this will become a dominant issue in the near future as commercial devices are scaled to 0.25 μm and below. Fortunately, the problem appears to be less severe for low-power technologies, which are likely to be the first choice for space applications. However, if the scaling predictions are reasonably accurate, even low power technologies will be affected by hard errors at the 0.1 μm level.

There is always some risk in attempting to predict the effects of future technology changes, but in this case the point at which hard errors are expected to be a severe problem is not that far away. More work needs to be done to study hard errors in current generation devices -- 64 Mb DRAMs and microprocessors -- to determine if the scaling predictions based on the previous generation of devices still holds. It appears that hard errors are likely to be the dominant problem for the next generation of such devices, and is vital to understand this before they are designed into space systems.

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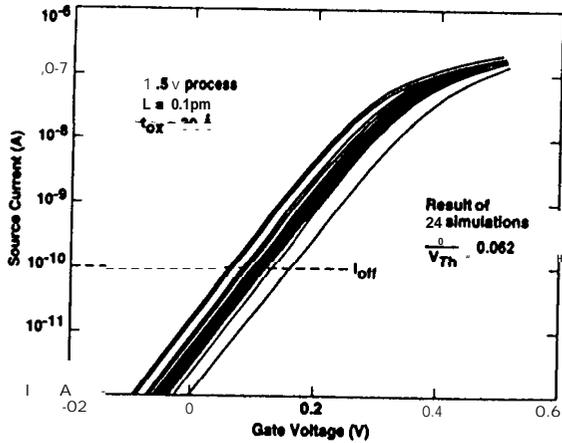


Figure 1. Threshold Voltage Distribution for Scaled Devices Due to Doping Fluctuations

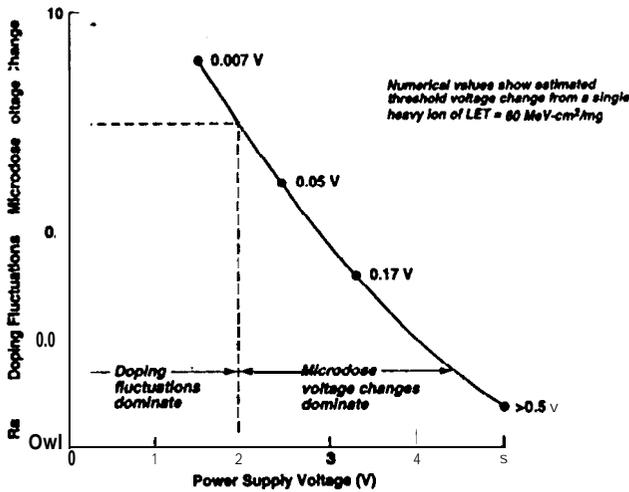


Figure 2. Comparison of the Effects of Voltage Fluctuations and Heavy-Ion Microdose on Scaled Devices

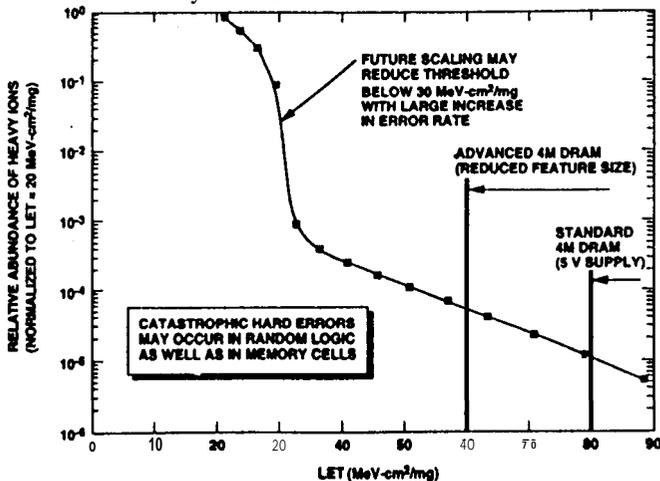


Figure 3. Change in Threshold LET for 4-Mbit DRAMs Due to Device Scaling

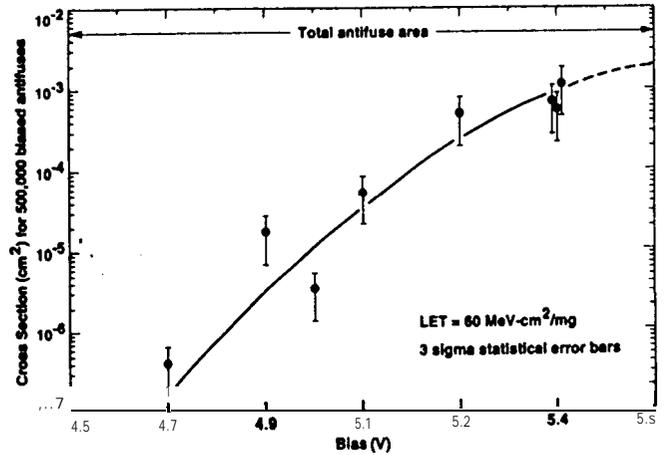


Figure 4. Effect of Voltage on Heavy Ion Hard Error Cross Section for Oxynitride Structure in Field Programmable Gate Arrays

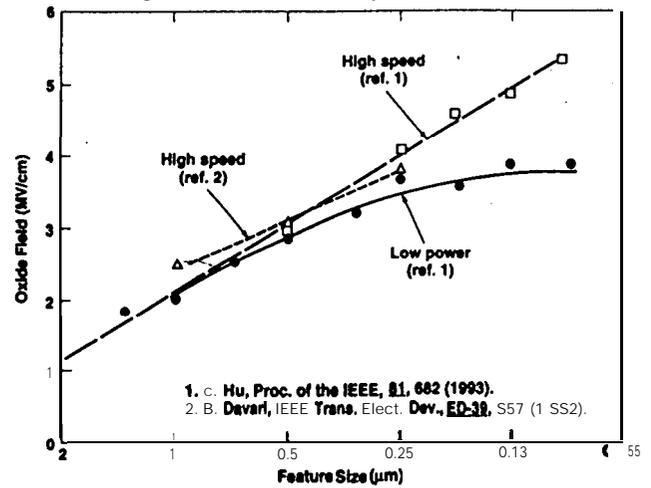


Figure 5. Predicted Increase in Oxide Field Strength for High-Speed and Low-Power Scaling

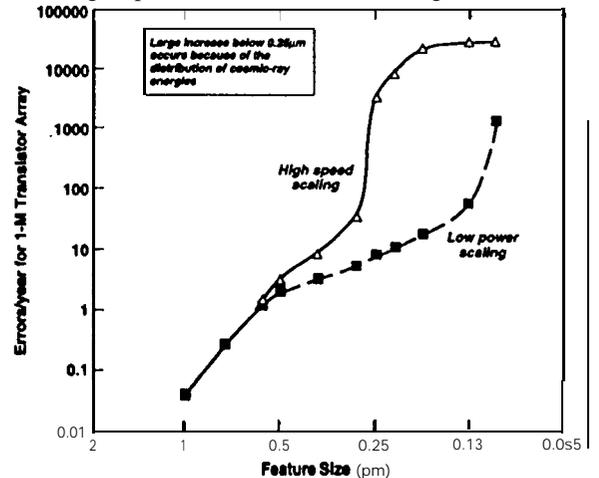


Figure 6. Scaling Predictions for Hard Errors for an Array with One-Million Transistors

	<u>OXIDE THICKNESS</u>	<u>ELECTRIC FIELD</u>	<u>THRESHOLD FOR HARD ERRORS</u>
4-Mbit DRAM (Standard)	180A	2A MV/cm	<80 MeV-cm ² /mg
4.Mbit DRAM (Scaled)	150A	2.8 MV/cm	<60 MeV-cm ² /mg
4-Mbit DRAM (Different vendor) ---	---	...	<60 MeV-cm ² /mg
FPGA	● 98.5 Å	5.7 MV/cm	52,8 MeV-cm ² /mg
FPGA	~*87 Å	6.3 MV/cm	40 MeV-cm ² /mg

*Equivalent oxide thickness of O-N-O ● wJwich structure

Table 1. Hard Error Thresholds for Several Types of Device Technologies

Year	1890	1885	1998	2001	2004	2007
V _{DD} (V)	5	3.3	2.5	1.8	1.5	1.2
I _{ox} (A)	200	120	100	75	60	40
Feature size (µm)	0.8	0.35	0.25	0.18	0.13	<0.1
Substrate technology	bulk	epi	epi	epi	epi	sol

Key Issues: voltage fluctuations
noise margin
oxide quality

Table 2. Predicted Evolution of Device Technology
(from a 1994 Industry Roadmap Report)