

# Comparison of Total Dose Responses on High Resolution Analog-to-Digital Converter Technologies\*

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## 1. INTRODUCTION

High-speed and high-resolution analog-to-digital converters (ADC) are critical devices for space electronic systems. Analog Devices's bipolar technology 12-bit A/D converter, AD574A, was proven to withstand up to 100 krad(Si) [1], but excessive power consumption limits its applications in many new high-speed and low-power system designs. Several other commercial 12-bit successive approximation register (SAR) A/D converters with BiCMOS technology from different manufacturers have been tested and showed various results [2]. Failure modes were also quite different for those converters at different dose rates [3].

This paper compares total dose effects on two different technology (CMOS and BiCMOS) 12-bit ADCs from the same manufacturer, Burr-Brown. Low dose rate (LDR) test for the BiCMOS converter is in progress and will be reported in the final paper. CMOS ADCs are particularly attractive in low-power circuit design in space applications. However, there were inherent limitations with analog CMOS technology even with self-calibration architecture as in Crystal's CS5016 16-bit ADC [4]. The CMOS converter failed at a very low total dose level with high dose rate (HDR) irradiation. Despite the improved failure level of the CMOS converter at LDR, BiCMOS converters showed that they were indeed better candidates for space applications provided they did not show enhanced low dose rate (ELDR) effect in their bipolar components [5-8]. A BiCMOS converter from Maxim, MX674A, failed catastrophically at total dose levels below 5 krad(Si) at LDR because of ELDR effect; the converter functioned to about 25 krad(Si) at HDR and recovered quickly during annealing [3]. This paper discusses results for both CMOS and BiCMOS technology 12-bit converters from one manufacturer, comparing architectures and radiation response mechanisms. More low-power CMOS 12- and 16-bit converters from Burr-Brown and Harris will be included in the final paper.

## 11. EXPERIMENTAL APPROACH

ADC574A is fabricated with a CMOS and laser-trimmed bipolar technologies. This BiCMOS converter has internal scaling resistors which can be used to select analog input signal ranges of 0V to + 10V. ADS574A is a CMOS A/D converter

which uses a capacitor array implemented in low-power CMOS technology. Key features of the device are low power consumption and internal sampling. The converter can be also operated from a single +5V supply. These area drop-in replacements for AD574 models of other manufacturers for most applications.

Devices were irradiated with a room type irradiator at a high dose rate of 50 rad(Si)/s. Low dose rate tests of the ADC574A BiCMOS converter at 0.005 rad(Si)/s are in progress to see whether it will show ELDR effects. Results will be reported in the final paper.

## III. TEST RESULTS

The BiCMOS converter, ADC574A, requires supply voltage of 5V and \*15V. The +5V is specified as  $V_{logic}$  supply. The CMOS converter, ADS574A requires only  $V_{dd}$  of 5V and -15V for  $V_{ee}$  (no +15V supply is required). The CMOS converter is recommended for use in low power consumption applications.

The +5V power supply current was measured at HDR of 50 rad(Si)/s and plotted in Figure 1. The supply current of the CMOS converter continuously increased until 35-40 krad(Si) where devices were nonfunctional. Although not shown in the figure, the supply current of the CMOS device annealed and recovered to the initial values after 24 hours at room temperature. Note that dotted portion (in between open-square symbols) of the CMOS plot between 35-40 krad(Si) total dose levels where devices became non functional. The supply current of the

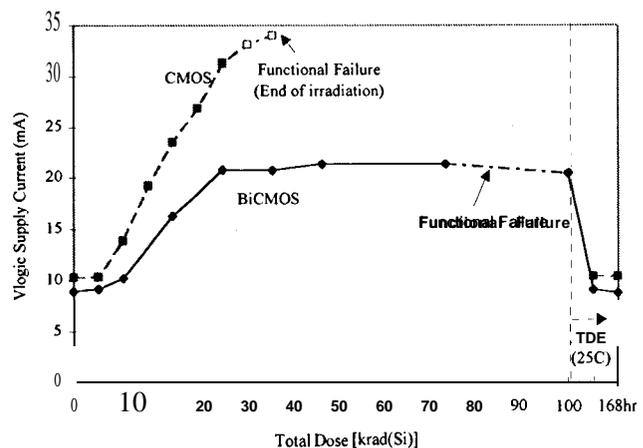


Figure 1. Comparison of  $V_{logic}$  supply current degradation at 50 rad(Si)/s.

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CMOS converter increased further to 34 mA when devices failed functionally at the final total dose level of 40 krad(Si). Supply current of the BiCMOS converter sharply increased up to 30 krad(Si) and remained at 21 mA until the final total dose level of 100 krad(Si). It annealed back to initial values at room temperature. The device failed functionally between 75 and 100 krad(Si).

Conversion time of these converters is another parameter that showed significant differences in degradation as shown in Figure 2. The conversion time of the CMOS converter did not show any degradation at all up to 35 krad(Si). The converters abruptly stopped functioning at 40 krad(Si), and could not make any conversions. Thus, conversion time could not be measured at 40 krad(Si).

The conversion time of BiCMOS converters increased gradually until 75 krad(Si), the last radiation level at which the converters were still functional. This may indicate that degradation of the bipolar device is the cause of the large increases in conversion time. However, this may be inconsistent with the room temperature annealing.

The failure mechanism of these devices will be investigated in more detail for the final paper. Devices will be opened up and cross-sectioned for scanning electron microscope (SEM) analysis, and localized SEM irradiation will be used to find the sensitive internal component.

The last parameter that showed significant differences in radiation degradation is the integral nonlinearity (INL), shown in Figure 3. INL is the most important parameter of these SAR type 12-bit ADCs. The CMOS converter showed tremendous increase in nonlinearities from 20 krad(Si) to 35 krad(Si). When converters became nonfunctional at 40 krad(Si), INL could not be remeasured anymore. The INL parameter recovered during 168 hours room temperature anneal. However, it did not fully recover to the initial value. High temperature (100 °C) annealing is in progress to observe further recovery. For the BiCMOS

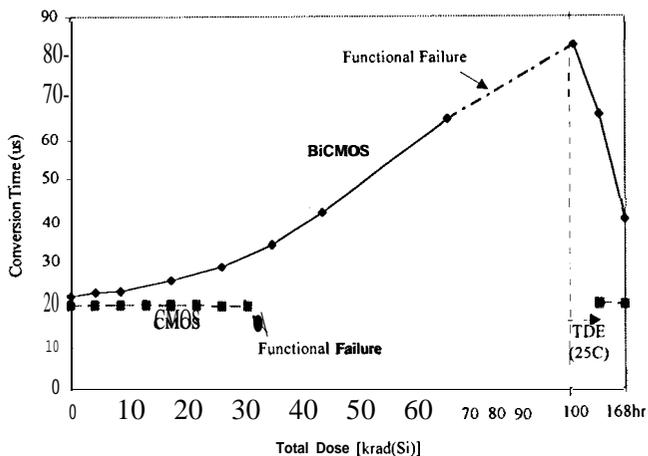


Figure 2. Conversion time degradation of two different process converters at 50 rad(Si)/s.

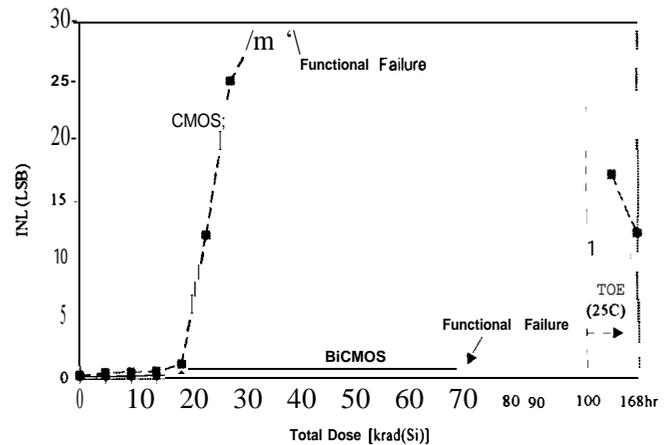


Figure 3. Comparison of Integral nonlinearity degradation at 50 rad(Si)/s.

converter, INL increased slightly and recovered during room temperature anneal. This is one of most important parameters and critical results for decision making process for converter applications in space environment.

#### IV. DISCUSSION

Reducing power consumption is a far more difficult in analog circuit design than for digital circuits because of inherent limitations in bandwidth, resolution, and signal-to-noise ratio [9]. Some flash ADCs are designed and fabricated for low-power applications, but these converters do not have resolutions as needed in space applications. The most critical component in high accuracy SAR converters is the internal comparator which requires extremely close matching of parameters in analog circuitry. This is much easier to achieve in bipolar technology because of the inherently better matching and high transconductance of bipolar devices compared to CMOS devices.

Three different technologies are available for this particular 12-bit SAR A/D converter. The older bipolar converter dissipates almost one watt. Therefore, it is not even comparable in power consumption to other two later technology converters. The CMOS converter is designed for low-power applications. However, the power dissipation increases as the radiation level increases and the most important parameter, INL, also degraded significantly. The BiCMOS converter, on the other hand, can operate at much higher radiation levels than the CMOS converter with some degradation of conversion time. Functional failure in the BiCMOS converter occurred at much higher levels and was far higher than that of the MX674A. The CMOS converter failed abruptly at lower radiation levels because of inherent limitations in CMOS technology.

For actual LDR environment, however, the CMOS converters may perform better compared to the BiCMOS converters. BiCMOS converters may show ELDR effect in bipolar components internal to the converter. In this case, a low-power CMOS converter may be more suitable to use in space applications. Several other 12-bit and 16-bit CMOS ADCs from Burr-Brown

will be tested in near future. LDR results of these devices along with the BiCMOS converter will be discussed in the final paper to determine which process converter is better to use in space applications.

## V. REFERENCES

- [1] C. I. Lee, B. G. Rax, and A. H. Johnston, "Total Ionizing Dose Effects in 12-bit Successive-Approximation Analog-to-Digital Converters," IEEE Workshop Record, Radiation Effects Data Workshop, 112 (1993).
- [2] T. L. Turflinger, M. V. Davey, and J. P. Bings, "Radiation Effects in Analog CMOS Analog-to-Digital Converters," 1996 IEEE Radiation Effects Data Workshop, IEEE 96TH8199, in press.
- [3] C. L. Lee, B. G. Rax, and A. H. Johnston, "Total Ionizing Dose Effects in High Resolution A/D Converters," IEEE Trans. on Nucl. Sci., NS-41, p.2459 (1994).
- [4] C. I. Lee, B. G. Rax, and A. H. Johnston, "Hardness Assurance and Testing Techniques for High Resolution (12- to 16-bit) Analog-to-Digital Converters," IEEE Trans. on Nucl. Sci., NS-42, p. 1681, (1995).
- [5] J. Beaucour, T. Carriere, A. Gash, D. Laxague, and P. Poirot, "Total Dose Effects on Negative Voltage Regulator," IEEE Trans. Nucl. Sci., NS-41, 2420 (1994).
- [6] D. M. Schmidt, D. M. Fleetwood, R. D. Schrimpf, R. L. Peace, R. J. Graves, G. H. Johnson, K. F. Galloway, and W. E. Combs, "Comparison of Ionizing Radiation Induced Gain Degradation in Lateral, Substrate, and Vertical PNP BJTs," IEEE Trans. Nucl. Sci., NS-42, 1541 (1995).
- [7] J. M. Bose, G. Sarraiyrouse, and F. X. Guerre, "Total dose effects on elementary transistor of a comparator in bipolar technology," RADECS Proceeding, p. 223 (1995).
- [8] R. D. Schrimpf, "Recent Advances in Understanding Total-Dose Effects in Bipolar Transistors," RADECS Proceeding, p.9, (1995).
- [9] K. Shimohigashi and K. Seki, "Low-Voltage ULSI Design," J. of Solid-State Circuits, SC-28, p.408, (1993).