A Review and Prediction of Chip Scale Solder Joint Reliability

Reza Ghaffarian, Ph.D.
Jet Propulsion Laboratory
California Institute of Technology

Abstract

Availability of board level solder joint reliability information is critical (o the acceptance of CSPS as alternative packages. This paper will review different CSPS as well as their assembly reliability. Based on this information, solder joint reliability of these packages will be projected for a specific environment using a modified Coffin-Manson relationship. Projected board level reliability for different package type and the pin count will be presented in graphs.

Introduction

Emerging Chip Scale Packages (CSPs) are competing with bare die assemblies and are now at the stage BGAs were about three years ago. These packages provide the benefits of small size and performance of the bare die or flip chip, with the advantage of standard die packages.

CSPS are defined as packages that **arc up to** 1.2 or 1.5 times larger than the perimeter or the area of the die, respectively. Many manufacturers now refer to CSP as package that is the miniaturized version of its previous generation. Packaging accomplishes many purposes including the following:

- Provides solder balls and leads that are compatible with the PWB pads for reflow assembly processes whereas aluminum pads do not,
- Redistributes the tight pitch of the die to the pitch level that is within the norm of PWB fabrication. Small sizes of CSPS do not permit significant redistributions and the **current** cost effective PWB fabrication limits full adoption of the technology, especially for high 1/0 counts.
- Protects the die from physical and alpha radiation damages, and provides a **vehicle** for thermal dissipation and ease of testability for die functionality.

CSPS generally have been categorized in different types based on their fundamental structures. These are:

- Interposer packages with either flex or rigid substrate
- Wafer level molding and assembly redistribution
- Lead On Chip (LOC) packages.

Currently, most of data are those that were generated for package qualifications by manufacturer and a very limited published information available on assembly reliability. These data are of limited value to the end user since they have been collected under significantly different manufacturing and environmental conditions for packages with different pin counts.

Assembly Reliability **for Conventional Packages and Those Projected for CSPs**

Reliability of conventional SM packages as well as Ball Grid Arrays have been investigated at JPL. Cycles to failure test data points and their Weibull distributions for 28-, and 20-pin I,CC, and 68-pin gull wing assemblies are shown in Figure 1. Thermal cycling ranged -55°C to 100°C with 246 minute duration ... The failure distribution percentiles were approximated using a median plotting position, Fi= (i-0.3)/((n+0.4). The two-parameter Weibull cumulative failure distribution was used to fit data.

For comparison, projected cycles to failure for low count CSPs are also included. Results are those gathered from literature and projected based on a modified Coffin-Manson relationship, It is seen that

board level reliability of most CSP packages arc comparable or better than their LCC counterparts. These packages, however, are not as robust as leaded packages including gull wing and J-leads (not shown in Figure since there were no failures to 3,000 cycles).

Consortium to Assess Board Level Reliability

Board level solder joint reliability information critical to the acceptance of CSPS as alternative packages. For wider applications of this technology, the potential user will need reliability data for its design since often they have no resources, time, or ability to perform complex environmental characterizations. JPL has formed a consortium with the objectives of addressing many technical issues regarding the interplay of package type, 1/0 counts, PWB materials, surface finish, and manufacturing variables on quality and reliability **of assembly packages**

Currently, **the** MicrotypeBGA consortium has defined packages for the test vehicles and is in the **process of design** of the test vehicles. 1(is anticipated that more than 300 test vehicles will be assembled and subjected to various environmental conditions representative of space and military as well as commercial applications.

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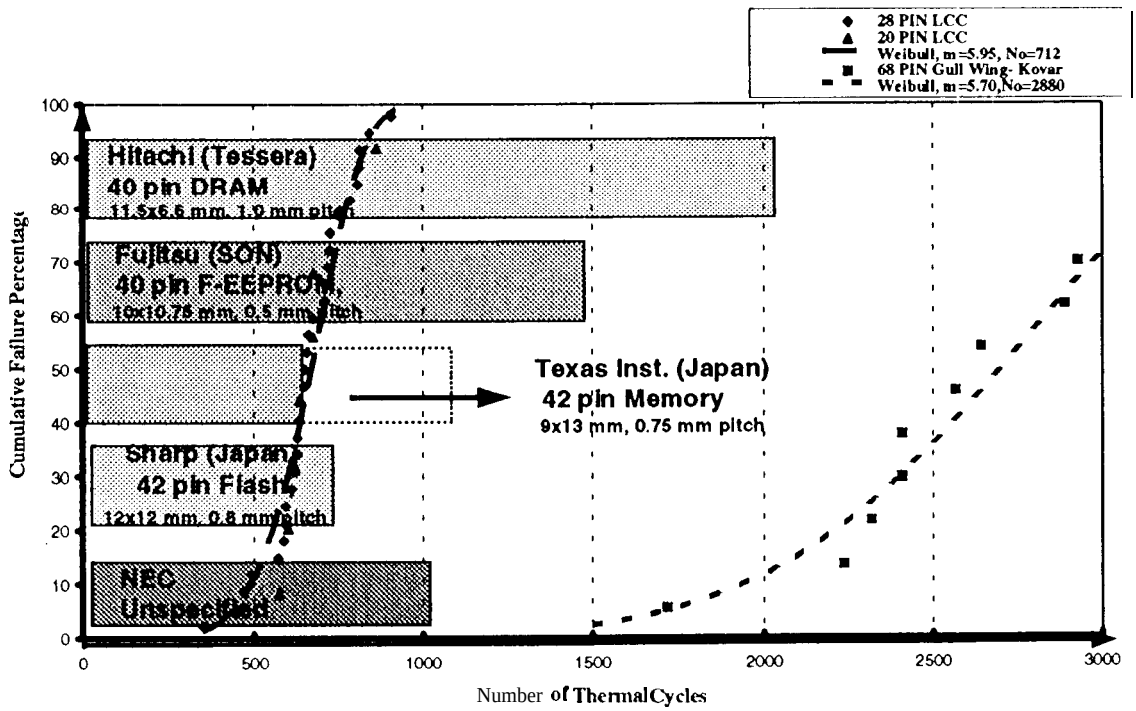

Figure 1. Projected Cycles to failures for Low Pin Count CSP Assemblies and Cumulative Failure Distribution for Conventional SM Package Assemblies Tested at JPL (-55°C to 100"C)