

## Megapixel CMOS AI% with Analog and Digital Readout

*Barnak Mansoorian\*, Guang Yang, Roger Panicacci\*, Craig Staller,  
Bedabrata Pain, and Eric Fossum\**

Center for Space Microelectronics Technology  
Jet Propulsion Laboratory - California Institute of Technology  
4800 Oak Grove Drive, Pasadena, CA 91109  
Phone: (818)-354-5462, Fax: (818)-393-0045, Internet: Guang.Yang@jpl.nasa.gov

Two 1024x1024-element CMOS active pixel image sensors (AIS) with on-chip analog-to-digital conversion (ADC), analog and digital readout signal chain electronics have been designed, fabricated and tested. One is based on photodiode-type CMOS APS pixels and the other on photogate-type pixels; both feature in-pixel source followers, row selection and reset transistors. The chips have been implemented in a 0.55  $\mu\text{m}$  n-well process, have a 11.0  $\mu\text{m}$  pixel pitch, and operate from a +3.3 V supply. They are intended for slow-scan space applications.

Each sensor has two separate readout signal chains one analog and the other digital. The analog readout signal chain performs correlated double sampling (CDS) to suppress pixel fixed pattern noise, and double delta sampling (DDS) to suppress column dependent fixed pattern noise. The digital readout signal chain consists of a 1024 column parallel 10-bit single slope ADCS with built-in CDS. The ramp reference voltage is supplied by a single on-chip ramp generator. A block diagram of the chip architecture is shown in Figure 1. The analog outputs are VS\_OUT (signal) and VR\_OUT (reset), and the digital outputs are D\_out0 to D\_out9. The analog and digital readout chains are separated by the pixel array. Each imager can be operated in analog or digital readout mode. Layout of the 1kx1k CMOS APS with on-chip ADC is shown in Figure 2.

Testing results show a conversion gain of 10  $\mu\text{V}/\text{electron}$  and a signal saturation level of 600 mV for the photogate based image sensor, measured through the analog signal chain. The photodiode based sensor was found to have a 2.1  $\mu\text{V}/\text{electron}$  conversion gain, a signal saturation level of 620 mV and a dark current of 14.8 mV/see. When operated in analog mode, the photodiode based sensor consumes 60 mW and 80 mW in digital mode. Figure 3 shows a full 1kx1k image from the photodiode based sensor operated in analog mode. NTSC operation has been demonstrated within a window subsection of the chip.

Further testing results including dark current of photogate based sensors, quantum efficiency, signal-to-noise ratio, and maximum pixel rate of the image sensor will be presented. The analog readout circuit and the 10-bit single slope ADC of the imager will be explained in more detail, and issues particular to CMOS AI% design in submicron processes in terms of yield, crosstalk, and dynamic range will be explored.