

RADIATION ISSUES ASSOCIATED WITH THE INSERTION OF COMMERCIAL TECHNOLOGIES IN SPACE SYSTEMS

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ABSTRACT

In this paper we discuss radiation effects issues that have become important for NASA programs in the last few years. Particularly critical is the increasing usage of commercial off-the-shelf (COTS) devices and circuits in interplanetary missions that experience significant exposure to radiation. Demands for increased performance levels in spacecraft systems will drive the insertion of the latest electronic and photonic devices. Advances in electronics to achieve high performance will result in scaling (miniaturization) of devices, which, in turn, will lead to increased radiation vulnerability in many cases. These issues are discussed within the context of recent technical examples of challenging radiation effects problems.

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INTRODUCTION

The radiation effects and testing programs in place at the Jet Propulsion Laboratory support the insertion of traditional, advanced and emerging microelectronic and photonic technologies in NASA systems through research and testing that enhances the radiation hardness assurance (RHA) of these technologies. With the decreasing availability of radiation hardened electronics and the new NASA paradigm of faster, more aggressive and less expensive space missions, there has been an increasing emphasis on using high performance commercial microelectronic parts and circuits in NASA spacecraft. The use of commercial parts and circuits (often referred to as commercial off-the-shelf (COTS)) in space systems poses many potential reliability and radiation problems.

In the case of reliability phenomena, one can take advantage of other high volume, high reliability applications, such as automotive and medical, to leverage statistical measures of reliability, minimum cost and quick schedule, but radiation represents a unique requirement not encountered by other high volume application areas. In addition, the downturn in DoD hardened electronic part development, testing and acquisition has resulted in reduced availability of radiation hardened or even radiation tolerant electronic parts. The rapid evolution of traditional circuits, such as microprocessors and memories, is driven by intense competition in the private sector, and these advances, primarily due to scaling effects, often result in increased vulnerability to radiation. In addition, radiation testing which reveals that a particular generation of parts is appropriate for certain dose ranges, may be rendered irrelevant by the introduction of next-generation versions and the disappearance of the radiation tolerant parts from the market place. The introduction of emerging technologies that promise greater performance without increased power, weight or volume may have completely unknown radiation effects behavior that must be established through testing. In this paper, we present radiation testing results that are relevant to these issues.

ENHANCED LOW DOSE RATE EFFECTS IN BIPOLAR CIRCUITS

Relatively simple bipolar circuits such as operational amplifiers and comparators, form an essential part of many electronic circuits, hybrids and systems. Such devices will continue to play an integral role in the functionality of advanced spacecraft subsystems and instruments. Thus, their radiation response will influence the ability of a spacecraft and its instruments to survive the hostile space radiation environment.

Recently, it has been established [1-10] that many bipolar integrated circuits are much more susceptible to ionizing radiation at low dose rates (0.001 to 0.005 rad(Si)/sec) than they are at the high dose rates typically used for radiation testing of parts in the laboratory. Since the low dose rate regime is equivalent to that encountered in space, for these devices the standard laboratory radiation test at moderate to high dose rates is no longer conservative. The seriousness of this problem has led the Air Force to issue an Alert Concern for this effect. Because of the greater radiation sensitivity at very low dose rates, the only way to provide radiation hardness assurance to designers is to perform a radiation test at low dose rates which by its nature is very time consuming. Consequently, it is imperative that an RHA test be developed which can be performed at moderate to high dose rates. Because the physical mechanism for the enhanced low dose rate effect is not yet completely understood, it is not possible to propose a reliable RHA test. Herein, we will merely provide some examples of this effect, which serve to emphasize the seriousness of the enhanced low dose rate susceptibility problem.

Initial work [1] on the enhanced low dose rate (ELDR) effect suggested that as the dose rate was decreased, the enhancement effect saturated at around 10 rad(Si)/s and did not become any stronger at lower dose rates. However, expanded studies [2-10] of the ELDR effect clearly indicate that for many devices, saturation, if and when it occurs, must come at very low dose rates. For example, Figure 1 shows how input offset voltage, V_{os} , of the LM324 operational amplifier depends on total dose at different dose rates. Note that while there is little change in V_{os} for dose rates as low as 0.005 rad(Si)/s, there is a dramatic decrease in offset voltage at low doses when the LM324 is irradiated at 2 mrad(Si)/s. The change in V_{os} may come at even lower doses if one were to expose the part at 0.001 rad(Si)/s. To understand how impractical an RHA test becomes under these conditions, suppose that a mission has a total dose requirement of 15 krad(Si) and testing must be done at 0.001 rad(Si)/s to obtain the lowest failure dose because of the type of behavior shown in Figure 1. In order to test to the mission requirement, the radiation exposure would last for nearly 6 months, a test time that would be prohibitive for many fast, aggressive flight projects.

Studies of the response of individual bipolar transistor types to different dose rates have shown that the problem is most severe for *pnp* transistors used in many linear circuits with conventional junction isolation. Damage in *pnp* devices can be 6 to 7 times greater at low dose rates than at high dose rates [4]. In contrast, *nnp* transistors from the same fabrication processes are generally not sensitive to dose rate effects below approximately 1 rad(Si)/s. Thus, circuits which use both types of components may exhibit different failure modes at low and high

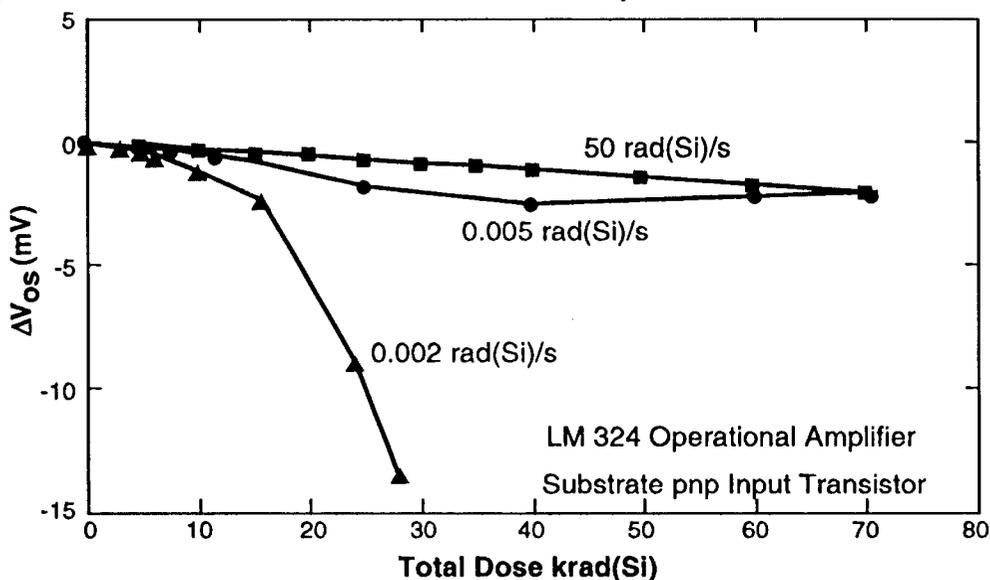


Figure 1. Degradation of input offset voltage of the LM324 operational amplifier at various dose rates.

dose rates because of the different amount of relative damage that occurs in the two types of component transistors at low dose rates. In addition, different bipolar circuits that use varying mixes of the two transistor types can exhibit different failure characteristics, even for parts from the same process line. For example, Figure 2 compares input bias current degradation of two bipolar circuit types with similar input stage designs from the same manufacturer. Dose rate effects are relatively easy to evaluate in linear circuits with *pnp* input transistors because the input bias current provides a straightforward way to measure input transistor gain degradation. For the LM111 and LM324 shown in Figure 2, both devices use substrate *pnp* transistors, but the typical value of input bias current is three times greater for the LM111 than for the LM324. Although both circuits are more damaged when they are irradiated at low dose rate, degradation in the LM324 is much greater. Damage in the LM111 saturates at relatively low total dose levels, reducing the significance of enhanced damage. Input bias current of the LM324 continues to degrade at low dose rate as the radiation level increases, and it is well above the specification limit even at 10 krad(Si). Even higher damage occurred in this device at 0.002 rad(Si)/s, although this is not shown in Figure 2. These results show that large differences can occur between different circuit types produced by the same manufacturer, and that it is risky to make blanket assessments about dose rate effects on the basis of limited test data.

It has also been shown [4] that the same device type from different manufacturers can exhibit significantly different ELDR effects. For example, Figure 3 shows input bias current degradation for LM111 voltage comparators, which use substrate *pnp* input transistors, procured from three different vendors, and tested at two widely different dose rates. For two of the manufacturers, damage of the input transistors is about six times greater at low dose rates so that they exhibit rapid increases in input bias current at the lower dose rate of 0.005 rad(Si)/s. Devices from the third manufacturer (vendor A) show only a small increase in damage at the lowest dose rate, even though the geometry of the input transistors of this vendor are identical to that of the vendor with the highest damage at low dose rates. Thus, determination of the extent of the ELDR effect for a particular device type is not sufficient to provide RHA if a different vendor is selected than the one used for radiation test samples.

Bipolar circuits with JFET input stages have also been found to be sensitive to the ELDR effect. Illustrative results are shown in Figure 4 for two operational amplifiers, OP-42 and OP-249. Note the dramatic difference in radiation sensitivity as the dose rate varies from 100 rad(Si)/s to 5 mrad(Si)/s. More recent results have shown that the onset of the change in offset voltage occurs at an even lower dose as the dose rate is decreased to 1 mrad(Si)/s.

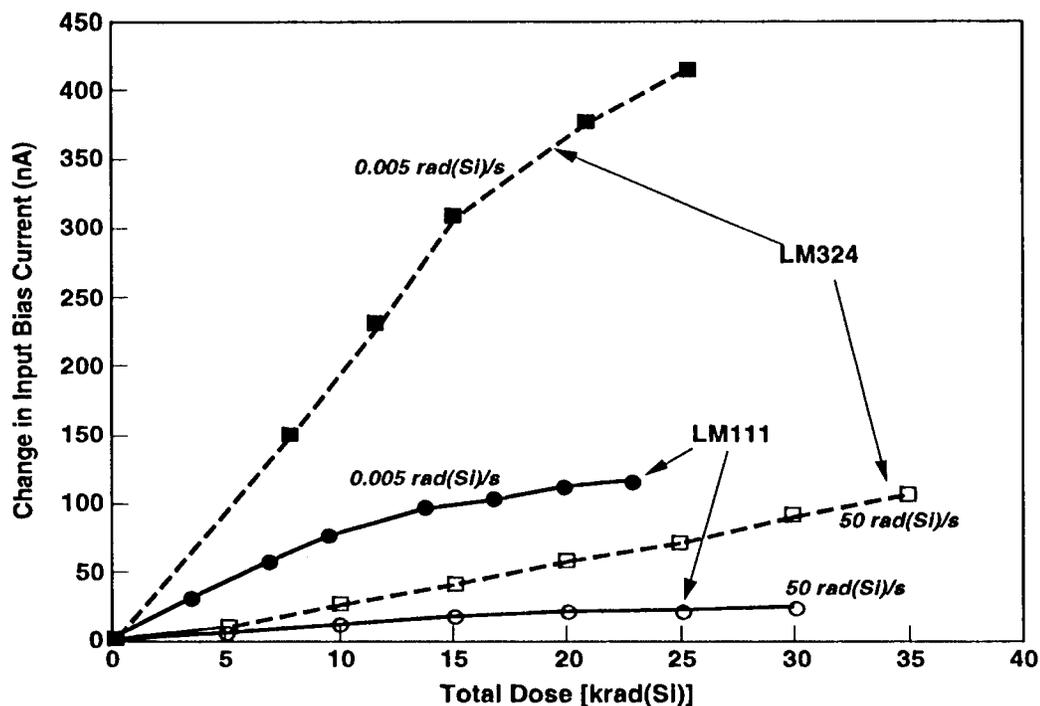


Figure 2. Degradation of input bias current of two different bipolar circuits with similar input stages from the same manufacturer.

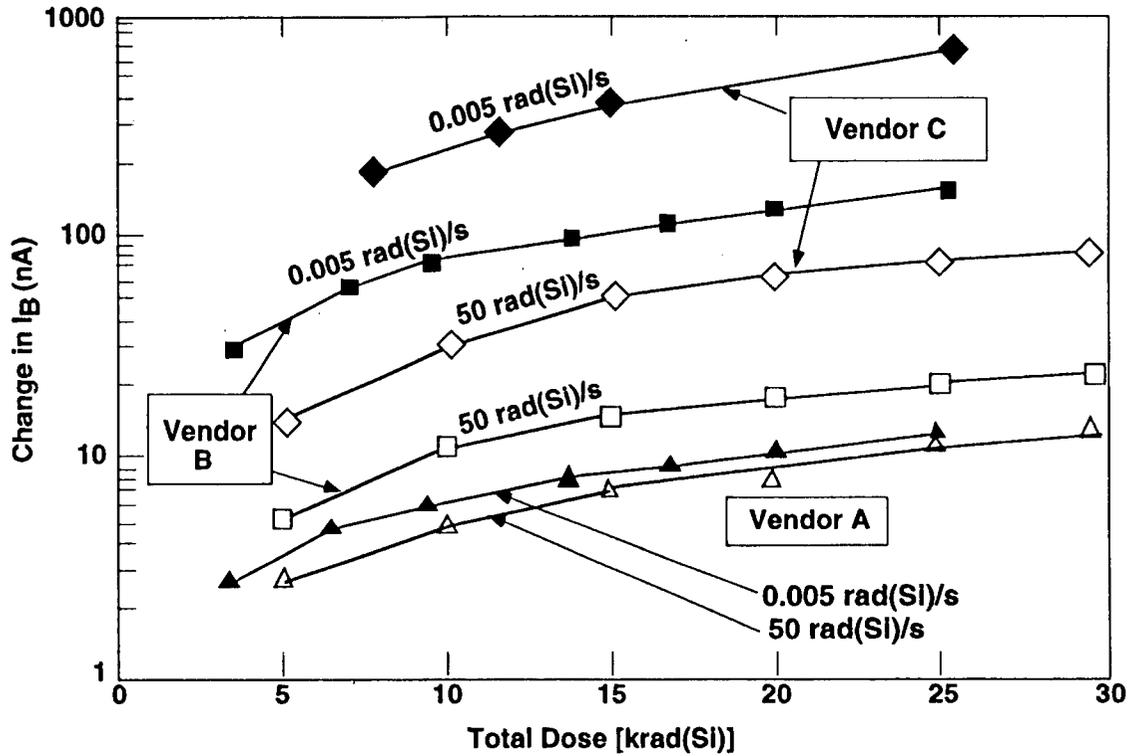


Figure 3. Total dose degradation of LM111 comparators from three different manufacturers at high and very low dose rates.

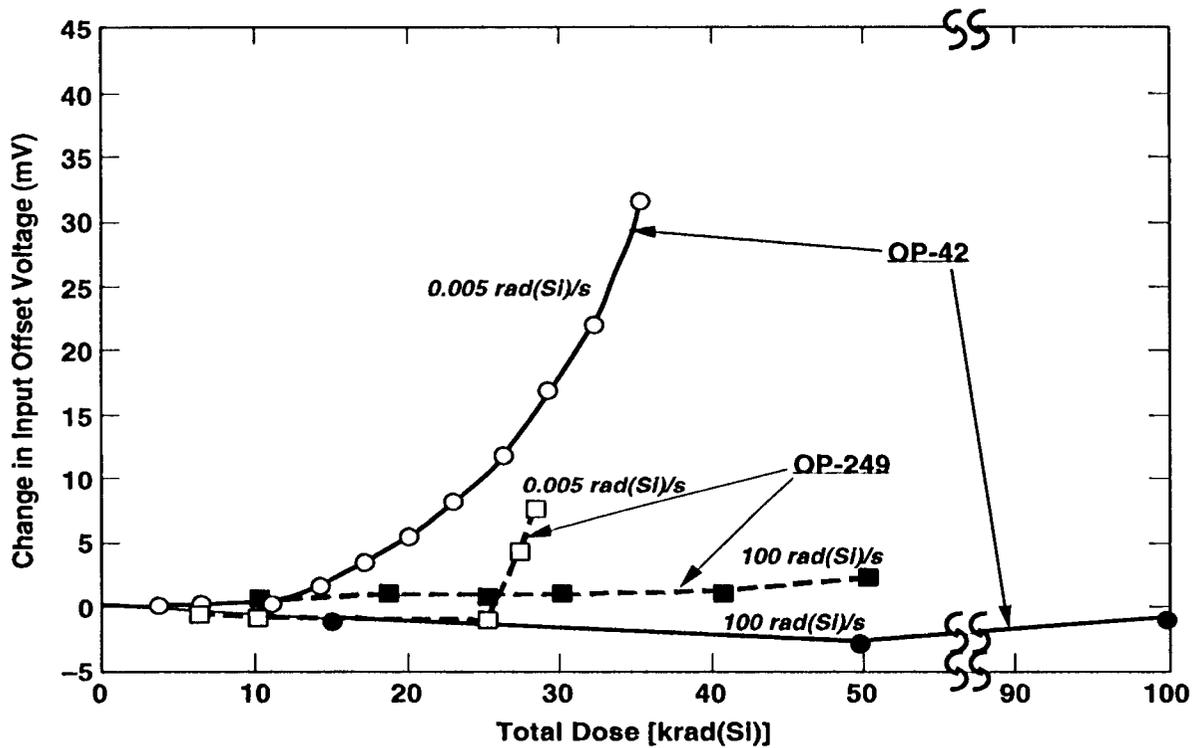


Figure 4. Effect of dose rate on the response of two operational amplifiers to irradiation.

The remaining challenge for the radiation effects community is to devise an RHA test for the ELDR effect other than direct testing at very low dose rates, an expensive and time consuming alternative which is unacceptable, but necessary in some cases at this time. While the physical mechanism of the ELDR effect has not been completely defined, promising models are being developed [3,6] that are associated with the dynamics of radiation-induced electrons and holes in thick oxides with weak electric fields. One of the approaches suggested by these models is irradiation at moderate to high dose rates at elevated temperature. Recent work [3,7] has shown that the increased damage at low dose rates can be at least partially reproduced by irradiating at high dose rates and at 60°C to 100°C for certain device types from particular vendors. Typical results are shown in Figure 5 for LM111 comparators irradiated at 90°C at different dose rates. Note that at a dose rate of 1 rad(Si)/s, the damage enhancement approaches that observed at room temperature at a dose rate of 5 mrad(Si)/s. Thus, irradiation at a moderate dose rate (0.1 to 1 rad(Si)/s, quick enough for most NASA total dose requirements) and an elevated temperature is sufficient to approximately simulate the ELDR effect.

Unfortunately, it is not clear what the temperature should be for a given process technology, or whether or not saturation of the increase in damage will occur at a

reasonable temperature. In addition, if one raises the temperature further to increase the damage, the opposite may occur once damage begins to anneal. We have recently observed this to be the case with the LM111 comparators. When the irradiation temperature was increased to 135°C the damage observed at 6 rad(Si)/s was significantly less than that shown in Figure 5.

Until the high temperature RHA test is better defined, another way to deal with this problem is to require tests at two different dose rates, selecting the lower dose rate so that it is sufficiently high to allow tests to be completed in days or weeks instead of the extremely long time periods imposed by the very low dose rates discussed above. Although this is not a substitute for doing tests at very low dose rates for devices that have severe enhanced damage at low dose rate, it is a more pragmatic way to identify devices that have minimal sensitivity to dose-rate effects. JPL has implemented this approach for several devices, using 0.02 rad(Si)/s for the lowest dose rate.

MIXED SIGNAL DEVICES

Mixed signal devices, such as analog to digital converters (ADCs), pose particularly difficult RHA problems, especially for flight environments where the majority of the dose is due to protons. For devices contain

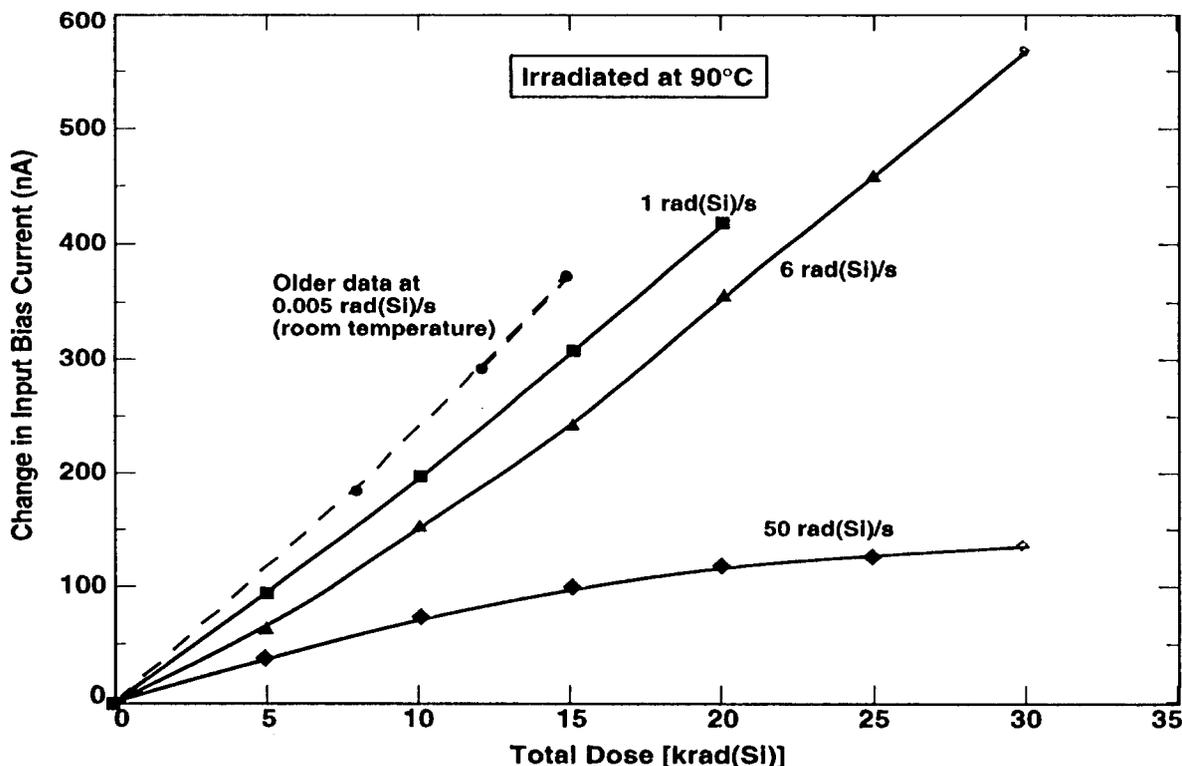


Figure 5. The effect of different dose rates on of LM111 comparators irradiated at 90°C.

ing both CMOS and bipolar elements (BiCMOS), there can be at least four radiation-induced failure modes:

1. Failure due to trapped hole charge in the gate and field oxides of MOSFET devices.
2. Failure due to interface state effects at the SiO₂/Si interface of MOSFETs.
3. Failure due to the ELDR effects in bipolar sections of the device.
4. Failure due to displacement damage effects in bipolar transistors caused by protons.

In addition, the failure mode will depend on the specific environment and how the device is operated while it is undergoing exposure. Thus, it is difficult to draw general conclusions about the hardness levels of such devices, especially when they are commercial products.

To illustrate the potential difficulties arising from the variety of possible failure modes in BiCMOS devices, we show in Figure 6 a summary of detected failure levels and modes for three different ADCs. The CS5016 ADC, a 16-bit CMOS device, behaves as expected for a CMOS device in that failure at high dose rate occurs

at a much lower dose level than failure at very low dose rates. At VLDR the trapped hole charge has time to anneal during exposure so that there is little net effect of this failure mechanism. The BiCMOS 12-bit MX7672 exhibits failure mode behavior similar to the CS5016 indicating that the CMOS elements dominate total dose failure under the conditions of these irradiations rather than the bipolar portions of the circuit.

In contrast, note that the BiCMOS AD7872 14-bit ADC has complex failure modes depending on the dose rate. Not only does the relative dose range over which parametric degradation is observed change with dose rate, but in addition, there is not a trend with dose rate in the observed functional failure levels. The results suggest that the HDR failure is determined by a more sensitive response in the CMOS sections, while the failure at very low dose rates is dominated by the bipolar portions of the device. Thus, the failure mode depends on the radiation environment for part exposure.

Another example of the difficulties that can be encountered when using relatively complex COTS devices that may contain both bipolar and CMOS elements is illustrated by comparing three different COTS devices from the same manufacturer (not necessarily the same process line). First, recall from Figure 3 that the LM111

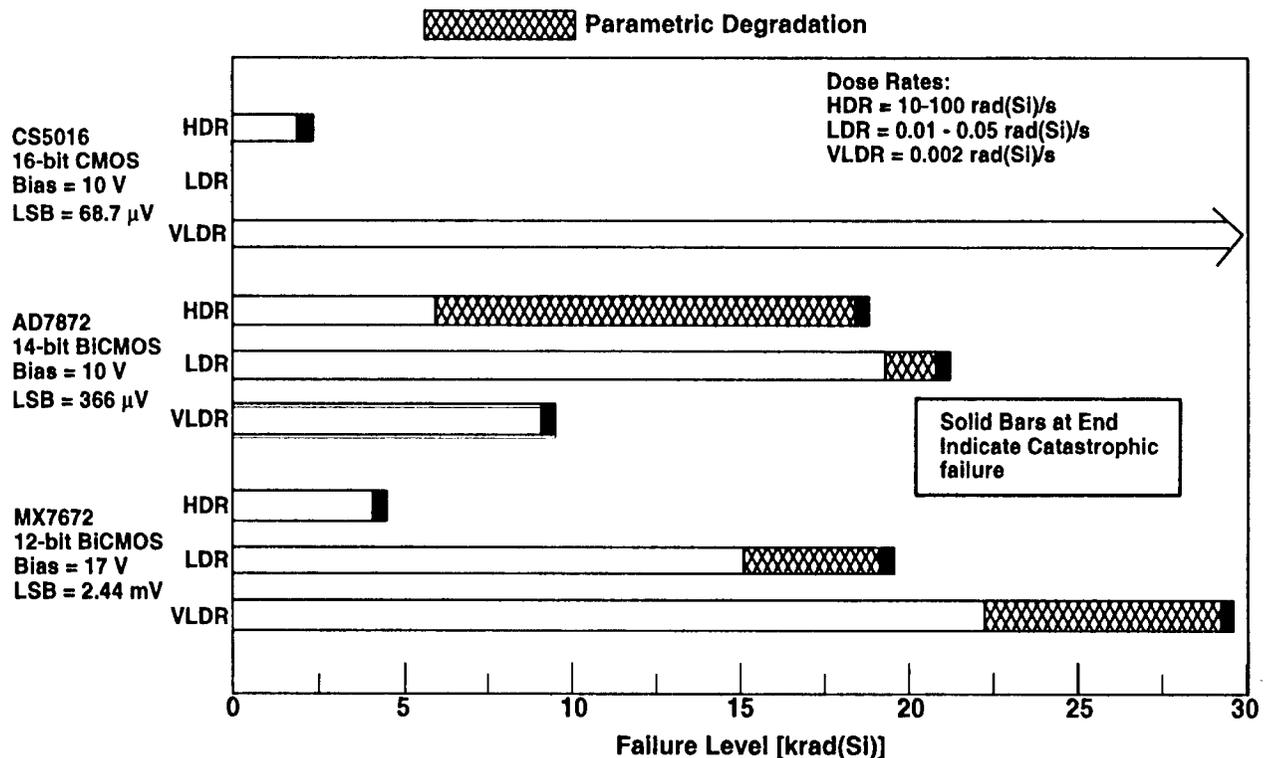


Figure 6. Dose rate dependence of failure modes in three analog to digital converters.

comparator from Vendor A showed comparatively little ELDR sensitivity.

In contrast, results are shown in Figure 7 for the AD652 voltage to frequency converter (VFC) from the same manufacturer. For this second device type, a very strong ELDR effect was seen in the bipolar sections of this complex commercial device. Note that the percent change in linearity exceeds the manufacturer's specification at about 7 krad(Si) when the part is irradiated at 5 mrad(Si)/s, but that this spec level (0.02%) has not yet been reached at a dose of 50 krad(Si) when the device is irradiated at 50 rad(Si)/s.

The third example from the same manufacturer is shown in Figure 8 for the AD847 operational amplifier fabricated in a junction-isolated complementary bipolar process. In contrast with the AD652 in Figure 7, the AD847 does not exhibit the characteristics of a bipolar part which is sensitive to the ELDR effect. Quite to the contrary, it behaves as one would expect for a CMOS part. The total dose effect is greater for high dose rate under bias. If the bias is removed and the part irradiated at high dose rate little change in offset voltage is observed. Similarly, if the part is irradiated at low dose rate, biased or unbiased, essentially no change in offset voltage is seen. These latter observations agree with the strong annealing observed in this device following biased, high dose rate exposure. All of these attributes are typical of a CMOS part which is sensitive to the effects of trapped hole charge deposited in oxides during radiation exposure.

The contrasting behavior of the three bipolar parts discussed above, which are all from the same manufacturer, clearly demonstrates the potential hardness assurance problems that can be encountered with COTS devices. The ability to predict radiation response of COTS devices from general models of expected behavior will continue to be a risky process. Strong variations in radiation behavior combined with an inability to provide traceability for most COTS parts, suggests that more intensive radiation testing will be required for future space applications of COTS devices and circuits.

DISPLACEMENT DAMAGE: A "NEW/OLD" PROBLEM

Early, pioneering studies [11] of radiation effects in semiconductors were concerned primarily with displacement damage, the disruption of the semiconductor lattice by a relatively massive particle such as a proton or neutron. Kinetic energy is transferred from the bombarding particle to a lattice atom to an extent that the atom is ejected from its lattice site and often has enough energy to displace additional secondary and tertiary lattice atoms. These displaced atoms can come to rest at interstitial and vacancy sites within the lattice, or they can become trapped at impurities or other types of defects in the lattice. When in such locations, the displaced atoms introduce levels in the semiconductor forbidden energy gap in the same manner as dopant impurities, except that these damage levels are usually relatively deep in the gap. The accumulation of these deep levels with greater damage

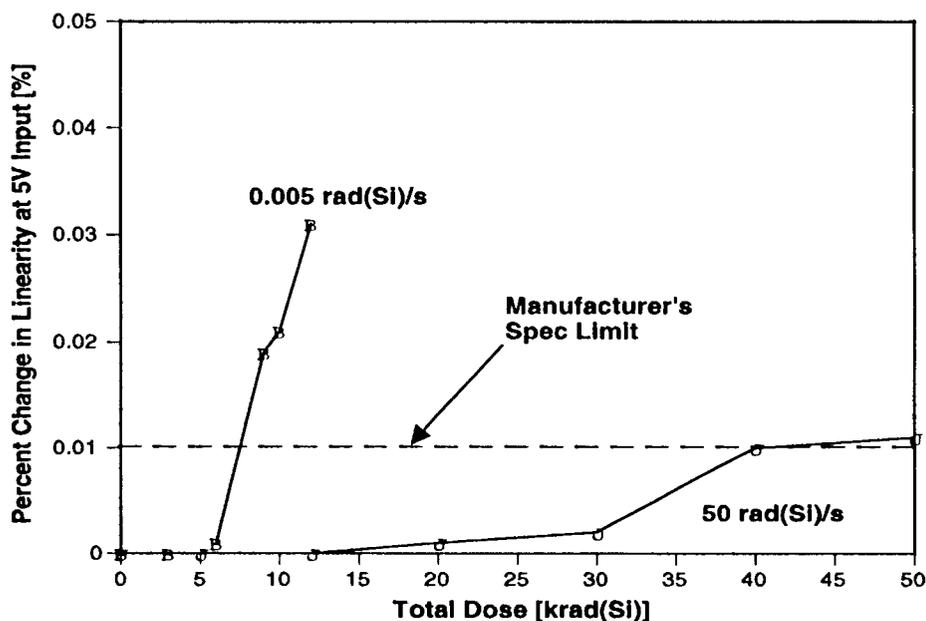


Figure 7. Change in linearity of the AD652 voltage to frequency converter as a function of dose rate. Note that the manufacturer's specification is exceeded after 7 krad(Si) at low dose rate.

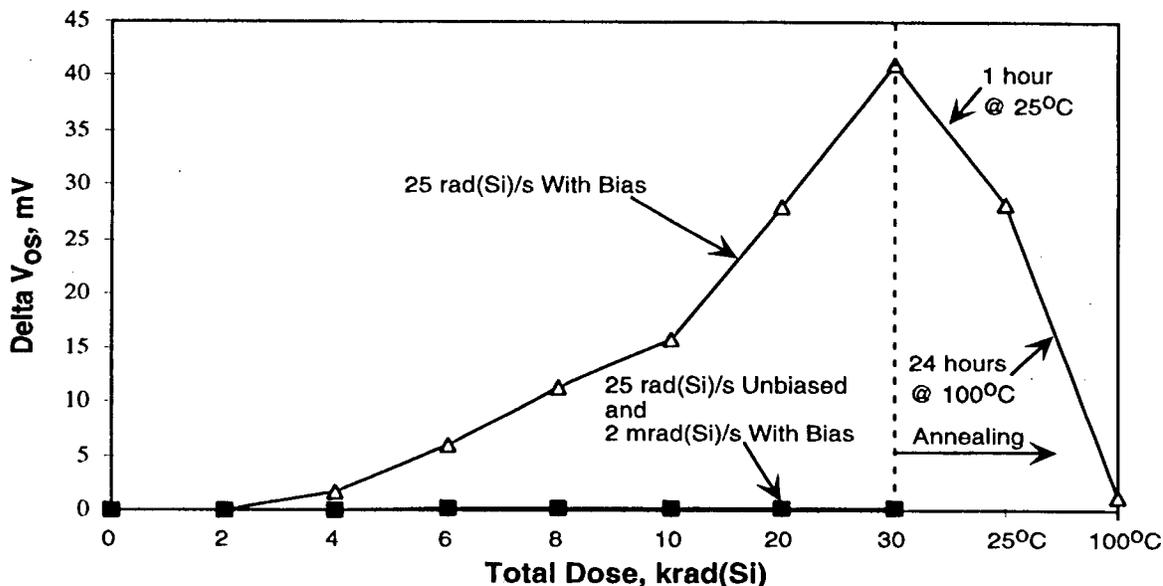


Figure 8. Change in input offset voltage of AD847 low power operational amplifier for three irradiation conditions: exposure at 25 rad(Si)/s under bias, 25 rad(Si)/s with no bias, and 2 mrad(Si)/s with bias. Note the strong annealing of the high dose rate damage.

causes minority carrier lifetime degradation, mobility degradation and carrier removal in the semiconductor resulting in an alteration in electrical and optical properties of the material, and changes in device operating characteristics. For radiation environments that have not included high neutron fluences (nuclear weapon), those device types that have been significantly affected by displacement damage include solar cells and high gain bipolar transistors due to lifetime degradation. It is important to note that digital CMOS is not affected except at high levels of displacement damage where carrier removal and mobility degradation are significant.

Because the typical NASA mission radiation environment does not result in high levels of displacement damage, specific radiation requirements governing the allowable displacement damage have not been included in most requirements documents for the past several years. Rather, the important radiation issues for NASA have centered around single event effects (SEE) and total ionizing dose (TID) effects, primarily because of the sensitivity of CMOS devices and circuits to these effects. However, in recent years displacement damage has had a resurgence as a relevant radiation hardness assurance (RHA) issue for NASA space systems because of the increased usage of high performance circuits, such as high precision voltage reference devices and high resolution analog to digital converters (ADCs), and new technology devices such as photonics (light emitting diodes (LEDs), laser diodes, phototransistors and photodiodes), which are sensitive to displacement damage.

Many of these devices exhibit a sensitivity to both displacement damage and deposited ionizing energy (TID), and this has resulted in confusion in the imposition of radiation requirements and corresponding radiation testing. A recent important example is the use of 4N49 optocouplers in various space systems. In spite of the fact that Co⁶⁰ testing of 4N49 optocouplers has indicated that they do not degrade significantly at levels like 100 krad(Si), there have been observed failures of these devices on the TOPEX/Poseidon (T/P) satellite at doses less than 30 krad(Si). This disparity arises because Co⁶⁰ produces essentially no displacement damage, but the T/P radiation environment is dominated by protons at the optocoupler location (behind considerable shielding), and the LED and phototransistor making up the 4N49 are both sensitive to proton-induced displacement damage [12]. Typical 200 MeV proton irradiation results verifying this displacement damage susceptibility are shown in Figure 9 at three different LED drive currents, which correspond to the drive currents used in the TOPEX/Poseidon applications. Note that the current transfer ratio (CTR) of the 4N49 optocouplers degrades rapidly with 200 MeV proton fluence. As indicated by the marker in Figure 9 for the estimated proton fluence seen by T/P after two years (the failure point for the most sensitive T/P application), the normalized CTR has degraded to about 0.3 of its pre-irradiation value.

Another example of a sensitivity to displacement damage is shown in Figure 10 for the Analog Devices AD2710 high precision voltage reference. Note that the

specified sensitivity of the device is 0.0025%. This level of precision results in a strong susceptibility to radiation damage, and in particular, if the internal bipolar gain of transistors in the AD2710 on-chip circuit changes by even a small amount due to displacement damage, the device will be out of specification. This is indeed the case as shown in Figure 10 where the AD2710 exhibits a much greater sensitivity to 200 MeV proton bombardment than it does to Co^{60} irradiation. Thus, if this device were tested only with Co^{60} , the standard method of testing parts to meet mission requirements, the results would suggest a greater resistance to radiation than is actually the case. The important message that emerges from these studies is that mission assurance and electronic design engineers must be cognizant of possible sensitivities to displacement damage and require that devices and circuits that may exhibit this vulnerability be tested with protons in addition to Co^{60} gamma rays.

NEW RADIATION PHENOMENA IN ADVANCED DRAMs

Perhaps more than any other class of advanced microelectronic device, DRAMs represent a challenge with regard to their insertion in space systems. Advanced DRAMs are particularly attractive for mass storage systems on board spacecraft and satellites, so that it is tempting to incorporate them in large memory designs. How-

ever, because the radiation tolerant space applications market is vanishingly small compared to the commercial market for DRAMs, the designer is restricted to using commercial devices with little chance of device or process modification to accommodate radiation requirements. Thus, it is imperative to perform extensive radiation testing to determine if the commercial device under consideration will meet specific mission requirements. Unfortunately, under the pressure of competition in the commercial market place, DRAM advancements are proceeding so rapidly that by the time one has expended considerable (SEE) and Total Ionizing Dose (TID) effects radiation tests, the DRAM under test is obsolete and essentially unavailable. In addition, scaling effects in newer devices can render radiation test results inapplicable to the latest DRAM technology. Add to this the new phenomena we discuss below and one is faced with a very challenging assurance problem for space applications of advanced DRAMs.

In the past few years, several studies [13-23] of DRAMs and SRAMs have revealed new radiation effects phenomena that can affect solid state memory performance in radiation environments. As we will show, technology advancements in the form of scaling to achieve reduced feature sizes and greater memory cell densities will probably exacerbate these effects.

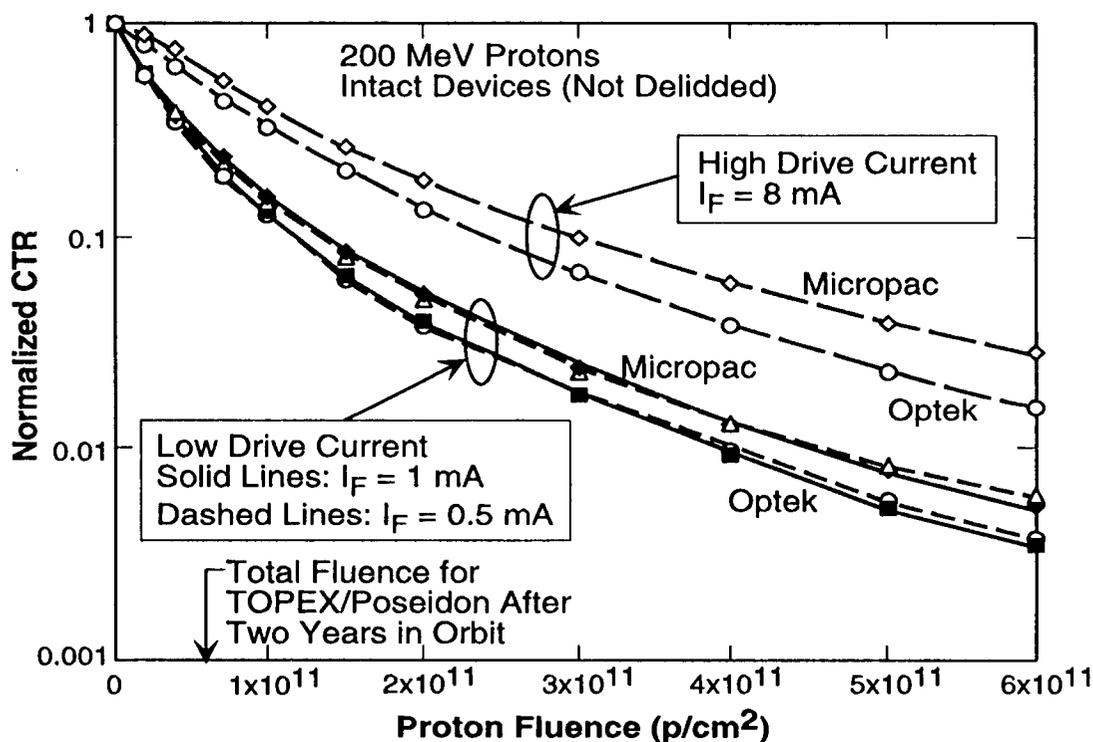


Figure 9. Proton-induced degradation of 4N49 optocouplers.

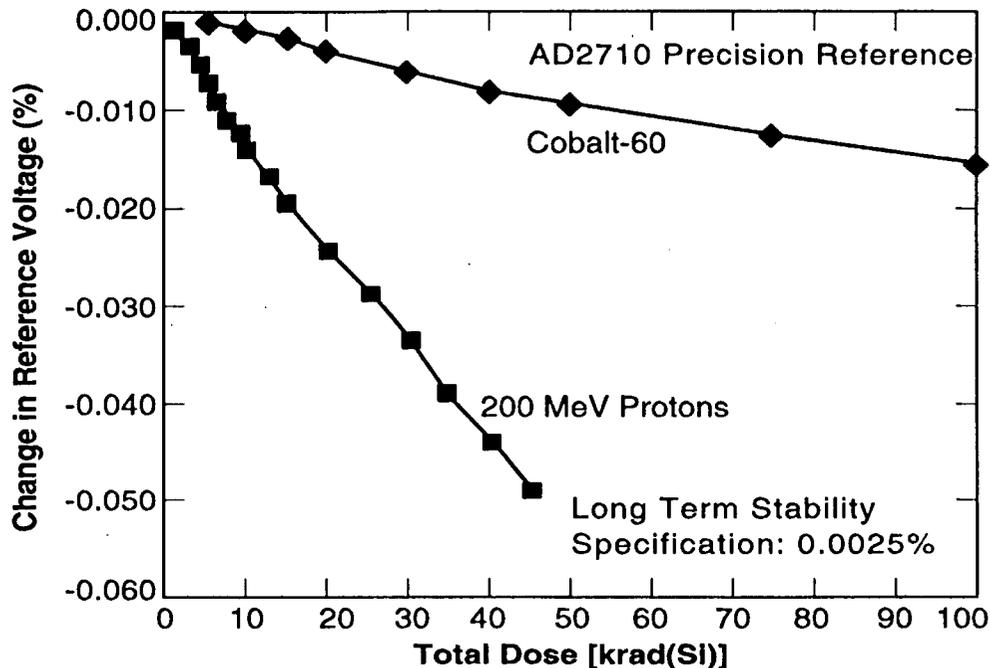


Figure 10. Comparison of Co^{60} and 200 MeV proton degradation of a high precision voltage reference device.

State-of-the-art DRAMs are complex devices that often incorporate much more circuitry than simple DRAM cells and the necessary peripheral circuitry for accessing and writing/reading these cells. In particular, several operating modes may be built into the device in order to facilitate various test modes of operation. Normally a command sequence is used to place the DRAM in a test mode, but recent SEE testing [13] has revealed that an energetic heavy ion can throw the DRAM out of normal operating mode and into one of its test modes if the particle hits the circuit device that controls operating mode. These so called Single Event Functionality Interrupt (SEFI) events render the device inoperable until it is placed back in normal mode by specific commands. Unlike a traditional Single Event Upset (SEU), which results in a single error in one logic element, SEFIs manifest themselves as bursts of large numbers of errors due to a single particle hit. Thus, although the interaction cross section for a SEFI is less than that for a typical SEU, the effect has much greater impact on DRAM functionality. Fortunately, the effect is not permanent and can be removed by commanding the device to reenter standard operating mode. Thus, it is not permanently catastrophic in contrast with an important new class of single event hard errors we will discuss next.

During the last few years, several laboratories have observed single particle induced errors which are permanent in nature in contrast with the more traditional

SEU event which is a temporary change in logic state of a circuit logic element. These "stuck bits" or "hard errors" remain in the device despite power cycling or reloading of a memory. More recently, work at various heavy ion accelerators [15-18,20-22] has led to a tentative identification of the nature of these hard errors. Earlier work [15,16] suggested that the only mechanism for hard error formation was a so-called "microdose" effect. This effect is the single particle/single transistor equivalent of a Co^{60} or total dose irradiation, and is due to microscopic ionization damage from the passage of a single ion (or a small number of ions) within the transistor gate region. As the result of continued scaling, transistors in advanced memories are now small enough so that a single ion can deposit enough ionizing energy to create the equivalent of a "total dose" effect within a single transistor. This effect is primarily important for DRAMs or 4-transistor memory cell SRAMs that use dynamic storage, but is not expected to be significant for random logic or 6-transistor memory cell SRAMs. In addition, it has been established that at least some fraction of these microdose-induced hard errors will anneal, as one might expect based on the characteristics of typical TID damage. Thus, these hard errors will recover slowly, unlike the second type described below.

The second mechanism causes catastrophic shorting of the gate oxide in the specific transistor that is struck by the energetic heavy ion [18]. It is attributed to

gate rupture, and occurs because the high charge density produced by the ion track reduces the electric field needed to cause dielectric breakdown of the gate insulator. The result is destructive, permanent damage caused by the combination of applied field and heavy ion strike. Similar effects have been studied for several years in power MOSFETs [24,25], but they have only recently been observed for lower voltage transistors in VLSI devices. Theoretically, gate rupture can occur for random logic as well as memories, and may prevent the use of extremely scaled (miniaturized) devices in space. Note also that this effect is similar to the anti-fuse SEDR effect described above for FPGAs.

Heavy ion data, shown in Figure 11, taken on commercial 4-Mb DRAMs illustrates the striking difference between the two hard error mechanisms [18]. The distribution of lost bits as a function of DRAM retention time for iodine bombardment agrees with observations after total dose irradiation in which the distribution "walks" to the left in Figure 11 so that fewer and fewer bits have long retention times above the part specification of 360 ms at 45°C. In contrast, for gold bombardment two different types of data are observed. In addition to results similar to the iodine induced microdose distribution, the Au also causes permanent damage that is characterized by extremely short retention times, essentially zero. As in the case of power MOSFET gate rupture and

the FPGA rupture effect described above, the angular dependence of the permanent damage is unlike traditional SEU. The natural separation into "lost ones" and "lost zeros" is also suggestive of a permanent effect that requires a bias on the transistor to cause damage. This second mechanism is particularly important for several reasons: 1) it is permanent and does not anneal so that over the course of a long mission, these errors will accumulate; 2) this effect causes catastrophic failure of the transistor in which it occurs; 3) this type of hard error could occur in any MOS transistor with bias on the gate so that it will also affect microprocessors and random logic circuits which are not amenable to software-based error detection and correction; and 4) this effect will become worse with continued part scaling that is sure to take place as circuits with greater and greater performance are brought into the market place.

Total dose studies [21,26] of advanced DRAMs are also taking place in our laboratory and elsewhere. It has been determined that the mean retention time of a DRAM is a sensitive measure of total dose-induced degradation of DRAM performance [21]. More recently, total dose testing of advanced 64-Mbit DRAMs has been performed. Typical results are shown in Figure 12 for DRAMs from three manufacturers. It is important to remember that these are all commercial devices. Thus, the Samsung device has very good radiation tolerance.

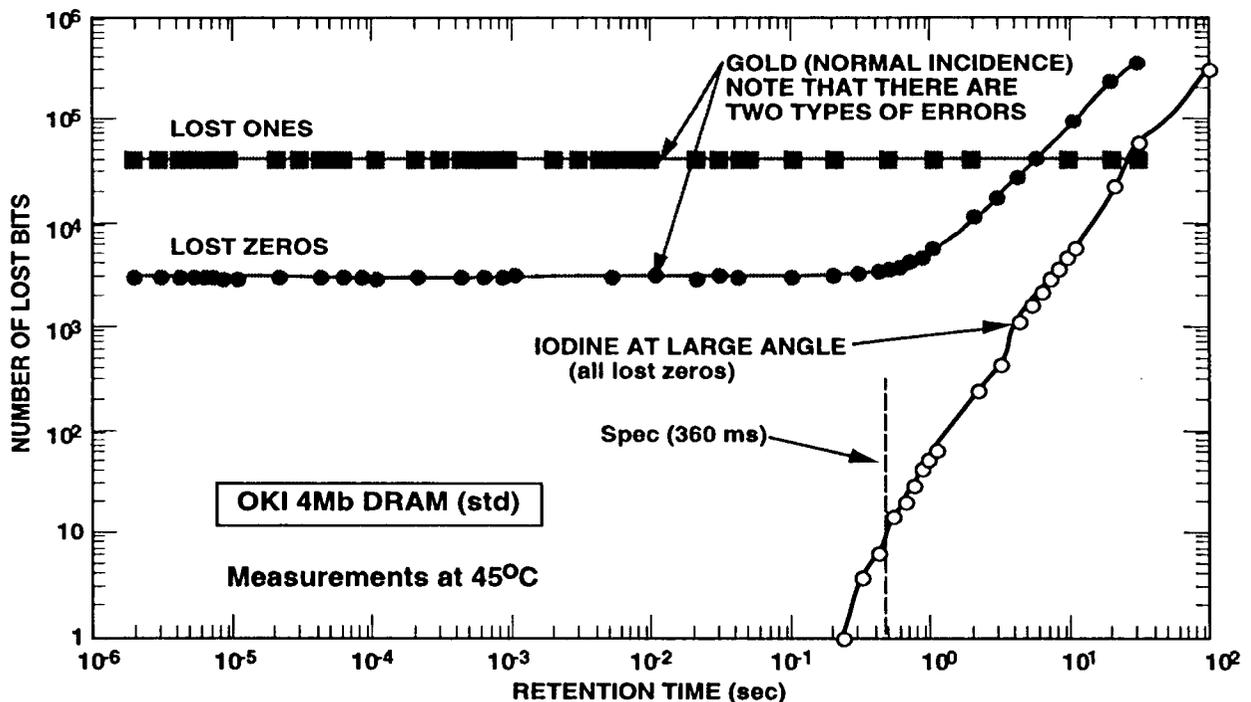


Figure 11. Retention time distributions for iodine ($LET = 0.6 \text{ pC}/\mu\text{m}$) and gold ($LET = 0.8 \text{ pC}/\mu\text{m}$) bombarded OKI 4 Mb DRAMs.

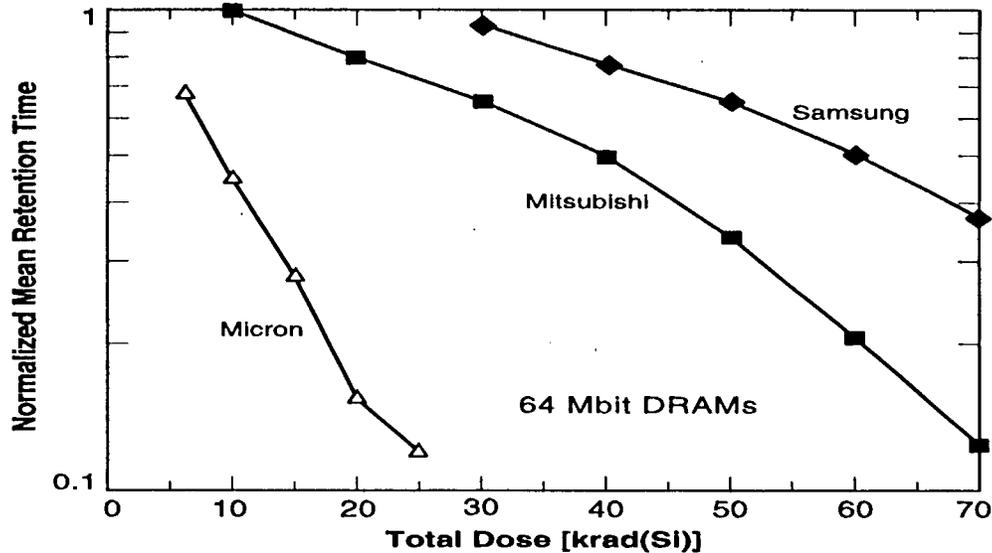


Figure 12. Median normalized retention time for three Co^{60} irradiated 64-Mbit DRAMs.

Finally, we wish to consider the effects of device scaling (miniaturization) on radiation hardness assurance. In the case of hard error mechanisms in scaled devices, JPL examined other 4 Mb DRAMs that had 20% smaller dimensions and thinner gate oxides compared with those discussed above. The scaled devices were more sensitive to the permanent damage effect in that the effect was observed for iodine at a lower LET than for gold. The damage thresholds, expressed in terms of the linear charge density deposited by the ions, are shown in Figure 13. The dashed line shows a prediction of the effect of future scaling changes, assuming that the threshold for gate rupture varies as the reciprocal of the square of the electric field across the oxide, using oxide fields typical of high speed scaling techniques.

In order to understand the implications of these results, one must take into account the distribution of the ions making up galactic cosmic rays (GCRs), which decrease rapidly for high linear charge densities. Above 0.3 pC/ μ m, the distribution falls abruptly by more than three orders of magnitude, the so-called iron ion threshold that is characteristic of the GCR spectrum. These results have been used to calculate the catastrophic hard-error rate for devices with different feature sizes, as shown in Figure 14. The error rate in Figure 14 is the number of failed devices for a VLSI circuit with approximately one million transistors. There is a pronounced difference in the error rate for the high speed scaling approach versus the low power scaling method because of the differences in the way the gate oxide field scales in each case. The very rapid increase in the error rate of the high speed scaling curve occurs when the threshold charge density falls be

low 0.3 pC/mm, where there is a large jump in the number of GCR particles. The curve suggests that it will be very difficult to use devices with 0.25 μ m feature size because of the hard error limit, and that devices optimized for low power operation will have a much lower error rate in space applications.

CONCLUSIONS

In this paper we have discussed important new radiation effects phenomena that will affect the radiation susceptibility of advanced microelectronic systems in spacecraft and satellites. Of particular concern are the radiation hardness assurance (RHA) issues associated with using commercial off the shelf (COTS) devices and circuits. Lack of process line and lot traceability and the intensive pressure of commercial competition lead us to the conclusion that extensive radiation testing will be necessary in the future, especially in the case of new advanced devices that employ a variety of basic circuit elements and transistor types in one device. In addition, we have seen that advances in performance in traditional electronic technologies, such as DRAMs and microprocessors, which are achieved through scaling (miniaturization) of feature sizes, will result in devices and circuits that are more sensitive to radiation effects. In closing, we wish to emphasize that care must be taken in the insertion of new, emerging technologies in space systems in order to avoid radiation effects problems that may jeopardize mission success. In many cases, the use of concurrent engineering to examine potential radiation problems at early design stages will catch problems before they reach a stage that will result in cost and schedule penalties to repair.

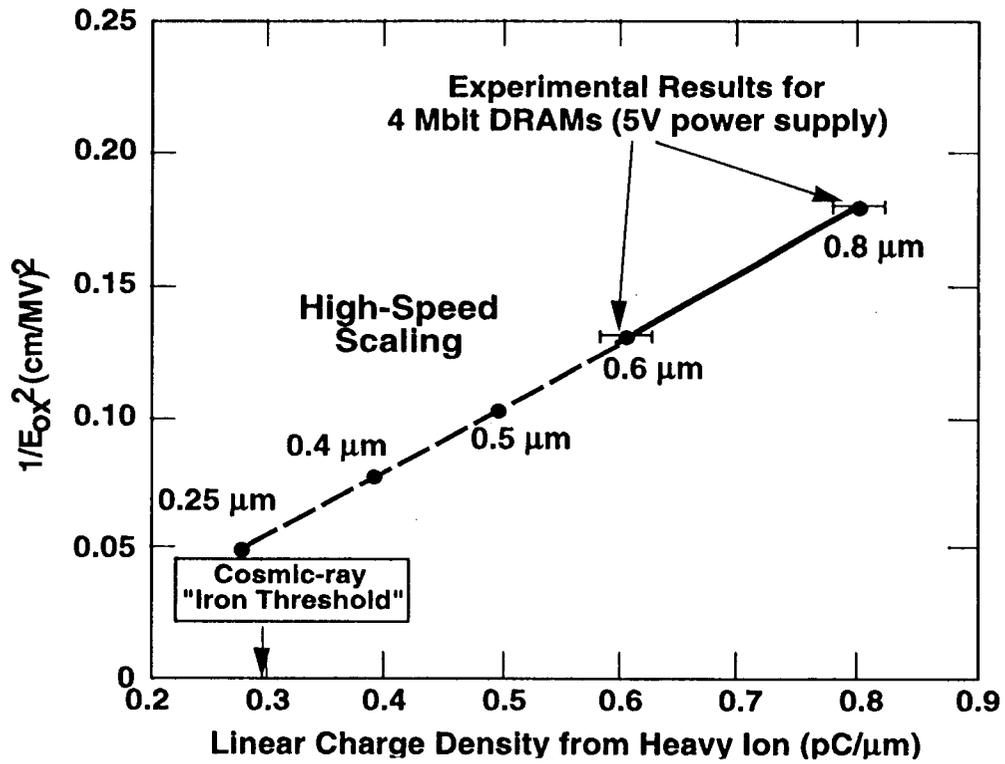


Figure 13. Effect of device scaling on hard error threshold for various feature sizes.

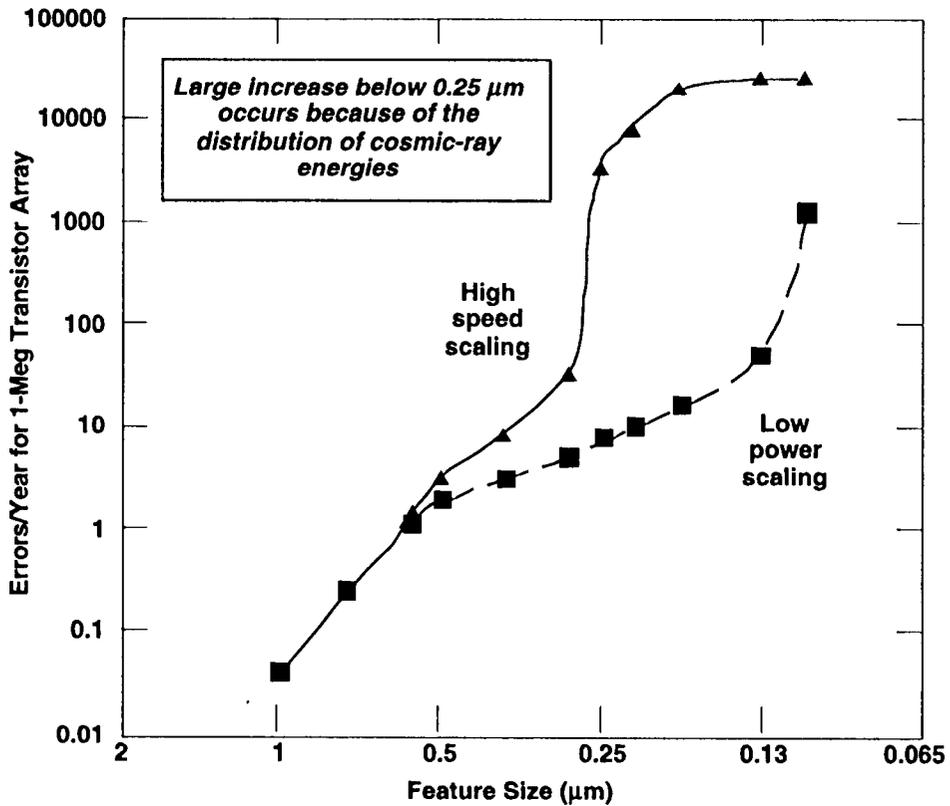


Figure 14. Hard errors induced by cosmic rays for a 1-M transistor array as feature sizes are reduced.

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