A Review of Chip Scale Package Assembled Reliability

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ABSTRACT

NASA Headquarters, code Q, has established the Advanced Interconnect Program (AIP) to address the NASA's common needs in electronic packaging for microspacecraft applications. The Jet Propulsion Laboratory was funded to address the quality and reliability of several high density electronic packaging technologies. Two key areas included Chip Scale Packaging (CSP) and Direct Chip Attachment (DCA) technology. In addition, DCA Chip-On-Board was selected for Mars Microprobe (MMP) soil exploration to meet its severe space and environmental constraints. Peak acceleration of 80 KGs and temperature down to -120 °C all favored the use of a relatively established COB technology. There are many issues with the CSP technology that are yet to be understood before its implementation. This paper will review technical issues that are associated with the CSP assembled reliability. Also, the objectives and future plans for a systematic characterization of microBGA assemblies quality and reliability will be presented.

OBJECTIVES

Background

In early 1995, the Jet Propulsion Laboratory formed a consortium to evaluate quality and reliability of ball grid arrays and to help in building the infrastructure for this technology. The NASA Code Q, Office of Safety & Mission Assurance (OSMA) funded JPL and each consortium team members furnished in-kind contribution by providing their internal resources and expertise. The consortium accomplished a great deal and answered many technical issues raised regarding the BGA technology in the start of the program in 1995 (References 1-2). It was recognized that wider acceptance of BGA technology will afford NASA as well as consortium industries inexpensive access to this technology and support miniaturization thrusts for their next generation applications. BGA is now becoming an acceptable alternative for high density applications.

There are further needs, however, in the development of infrastructure supports, improvement in design and functions, optimization for achieving higher reliability, and inspection techniques that could be used to characterize level of solder joint cracks and damages. Ability to assess quality of solder joint by inspection and assure its reliability is critical for NASA's low volume, high reliable missions.

The emerging CSP packages are competing with the bare die assembly. MicroBGA packages of CSP technology with many characteristics of BGAs now are at the level that BGAs were

about three years ago. This technology along with DCA are being investigated under the NASA's AIP program (References 3-4). DCA COB was selected for Mars MicroProbe (MMP) soil exploration to meet its severe space and environmental constraints. Peak acceleration of 80 KGs and temperature as low as -120 °C all favored the use of a mature COB technology.

MMP and the 1998 Mars Surveyor Lander, to be landed on Mars in 1999, both are innovative new technology demonstrators. The MMP aboard the Lander will be separated just prior to Lander's entry into Martian atmosphere. The probe with less than 2 kilograms weight (4.5 lb.) will plunge into the surface of Mars at 200 meters/second (446 mph) to ensure maximum penetration for obtaining soil samples and measurement below the sterilized Martian surface. Nearly all highly integrated electrical and mechanical design will be new to space flight.

MicroBGA Program

MicroBGA program was funded to develop quality and reliability for the assembled technology. MicroBGA program is considered to be a natural extension of the BGA program toward understanding technical issues associated with another miniaturization level that bring about a significant reduction in size and weight. The two technologies have very similar technical issues regarding the development of quality and reliability methodologies. A microBGA consortium is being formed that include the BGA team members and additional new members with expertise in this technology. This consortium will address many challenging issues regarding implementation of this technology. The MicroBGA consortium will concentrate its activities in the following areas and will include other aspects of technology if needs and supports identified by the team members:

- Defining/developing quality assurance methodologies required for low volume, high reliability manufacturing environments. This methodology will also benefit larger production interests since it will support the initial set-up of any manufacturing facility.

- Defining the manufacturing processes, the critical parameters involved with the manufacture of microBGA assemblies and mixed technology including DCA and identifying control parameters.

- Reliability performance of various microBGA package and mixed technology covering DCA used at JPL and those of interest to the consortium team members. The selected parts will have I/O counts centered for near and longer term applications.

- Similarly to BGA program, a design of experiment (DOE) will be used to toggle PWB materials, packages, manufacturing variables, and environmental conditions.

- Inspection techniques will be evaluated and failure analysis on assemblies will be performed and analytical tools will be developed to fully assess assemblies quality and reliability and project life for field applications.

Thermal cycling data generated will be analyzed and categorized using the Weibull distribution, and the Coffin-Manson relationship for the cycles to failure distribution and failure projections. Manufacturing defect and occurrence frequencies for different surface finishes and package types and configurations will be correlated. Modeling techniques will be used to correlate theory with the experiment. Results will be documented and disseminated to team members as well as industry to further help in the development of infrastructure for this technology.

MINIATURIZATION TRENDS IN SMT PACKAGES

SMT - CSP and DCA

In surface mount technology (SMT), electronic packages are mounted and terminated directly onto the printed wiring board (PWB) surface rather than inserting them into plated through-holes (PTHs). Survey results from the Issues in Global Technology survey (Surface Mount Technology Magazine, October 1996 issue) indicate that the percentage of surface-mount chip is expected to increase in 1997 from 47.5 to 49.6 whereas the through-hole is expected to decline from 26.9 to 23.3.

There are several surface mount package styles, both active and passive. Figure 1 shows the different kinds of active surface mount components (SMCs) and the miniaturization trends in each category. Active devices are divided into those with terminations of leads on the periphery of the component, 2 sides or 4 sides, or those with terminations (either pads or solder bumps) over much of the bottom component area. Peripheral Array Packages (PAP) have less potential for significant reduction in size in conjunction with increase in I/O counts compare to Area Array Package (AAP). The BGAs from the latter category are becoming an acceptable alternative.

The CSP version of 2 sides PAP are the Lead-On-Chip (LOC) packages and the most reduced package version for 4 sides are the Slim Tape Chip Carrier. The CSP versions for PAP are micro- (mini-)BGA packages with generally eutectic balls or Land Grid Array (LGA). The CSP packages similar to other packages will resolve incompatibility of IC's pad to assembly/reflow process as well as protection from physical damages and also package is a vehicle for ease of die functionality test.

Another level of miniaturization is accomplished by directly attaching the bare die on the PWB. The direct Flip Chip On Board (FCOB) is the ultimate miniaturization level achieving nearly 70% efficiency of the area of die to the PWB's foot print. In FCOB, solder bumps are permanently attached to the face of bare die, flip over, and mounts on the PWB. In Chip-On-Board, with about 50% area efficiency, the pads of wire bonded die is used to second level wire bonding onto the PWB. In the Tape Carrier version, the second level bonding is accomplished using tapes.

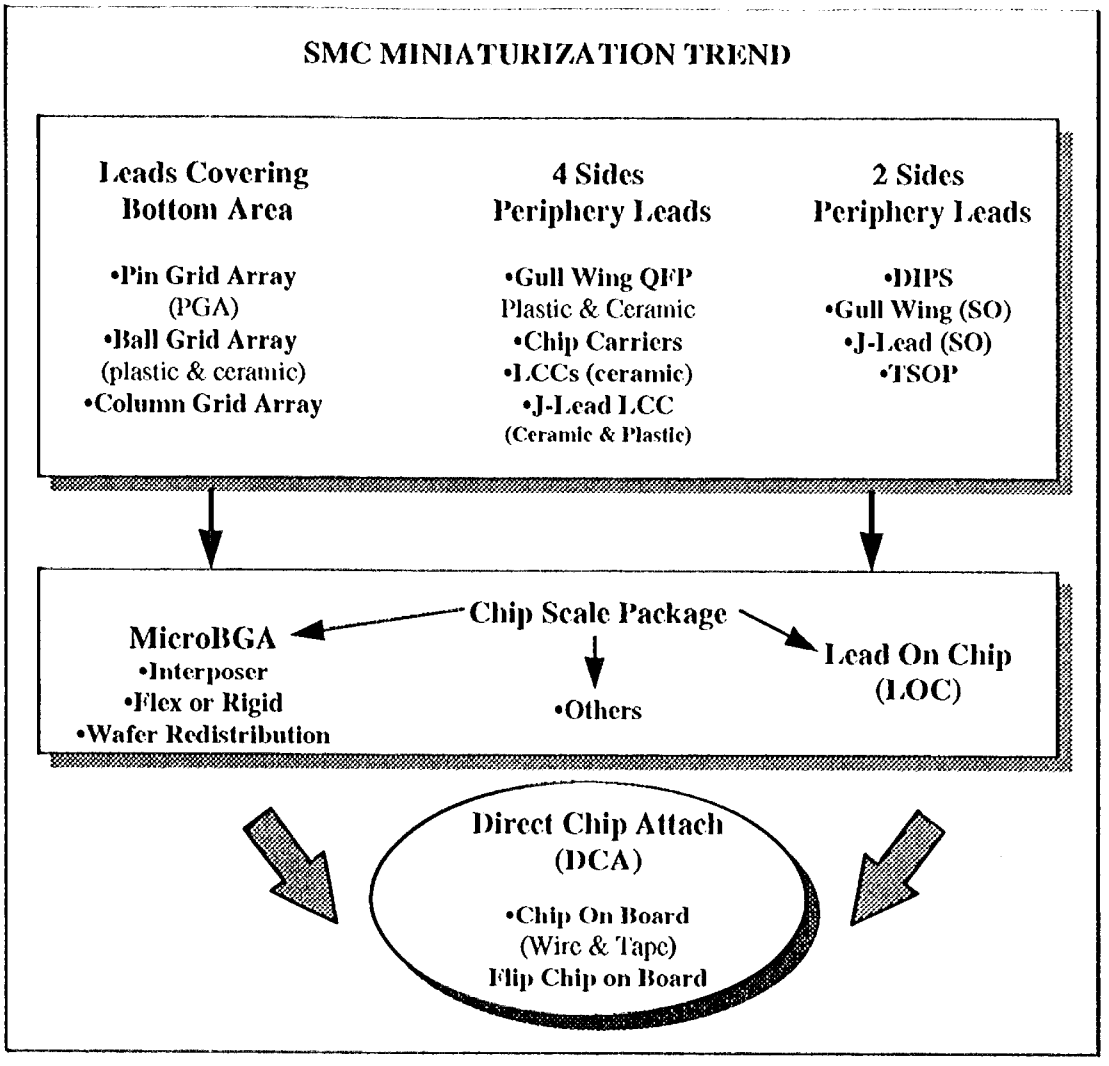


Figure 1. Surface Mount Package Miniaturization Trends

CHIP SCALE PACKAGES

CSPs are packages that are up to 1.2 or 1.5 times larger than the perimeter or the area of the die that it contains, respectively. These packages are seen as vision of future since they provide the benefits of the small size and performance of the bare die or flip chip and the advantage of the standard die packages. The packaging accomplishes many purpose including the following:

- Providing solder ball and leads that are compatible with the PWB pad for reflow assembly processes whereas the aluminum pad of the die is not.
- Redistributing the tight pitch of the die to the pitch level that is within the norm of PWB fabrication. Small sizes of CSPs do not permit significant redistributions and the current

cost effective PWB fabrication limits full adoption of the technology especially for high I/O counts.

- Protecting die from physical and alpha radiation (soft error) damages, and provide a vehicle for thermal dissipation and ease of testability for the die functionality.

CSP Package Types

CSPs generally have been categorized in five different types based on their fundamental structures. These are:

- Interposer packages with either flex or rigid substrate. The flex type employs flex circuit, e.g. Cu/polyimide, structure and rigid type uses rigid substrates, e.g. BT resin. For example Tessera's microBGA package, a flex type, uses TAB-like interconnects (S shape for the maximum thermal mismatch absorption) with an elastomeric layer to translate the die pads to an SMT pitch and footprint. The elastomeric layer decouple the expansion of silicone chip (CTE 2-3 ppm/°C) to that of PWB (CTE for FR-4 ~15 ppm/°C). An example of CSP with rigid substrate is Motorola's Slightly Larger than IC Carrier (SLICC) that employ FR-4 or BT substrate. The C4 (Controlled Collapse Chip Connection) flip chip die on BT substrate is redistributed through solder balls for PWB assembly. The height of the latter packages are within 1-2 mm is higher than former which is in 0.8-1 mm range.

- Wafer level molding and assembly redistribution. The wafer level molded package is processed at the IC level using thin film metallization in the inter-die scribe area prior to wafer singulation. Currently, these very thin packages (0.3 to 0.5) are limited to peripheral I/O formats and they are easily converted to three dimensional stacking version for memory cube. The Sandia miniBGA is an example of wafer assembled CSP where thin film metal/polymer redistributes the location of solder bump over chip compatible with the surface mount footprint. The height of the latter package type increases by the thickness of metal polymer layer from the former package and is between 0.5 to 0.7 mm.

- Lead On Chip (LOC) packages uses lead frame that extends over the top of the die rather than periphery for a standard plastic package.

In comparing the ideal CSP package attributes with those available, only a few types came close to meeting the criteria set (Reference 5). Among these, one key element of significant for space application is "proven reliability for application". Another significant aspect to low volume and highly reliable applications is the development of inspection methodologies that assure integrity of assemblies. Today, most of data generate are generally gathered for packages and there is limited environmental data available for board level interconnection. The board level reliability is further discussed in what follows.

BOARD LEVEL RELIABILITY

Failure at the board level could cause by either the failure of package or the package to board connection. The latter could cause by the intrinsic wear-out mechanism or by hostile environmental factors. The thermo-mechanical wear out (creep) of solder joint is the cause of failure of most of CSP assemblies. Failure in solder joint can cause by mechanical stresses in a non-uniform thermal expansion and contraction of different materials in the assembly. To achieve minimum damage to solder joints, thermal mismatch between the die and board should be minimized through an optimized CSP packaging. Only a few of the CSP packages have been designed to minimize such damages.

DCA package on the other hand are more prone to failure due to corrosion. Encapsulation, underfilling, and passivation polymeric materials are susceptible to outgassing of various constituent, moisture ingression and ionic migration resulting in corrosion failure. To avoid failure, bonding pads must be cleaned from contaminated, control the ionic materials such as Chloride (Cl-) to below 20 ppm, and select materials with minimum outgassing. These are few key reliability issues that need to be understood for implementation of DCA packages.

CSP Assembled Reliability

Table 1 lists the assembled reliability for several CSP packages. Being an emergent technology, there are very limited data published in this area. Currently, most of the data published are those that provided by package manufacturers. Since this technology is rapidly growing in the commercial sector, it is expected that considerable amount of reliability data become available for the current and improved packages. Thermal cycling test for assemlies listed in Table 1 is as follows:

- µBGA Package from Tessera (Flex Interposer)- This package is also manufactured by Shinko and Amkor. Tessera's package consists of a TAB-like IC interconnects, silicone elastomeric interposer, and eutectic solder balls. Thermal cycling data in the Table were for daisy packages on FR-4. Thermal shock tests were performed from the liquid nitrogen temperature (-196°C) to hot oil (160°C) with 5 minute dwell at each extreme temperature. Results for this and those with the extremely low and high temperatures might not be representative of the field failure. For example, it is expected that FR-4 board to show severe damage if thermal cycling temperature exceeds its glass transition temperature. Indeed, it was observed that FR-4 plated through holes had massive barrel cracking failure.
- Fine Pitch BGA (FPBGA) by NEC (Flex Interposer)- This package consists of a carrier tape (Cu/Polyimide), an adhesive (thermoplastic polyimide), and solder bumps (eutectic solder). Assemblies with the underfilling resin survived 200 thermal cycles of -40°C to 125°C.

Table 1. CSPs Assembled Reliability Data

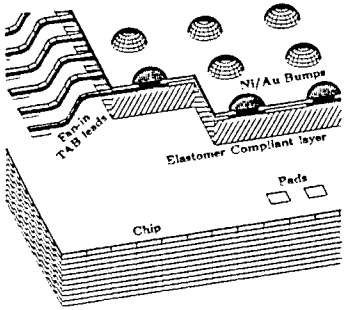
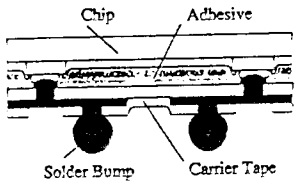
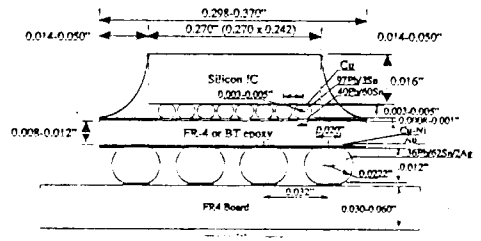
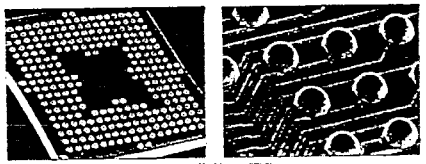
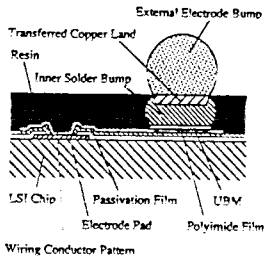
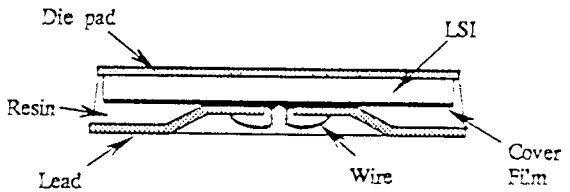
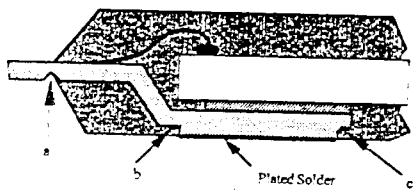
Package Schematic (not to scale)	Package Type	Cycling Condition	Total Cycles	Fails/ Samples	I/O	Ref.
	µBGA (Tessera)	-196°C, 5 min to 160°, 5 min	130 no underfill	0/3	188	6
	µBGA (Tessera)	-55°C to 150°C	100 test interrupted	0/48	188	6
	µBGA (Tessera)	0°C to 100°C	1163	0/46	188	6
	µBGA (Shinko)	-55°C, 5 min to 125°C, 5 min	1500	0/6	172	data sheet
	µBGA (Shinko)	-65°C, 30 min 150°C, 30 min	700	0/6	172	data sheet
	FPBGA (NEC)	-40°C to 125°C	200 undefill	0/20	232	7
	SLICC Motorola	-55°C,10 min to 125°C, 10 mins	320 560 >655 crack initiation by modeling	0/40 10/40 NA	64 64	8 8 9
	JACS (Motorola)	-40°C to 125°C	>1000 no underfill	NA	80	10

Table 1 Continued

Package Schematic (not to scale)	Package Type	Cycling Condition	Total Cycles	Fails/ Samples	I/O	Ref.
	MiniBGA (Sandia)	0°C to 100°C (Thermal Shock)	>2000 underfill <40 no underfill!	NA	266	11
	Mitsubishi	-40°C to 125°C, 1 hour/cycle	500 underfill 200 no underfill 100 bare die	0/3 (0/20) 10/30	96	12
	Jujitsu LOC	-65°C,30 min to 155°C, 30 min	500	0/40	26	13
	LG Semicon LOC (BLP)	-30°C 85°C	>1200	N/A	20	14

- Motorola's SLICC (Rigid Interposer)- This is a chip scale BGA package consists of flip chip IC, FR-4 or BT resin interposer, and 2%Ag eutectic solder balls. Earlier experimental thermal shock test (-55°C to 125°C) results indicated that the package assembly will survive at least 320 cycles. A more recent analytical modeling calculation indicates that solder joints will not initiate crack to 655 cycles. It is my understanding that other experimental data will be available by Motorola. Motorola also is developing a low cost version of this package called Just About the Chip Scale Package (JACS). The recent update results for this package also included in the Table.
- Sandia's miniBGA (Wafer level redistribution)- The recent update results presented is included listed in Table. This package, similarly to C4 assemblies, requires underfilling to achieve some level of assembled reliability.
- Mitsubishi' CSP for high pin (Wafer Level Redistribution)- It consists of copper conductor pattern interconnecting die to external electrode bump through under bump metals. The assembled package with no underfilling survived 200 thermal cycles (-40°C to 125°C) and showed 8 failures out of 20 at 500 thermal cycles. Underfilled assemblies showed no failure to 500 cycles. Cycles to failure for bare die were much lower than those of assembled ones and 10 and 25 samples out of 30 samples were failed at 100 and 200 cycles, respectively.
- Fujitsu and LG Semicon Lead-On-Chip- The former uses Bottom Lead Packages die with face down where the latter uses die with face up.

Assembled Reliability Challenges for Space Applications

Every space mission is unique and the electronic boards are specially designed for the specific missions. Space applications may range from shuttle missions lasting a few days to outer solar systems requiring multi-decade service life. The differences in reliability requirements plays a key role in the selection/design and inspection/testing process. Unlike commercial applications that reliability failure in part per million, the acceptable risk for the success of a space mission is associated with the first failure of electronic parts or interconnection. Even though the highest reliability is demanded, it is extremely difficult, however, to quantify the reliability level requirement and demonstrate its indices. One reason is due to unavailability of solder joint field data and failure statistics. These limits exact definition of reliability assurance requirement. Assurance must depend on qual testing methodologies unique to accelerated environments along with credible analytical prediction.

Until recently, generally a few critical components were tailor-made parts, but majority of components were selected from an available parts list based on military spefications. The current constraint on budget and changes in military specifications along with the applications of bold new technology for space missions, necessitates potential use of advanced commercial electronic packages. This is specially more critical in the miniaturization areas where even the PWB manufacturers are lagging to meet the demand of the rapid advancement in IC and package development. Use of advanced packages including BGAs and CSPs specifically their plastic versions are contingent upon resolution of many specific issues regarding the space applications such as radiation damage. Another key environmental feature of space that need to be considered is the thermal/vacuum environment. The absence of gas convection in a

vacuum environment can drastically change the temperature control and design characteristics of the advance electronic component with high dissipation power.

Since only very small production quantity is involved, the critical manufacturing steps are severely limited. Often, NASA requires a coupon-certification of the manufacturing process for potential candidate manufacturers; however, there are generally not enough test boards to fine tune the fabrication processes to achieve the level of quality obtained in a commercial mass production line. As a results, 100 percent visual inspection often become mandatory to provide another quality assurance step. MicroBGAs similarly to BGAs with hidden solder balls, obsolete the use of visual technique for quality assurance and therefore more advanced techniques are sought. In addition to development of criteria for visual characterization of peripheral solder joints, other techniques including X-ray and Scanning Acoustic Microscopy need to be further developed for assuring the quality of solder joint.

CONCLUSIONS

Board level solder joint reliability information is critical in acceptance of CSPs as alternative package. The very limited data available on cycles to failure of assembled packages are of even less value since data generated under significanty different environmental conditions. For wider applications of this technology, potential user will need the reliability data for its design since generally they have no resources, time, or ability to perform a complex environmental characterizations. JPL is currently coordinating an industry-wide BGA consortium that successfully accomplished building and testing of nearly 400 test vehicles. Similarly to BGA program, a consortium is formed to address many assembled reliability issues. The objectives of microBGA consortium are to address many technical issues regarding the interplay of package type, I/O counts, PWB materials, and manufacturing variables on quality and reliability of assembled packages

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ACKNOWLEDGMENTS

The research described in this publication is being carried out by the Jet Propulsion Laboratory, California Institute of Technology, under a contract with the National Aeronautics and Space Administration.

BIOGRAPHY

Dr. Reza Ghaffarian has nearly 20 years of industrial and academic experience in mechanical, materials, and manufacturing processes engineering. At JPL, he supports research and development activities in SMT, BGA, and CSP technologies for infusion into NASA's missions. He has authored or co-authored over 30 technical papers and numerous patentable innovations. He received his M.S. in 1979, Engineering Degree in 1980, and Ph.D. in 1982 all in engineering from University of California at Los Angeles (UCLA).