See DAA

A Systems Approach for Quality and Reliability of Chip Scale Package Assembly

Reza Ghaffarian, Ph.D.
Jet Propulsion Laboratory
California Institute of Technology
Pasadena, California
818-354-2059
Reza. Ghaffarian@JPL.NASA.Gov

Abstract

This paper reviews many factors that affect interconnect reliability of commercial-off-the-shelf (COSTS) chip scale package (CSP) assemblies. These include: package type, package build, board design, and assembly variables. Methods of accelerated environmental testing were discussed and reasons for unrealistic life projections for CSP assembly reliability by numerous modelers is also examined. Preliminary thermal cycling test results in the range of –30°C to 100°C for test vehicles especially a double sided assembly were also presented. It was concluded that availability of meaningful assembly reliability test results are needed to accelerate implementation of this technology. The JPL-led CSP consortia are addressing many of these issues.

TABLE OF CONTENTS

1. RELIABILITY A SYSTEMS APPROACH

CSP Reliability Challenges

Emerging grid Chip Scale Packages (CSPs), miniature version of ball grid arrays (BGAs) are competing with bare die flip chip assemblies. CSP is an important miniature electronic package technology for utilizing especially low pin counts, without the attendant handling and processing problems of low peripheral leaded packages such as thin small outline packages (TSOPs) and high I/O (input/output) quad flat packages (QFPs). Advantages include self alignment characterization during assembly reflow process and better lead (ball) rigidity. Reliability data and inspection techniques are need for its acceptance especially for high reliability applications.

Reliability, irrespective of its definition, is no longer an "after-the-fact" concept; rather, it must be an integral part of development and implementation. This is specifically true for microelectronics with demands for miniaturization and system integration in a faster, better, and cheaper environment. CSPs rapid development and introduction into the market is a good example of this trend.

The use of new materials, processes, and new applications obscure the traditional definition of quality and reliability assurance. New systems approaches are needed to assure quality and reliability as well as to manage risks. Quality should be assured by design for reliability, controls for processes, tailored testing methods for qualification, and use of unique accelerated environmental testing along with credible analytical prediction. In other words, an efficient concurrent engineering system approach must be implemented.

Environmental Testing

Among the many environmental accelerated testing methodologies for assessing reliability of electronic systems, thermal cycling is the most commonly used for characterization of devices as well as interconnections. Among the many predefined thermal cycling profiles, the military and commercial aspects represent the two extremes. Previously, NASA also had a preset specific thermal cycling requirement. Although the Military Standard (Mil-STD-883) recently was obsoleted, it is still used for benchmark testing. Within Mil-STD-883, there are three levels of accelerated cycling temperatures:

- Condition A, -55°/85°C
- Condition B, -55°/125°C
- Condition C, -65°/150°C

For benchmark conditions, devices are generally subjected to condition C and assemblies most often to condition B. The assemblies were traditionally considered qualified when they last 1,000 cycles. A commercial cycling profile, the J-12 IPC specification, recommends a thermal cycle in

the range of 0°C to 100°C. Within a temperature range, the dwell, heat and cool down rates are critical parameters and also affect cycles to failure.

The NASA thermal cycling requirements are stringent and are specified in various revisions of NASA Handbooks. For example, in a previous revision, NHB 5300.4 (3A-1), there was a well defined requirement for number of cycles and solder condition after exposure. No cracking of any solder joint was allowed after 200 NASA cycles (-55°C to 100°C with 245 minutes duration).

Performance-based Assurance Requirement

In a subsequent NHB revision, the requirements were based on meeting the specific mission condition. The build and test methodology is expected to yield confidence in reliability to satisfy the mission conditions. Mission requirements are emphasized rather than a universal cycle and a value for all missions.

Test to "establish the confidence in reliability" adopted by NASA a long-time ago is now "the reliability theme" for the commercial sector. Discussions on "Breaking Traditional Paradigms" and "Rethinking of Environmental Reliability Testing" by authors from the commercial sector are becoming hot topics with the introduction of new miniaturized CSPs. These packages have their own unique form factor not seen in SMT. Unable to meet the stringent requirements established by the previous military standards, a new "paradigm shift" is considered to be the solution. The "shift" is further motivated by several factors including the following:

- Reduction in life expectancy for consumer electronics
- Rapid changes in electronic technology
- Obsolescence of many military specifications

Additional unique tests are now adopted to meet the specific consumer electronic products. For portable electronics, bend test, drop test, and possible "washing machine test" are suggested. The IPC 9701 specification, Qualification and Performance Test Methods for Surface Mount Solder Attachments, is aimed to include some of these requirements. It must be recognized that no accelerated tests can be truly universal. Field reliability is the ultimate test, and either substantiates or invalidates the experimental tests.

For space missions, gathering information on the root cause field failure is almost impossible. For commercial applications, rapid changes in technology render field information almost useless for new product development. The only solution is to understand key reliability parameters and to design for reliability. Subsequent process controls, as well as efficient qualification and inspection, also help assure sufficient field reliability. In other words, risk control and risk management must be practical.

2- CSP Variables Assembly Reliability

There are many factors that affect CSP reliability. These include design, package build, solder paste, assembly, underfill, and type of test for reliability evaluation. In the following a few of these variables are discussed.

Design

PWB pad design— For BGAs, discussions on use of solder mask defined vs. non-solder mask (SMD vs. NSMD) were hot subjects for a short period. There were two camps, one showing the improvement due to use of SMD– reasoning that masks over copper are needed for improved pad adhesion strength as well as the potential benefit of cycles to failure increased due to increase solder joint height. The other camp showed that crack initiation in solder, due to overlaying of the mask, could reduce the number of cycles to failure. NSMD is now commonly recommended.

The pad size design relative to package has its own supporters. As a rule of thumb, the board pad size should be the same as the package. A slight unbalance in this relationship could result in failure at the board or package. Optimized conditions might differ for different packages depending on many factors including the ball attachment configuration, ball size, pitch, and I/O.

Package Variables

Die bond on interposer— There are various techniques that are used to transfer the die I/O to the interposer within the package. Each element of the package internal form has its own effect. For TAB CSP (Tape Automated Bonding), the TAB is the weakest link. For flip chip die in Jacs-Pak, the failure was observed on the C5 (board level) solder joint interconnection, when subjected to thermal cycling. This might not be the general case for the flip chip die. CSPs and BGAs with flip chip dies are more susceptible to internal package failure than their wire bond versions.

Interposer thickness— When the interposer was increased from 0.4 mm thickness to 0.6 mm, cycles to failure increased from 400 to about 800 cycles (-25/125°C). Data for Jacs-Pak™, indicates that semi-rigid interposer would have 1.88 times the number of thermal cycles. Is the rigidity equivalent to thickness change or possibly because of materials change? The answer is not known. Interposer CTE also has significant affect on the board reliability.

Interposer materials— CSPs with different interposer materials showed significantly different cycles to failure– about a three times increase (Sony, IMAPS '97). In an experiment, it was found that a factor of about three times will be achieved when a low CTE interposer was used (1200 vs. 400 cycles, -25/125°C).

Die size— In one study it was shown (Amkor, ECTC '98) that when die size increased from 6.4 mm to 9.5 mm, the first cycles to failure decreased from 1500 to 900 cycles in the range of -40°C to 125°C.

Solder Ball

Solder composition— Eutectic solder (63/37) is the most commonly used solder due to it having many desirable attributes, including low temperature melting. To improve fatigue characteristics, small amounts of silver (2%) have been added to this composition. Additive materials have the potential of formation of brittle intermetallic phases as well as softening by precipitation formation. These metallurgical transitions are further accelerated by increases in temperature. Effect of five element alloy was shown to improve thermal cycling reliability by 1.2 to 1.5 times (TI, SMI '97).

Ball shape attachment— For BGAs, it has been demonstrated that the DBGAs (Dimple BGA) improve reliability. This might be the case for CSPs too, but its significance is yet to be demonstrated.

3-CSP Assembly Variables on Reliability

Assembly Variables

Solder joint height— The effect of solder joint height on reliability has been widely discussed for BGAs. One reason for the use of an SMD pad for PBGAs, with collapsible solder, was to increase solder ball height and hence increase reliability. Height was also increased by use of columns in the ceramic column grid arrays to achieve significant reliability improvements compared to the ball grid array version. Improvement was shown for CSPs when ball heights are increased (Sony, IMAPS '97). When solder height is doubled, cycles to failure for the board tripled.

Underfill— One key advantage of CSPs over flip chips is that ideally there is no requirement for CSPs to be underfilled. The assemblers for consumer products prefer packages with no underfill one process step is eliminated and reworkability is permitted. However, for high reliability applications where vibration and shock are key in ruggedness, use of underfill might be the only solution now known to meet the harsh requirements.

For flip chips with very short cycles to failure, it has been shown that underfill will improve cycles to failure reliability an order of magnitude (5-10 at least). This is very similar to the results shown in Table 2 for the wafer level miniBGA packages with and without underfill.

Double Reflow— There are many concerns when double sided boards are assembled. Reliability reduction is one. For heavy BGAs, one concern was potential part fall from the assembled side during the second reflow. Similar concerns might be true for CSPs with the small solder volume; not enough tension force to hold even the small size of CSPs.

In addition, it has been shown that for double sided assemblies, cycles to failures were about half of the single sided assemblies (Sony, IMAPS '97). Recently, similar test results were presented for another CSP package (Sharp, ECTC '98). Double sided assemblies with packages on directly opposite sides of the board showed lower cycles to failure. This was improved with partial relative package offsets on the two sides.

Test results published recently on double-sided mirror-imaged BGA [5] assemblies indicate improvement on cycles to failure for double reflowed solder joints. Improvement were observed for both plastic and ceramic BGAs. Increase in stand-off height for plastic package and increase in solder volume for CBGAs were given as possible reasons. The optimum weight per solder joint to produce a uniform cylindrical fillet was found to be 0.04 gr. Since no comparison was made between the single and double sided assemblies, it is not known if the trend for BGAs is the same as CSPs.

Failure Mechanisms and CSP Reliability

For conventional surface mount assemblies, solder joint interconnects were considered to be the main cause of assembly failure. For CSPs, failure at the board level could also be caused by the internal failure of the package. For example, package internal TAB lead failures at heels were reported for the CTE absorbed CSP— a fatigue failure shift from the solder joint to the internal package (see Figure 1).

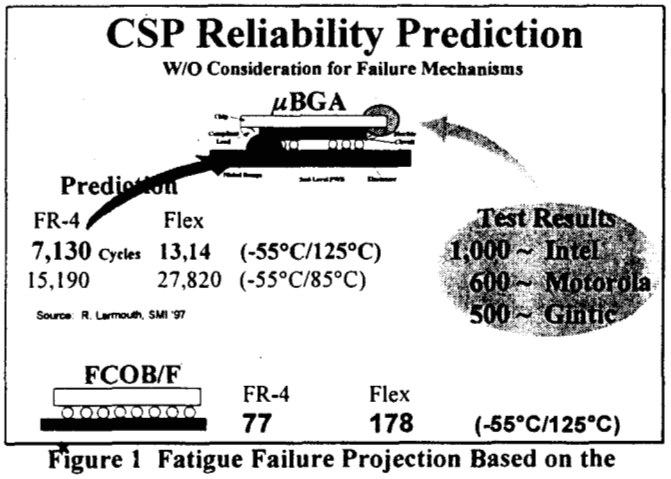

Figure 1 Fatigue Failure Projection Based on the Wrong Failure Mechanism Assumption

This new type of failure is in contrast to the traditional theoretical wisdom where the solder joint failure is generally considered to be the weak link in solder joint assemblies.

This and other failure mechanisms, which are being established for CSPs, must be understood by a modeler before he/she is to predict a meaningful reliability projection.

Table 1 includes four projections from different modelers and experiment test results. It is interesting to compare the theoretical values with those experiment test results for numerous CSPs. It becomes obvious that these calculation are at least 5 to 20 times higher than the test results. As noted earlier, the highest value test results are in the range of 500 to 1,000 cycles. Projections of more than 20,000 cycles to failure in the range of -55 to 125°C is unrealistic.

Unrealistic results could also occur when DNP is used as indicator for cycles to failure. In the IPC report J-STD-012 (Joint Industry Standard Implementation of Flip Chip and Chip Scale Technology), assembly reliability projections were based on flip chip die being attached to the board. DNPs were used for calculation of the first failure and projection of failure with size of package. This is not valid for most CSPs, except possibly for a few wafer level CSPs without underfill. Although there is a relationship between an increase in die size and reliability, the relationship is not linear and depends on many parameters. For example, fan-out packages with small die will not follow the DNP indications.

Table 1 Misleading CSP Cycles to Failure Projections by Modeling

Package Type	I/O	Cycle Profile	Cycles to Failure Projection	Test Results
TAB CSP	46	-55/125°C	7,000	500-1,000
WAFER CSP	96	-40/125°C	3,200	200-500 8 failures
FLIP CHIP CSP	N/A	-55/125°C	20,000	N/A
LOW COST CSP	N/A	-40/125°C	21,000	N/A

4- Preliminary Assembly Test Results

Many aspects of CSP technology, with focus on assembly reliability characteristics, are being investigated by the JPL-led consortia. Three types of test vehicles were considered for evaluation and currently two configurations have been built to optimize attachment processes and define the effects of package, board, and assembly processes. Nearly 200 test vehicles are being assembled and will be subject to thermal and mechanical evaluation.

CSP Manufacturing Robustness

Initially, seven trial #1 test vehicles and thirty #2 test vehicles were assembled for process optimization and preliminary environmental characterization. Grid CSPs are known to be robust in manufacturing, but there is disagreement on the acceptable manufacturing offsets. No defects were observed when thirty #2 test vehicles, each with 4 grid CSPs with 46 I/Os, were assembled.

Quality of Solder Joints

Figure 2 shows a SEM photomicrograph of a solder joint for a TAB CSP and a low I/O wafer level (8 I/O) package on a board. Low package height make inspection of the joints very difficult, either by visual or by SEM. Three of these wafer packages showed poor quality solder joints with signs of cracking. Poor quality of the package was the reason for existence of microcracks after assembly. For these reasons, this package excluded for the #1 test vehicle assembly.

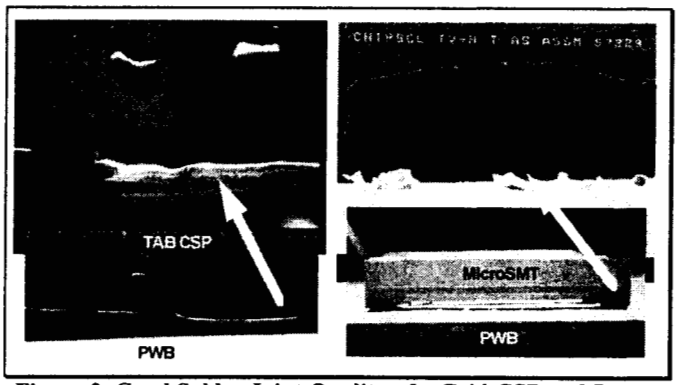

Figure 2 Good Solder Joint Quality of a Grid CSP and Poor Solder Joint Quality of Low I/O Wafer Level

Grid CSP Assembly Shear Forces

A trial test assembly #2 was subjected to shear testing to determine the solder joint shear strength. Low I/O wafer level assemblies could be sheared by the shear tester, but not the assembled TAB CSP. Therefore, four of these were subjected to pull testing to failure. The test results are as follows:

- The low I/O wafer level packages failed at 312, 249, 175, and 158 grams. These values are low and this is a serious concern. Die penetrant indicated the existence of cracks prior to shear.
- TAB CSP-1 assemblies were detached by pulling from the package. No solder joint failures were observed, but failure were observed at the ball interface traces in the package. The tensile forces for four of these were 28, 25, 22, and 13 Kg. The 13 to 28 kg for a package of 46 I/Os is equivalent to 280 to 600 g/ball. Ball shear forces for the same package were in the range of 320 to 400 g [6].

5- THERMAL CYCLING TEST RESULTS

Seven trial #1 test vehicles were assembled to optimize the assembly process and profile. The lowest stencil thickness, 4 mil, was used to determine the worst condition, that is, solder starving condition on a leadless package. A stencil thickness of 6 mil is the recommended thickness for assembly of leadless packages. One test vehicle was assembled double sided. Five of the PWBs had OSP surface finish, and two had HASL. All PWBs including the PWBs with HASL finish, were successfully assembled. As expected, working with HASL was much more difficult than OSP.

The five trial test vehicles with the OSP finish were subjected to thermal cycling in the range of -30 to 100°C (A condition). Both PWB and assembly conditions were not optimum for the trial test. Therefore, thermal cycling results may well suggest potential areas where the process can be optimized for the production test vehicle assemblies. Results are not valid for reliability and failure statistic analyses because of low number of test samples and no-optimum condition.

Resistances were measured manually before and at different thermal cycling intervals to check for electrical opens (solder joint failure). Automatic monitoring was impossible since connections to the ground plane were missed during file translation. This has been corrected and for full production assemblies, these daisy chains will be monitored continuously.

Table 2 shows resistances before and at different thermal cycles. Assemblies were periodically removed from the chamber and checked at room temperature for resistance (Ω). Resistance are different for different daisy chain patterns, but are approximately the same for the same package on various test vehicle assemblies. It is interesting to note that even for non-optimum conditions, the majority of solder joint assemblies survived to 500 cycles. These packages included four low I/O CSPs, leadless and grid CSPs, one high I/O CSP, and a TSOP. The high I/O CSP was underfilled.

Table 2 Daisy Chain Resistances of Assembled CSPs at Various Number of Cycles at Condition A (-30/100°C)

PWB ID	Package ID-Daisy	Cycles 0	Cycles 100	Cycles 300	Cycles 400	Cycles 500	Cycles 600	Cycles 700	Cycles 900	Cycles 1000
22-1A	28 I/O	2.8	2.8	*Open*	*Open*	*Open*	*Open*	*Open*	*Open*	*Open*
22-1A	2	4.6	4.7	5.4	4.8	4.8	4.8	4.9	4.9	4.7
22-1A	3	9.3	9.2	9.5	9.3	9.4	9.5	9.6	9.4	9.5
22-1A	4	6.8	6.6	7	6.8	6.8	6.6	6.8	6.9	6.6
22-1A	5	5.8	5.7	6	6.2	5.7	5.9	5.8	5.9	5.7
22-1A	6-1	20.9	20.7	21.2	21.1	21.2	21.1	21.2	21.1	20.6
22-1A	6-2	23.7	23.5	23.8	23.7	23.6	23.7	23.8	23.9	23.4
22-1	28 I/O	2.3	2.3	2.6	2.7	2.6	2.4	*Open*	*Open*	*Open*
22-1	2	4	4.1	4.1	4.3	4.2	4.1	4.2	4.2	4
22-1	3	9.3	9.3	9.4	9.4	9.2	9.2	9.6	9.6	9.5
22-1	4	5.9	6.3	5.9	6.2	5.8	5.8	6.2	6	6.1
22-1	5	6.1	6.2	6.9	6.6	6.9	6.3	6.6	7.1	45.8

The test vehicle with identification 21-1 and 21-A was the board with the double sided packages. The microvia side (21-A) was reflowed first, and the standard side (21-1) was reflowed next. Therefore, the microvia joints were exposed to two reflows, but the joints on standard side reflowed only once. One failure of a leadless package was observed between 100 and 300 cycles (21-A, daisy chain 1) on the microvia side. This package was also the only package which exactly overlapped (mirror-image) the package on the double side assembly. Other packages had different overlap conditions due to 90 degree pattern rotation.

Figure 3 shows an X-ray of solder joint failures. The first failure location was at a two cross-over corner in double sided package assemblies. The criticality of solder disturbance at the crossing corners will be verified in the full production test vehicle build. Early joint failure is qualitatively in agreement with other investigators' findings. The number of cycles-to-failure was reduced to almost half for double sided assemblies with the mirrored package assemblies. The number of cycles-to-failure was increased as double sided package assemblies moved away from the mirror position.

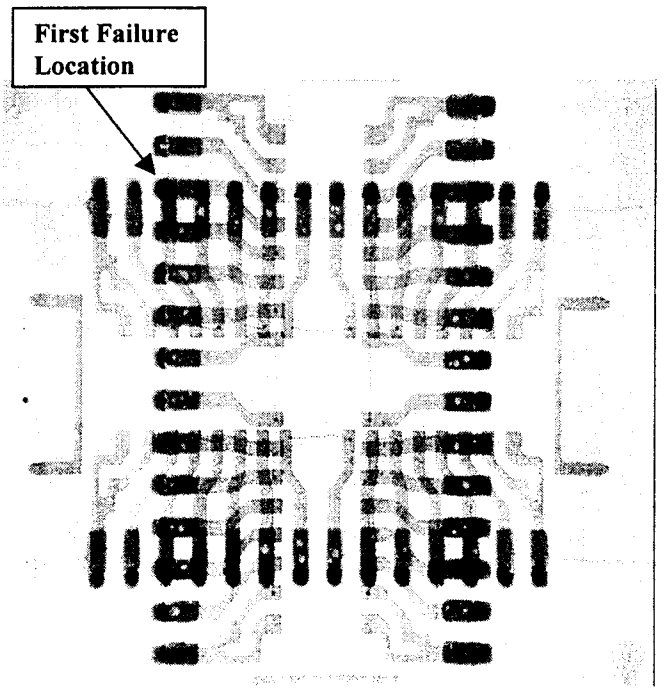

Figure 3 The Solder Joint First Failure in a Double Sided Assembly

Recall that these test vehicles were from the trial run, the chief purpose of which was to understand the critical issues with of PWB fabrication, process optimization, and daisy chain verification.

6- CONCLUSIONS

- A failure shift from solder joint to package may occur more often for miniaturized CSP packages. Projection based on the wrong failure mode result in the wrong forecast of cycles to failure.
- A 28 I/O leadless CSP in mirror-imaged double-sided (DSMI) assembly, reflowed twice, showed about half of cycles to failure the one with a single reflow. This is in qualitative agreement with the test results for other CSP double sided assemblies. This however, contradict a recent test results published for BGA DSMI. Further investigation is underway by JPL-led consortia to address this and many other issues.
- Understanding the overall philosophy of testing to meet system requirements as well as detecting new failure mechanisms associated with miniaturized CSPs is key to collecting meaningful test results. Availability of meaningful test results for CSPs will accelerate their use in bold technology validation space missions, and further qualification and testing will permit their use for scientific exploration missions.

7- REFERENCES

[1] SMI '97, *Proceedings of Chip Scale Packaging Symposium, SMI*, Sept. 7-11, 1997

[2] IMAPS '97, *Proceedings of International Symposium on Microelectronics*, Philadelphia, October 14-16, 1997

[3] CSI '98, *Proceedings of Chip Scale International*, San Jose, May 6-7, 1998

[4] ECTC '98, *Proceedings of 48th Electronic Components & Technology Conference*, Seattle, May 25-28, 1998

[5] Abtew, M, "Double-Sided Mirror-Imaged BGA Assemblies," Circuits Assembly, September 1998, pp. 66-71

[6] Ghaffarian, R, "Joint Integrity of Chip-Scale Packages Under Isothermal Aging,", Chip Scale Review, July 1998, pp. 74-78

8- ACKNOWLEDGMENTS

The research described in this publication is being carried out by the Jet Propulsion Laboratory, California Institute of Technology, under a contract with the National Aeronautics and Space Administration.

I would like to acknowledge the in-kind contributions and cooperative efforts of MicrotypeBGA consortium team members and those who had been or are being contributors to the progress of the program.

9- BIOGRAPHY

Dr. Reza Ghaffarian has nearly 20 years of industrial and academic experience in mechanical, materials, and manufacturing process engineering. At JPL, Quality Assurance Office, he supports research and development activities in SMT, BGA, and CSP technologies for infusion into NASA's missions. He has authored over 50 technical papers and numerous patentable innovations. He received his M.S. in 1979, Engineering Degree in 1980, and Ph.D. in 1982 in engineering from University of California at Los Angeles (UCLA).