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CHIP SCALE PACKAGE AND ASSEMBLY JOINT RELIABILITY

by
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Abstract

The popularity of emerging miniaturized Chip Scale Packages (CSPs) is rapidly growing because of their benefits and smaller size. There are more than fifty CSPs available from different sources with only limited applications. Wider implementation will be facilitated as the necessary infrastructure is developed.

Many aspects of this technology, with focus on assembly reliability characteristics, are being investigated by the JPL-led consortia. Three types of test vehicles were considered for evaluation and currently two configurations have been built to optimize attachment processes. These test vehicles use numerous package types. Nearly 200 test vehicles were assembled and subject to thermal and mechanical evaluation.

In addition, to understand potential failure mechanisms of assemblies, the grid type CSPs were also subjected to environmental exposure. Prior to exposure, they were subjected to visual inspection and scanning electron microscopy (SEM) to characterize their joint quality, solder ball metallurgy, and elemental compositions. These were then subjected to ball shear testing, with results compared to the plastic ball grid arrays. After initial testing, CSPs along with BGAs were subjected to isothermal aging at two different temperatures for two intervals. The exposed packages were then subjected to inspection, SEM, and shear testing, and the levels of damages documented. This paper presents the isothermal aging characteristics of CSPs as well their assembly reliability for the trial test vehicles.

Introduction

The thermo-mechanical wear (creep) of solder joints is the cause of failure for most CSP board assemblies. Failure at the board level can also be due to package internal failure or from the solder balls/package interface in grid CSPs.

A non-uniform thermal expansion and/or contraction of different materials in the assembly induces mechanical stress on solder joints. To achieve the least damage to solder joints, thermal mismatch between the die and board should be minimized either by package optimization or use of board materials that closely match coefficient of thermal expansion (CTE) of the package.

Only a few CSP packages have been designed to alleviate damage due to the thermal expansion of package/board mismatches. The floating pad technology (FPT) is another technique that was

recently conceived with the aim of absorbing CTE mismatches at the pad level (Wojnarowski, ITAP '98). The literature data on assembly reliability of a CTE absorbed package along with numerous other packages were presented (to be published in Chip Scale Review magazine, Nov. '98).

Failure Shift From Solder Joint to Internal Package

Assembly failure can be misinterpreted when there is a shift in failure mechanisms. For example, package internal TAB lead failures at heels were reported for the CTE absorbed CSP— a fatigue failure mechanism shift from the solder joint to the internal package. An example of cycles to failure theoretical projection with no consideration on failure shift is shown in Figure 1. A life of more than 7,000 cycles for a thermal cycle profile of -55°C to 125°C was projected. This is an order of magnitude larger than experimental cycles to failure of 1,000 to 1,500 cycles. The TAB failure just before assembly failure was detected at 1,000 cycles (Greathouse, CHIPCON '96)

Figure 1 also includes the most recent results from a user and evaluation by an independent investigator (Gintic, Singapore). Cycles to failure are much lower than those presented by the supplier of this package (Shinko and Tesserà). Data from Intel presented in late 1997 also show higher number of cycles to failure for this package assembly than those from Motorola presented in May 1998 (ECTC '98) and Gintic presented in November 1998 (IMAPS '98). About 1,000 cycles for former versus approximately 500 cycles for the recent tests. It is possible that the Intel data generated from a more controlled batch of package whereas the latter two might have packages from less controlled environment or different package supplier licensees. Metallurgical condition of the copper TAB has also considered to be the cause of lower failure cycles. Irrespective of reasons behind such early failures, this poses a serious concern from a user point of view especially those with low volume applications.

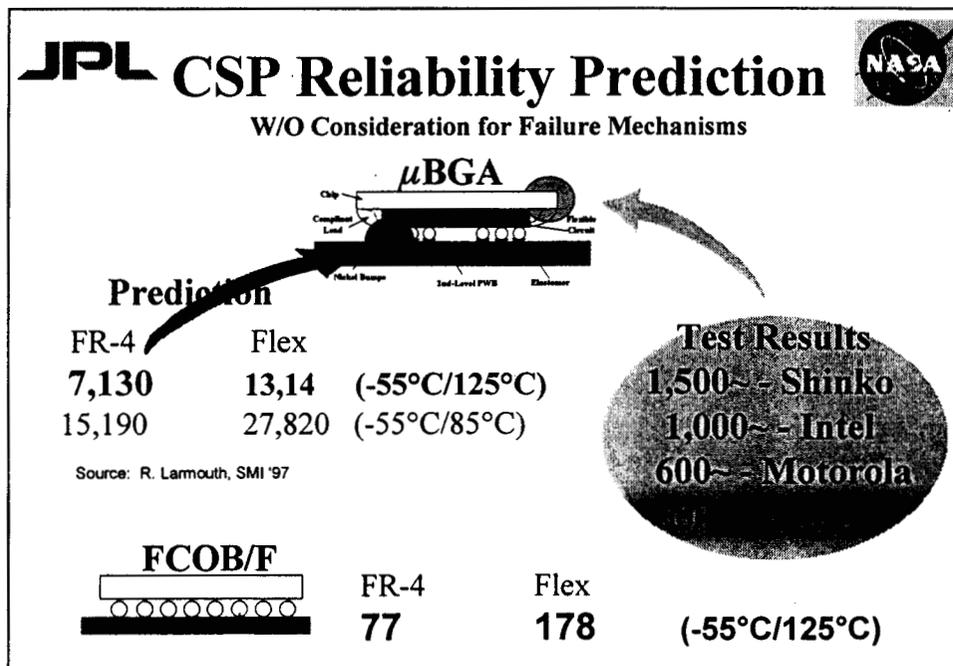


Figure 1 Fatigue Failure Projection Based on the Wrong Failure Mechanism Assumption for a CTE Absorbed CSP

Ball/Package Interface Failure

For grid CSPs, the interface between package and solder balls is another potential failure site. This failure type was observed for plastic BGAs after thermal cycling. For BGAs, cycles to failure and failure mechanisms under different environments were investigation under another program. Figure 2, adapted from Reference 1, shows cumulative failure percentages versus increasing cycles for several plastic BGA assemblies. Wider distribution for two peripheral BGA packages are evidenced from this figure.

The exact causes of wider distributions are yet to be identified. Possible causes include: PWB materials (FR-4, polyimide), solder volume, and ball/package integrity. Package/ball integrity plays a role since failure analyses of cycled BGA assemblies indicated that failures occurred either at package or board interfaces. This means that solder joint cycling test results for packages from prototype or early production might not be representative of full production results. Wider distributions are also expected if processes are not optimized.

This investigation included BGAs as well as grid CSPs to determine if there were differences in package/ball interface integrity before and after isothermal exposure and if this correlated with cycles to failure test results. The isothermal temperatures were the maximum thermal cycling temperatures. The grid CSPs were from the list of leaded, leadless, and CSPs. Their board assemblies are being evaluated by the JPL-led MicrotypeBGA consortium.

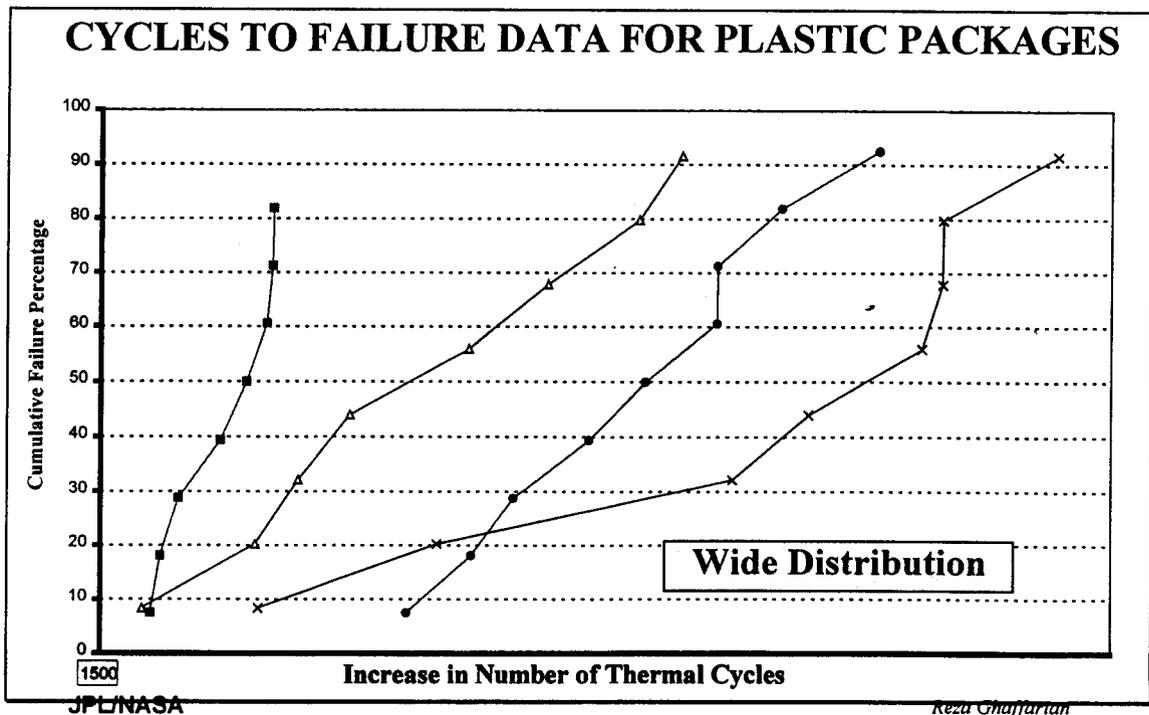
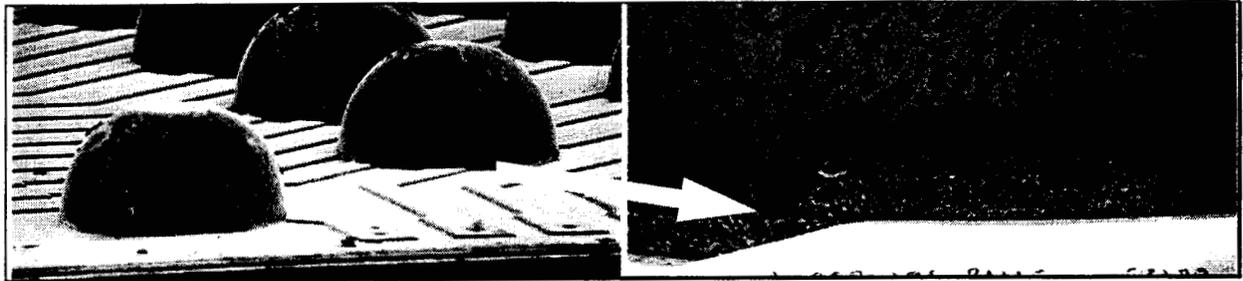


Figure 2 Wide Distribution for Two BGA Package Types

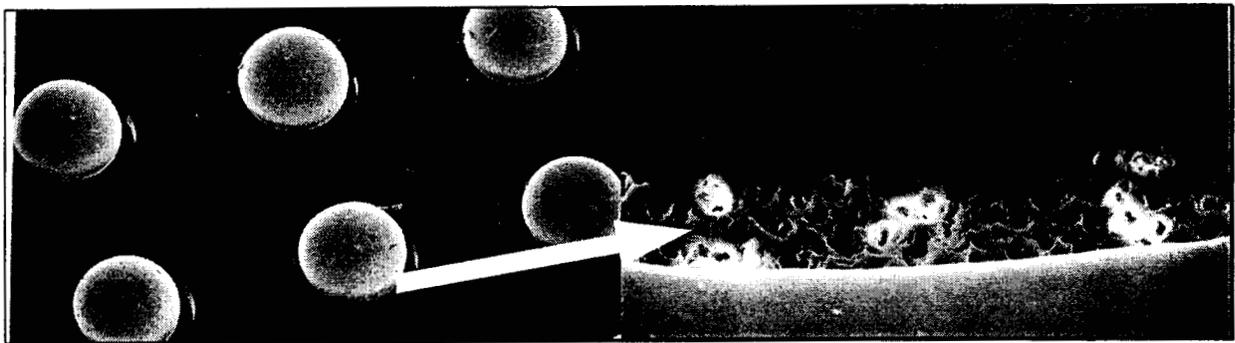
Package Characterization

SEM Characterization

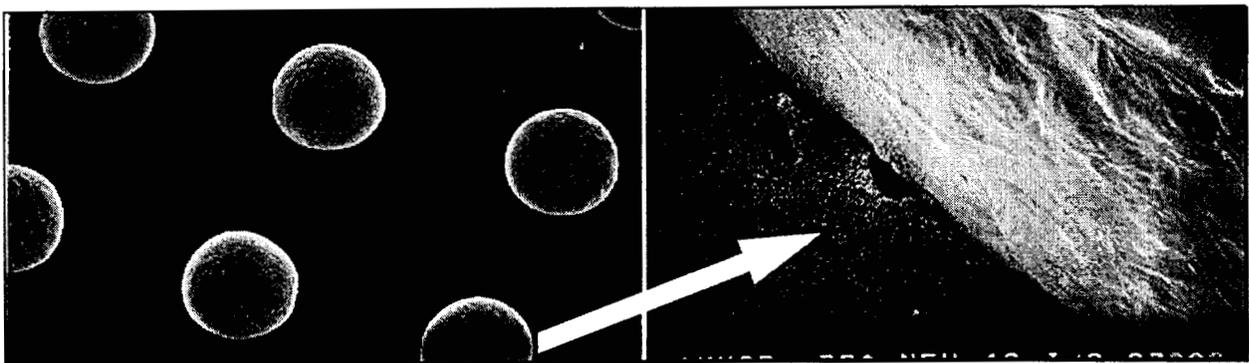
Representative SEM photomicrographs of CSP ball shapes and their interfaces are shown in Figure 3. Photos for a TAB CSP from two suppliers are shown in a and b, and for a wafer version in c. Note differences in interfaces for the same package, but from two suppliers as well as different package categories. The TAB CSP-1 had a non solder mask defined configuration whereas the CSP-2 had a solder mask defined appearance. These differences might not be significant for this specific package since this CSP is a CTE absorbed package and assembled failure is not expected to be from the solder joint.



(a) Wafer Level CSP



(b) TAB CSP-1



(c) TAB CSP-2

Figure 3 Ball/Package Configurations for Various CSPs

Shear Forces Before Isothermal Exposure

Figure 4 shows cumulative percentage versus shear forces for various packages. The median ranking ($i-0.3/n+0.4$) was used to calculate cumulative percentages. The fifty percentile shear forces as well as their respective shear stresses are shown in Table 1. It is interesting to note the significant difference in shear forces for different packages. Distributions for the same packages, but different suppliers are different.

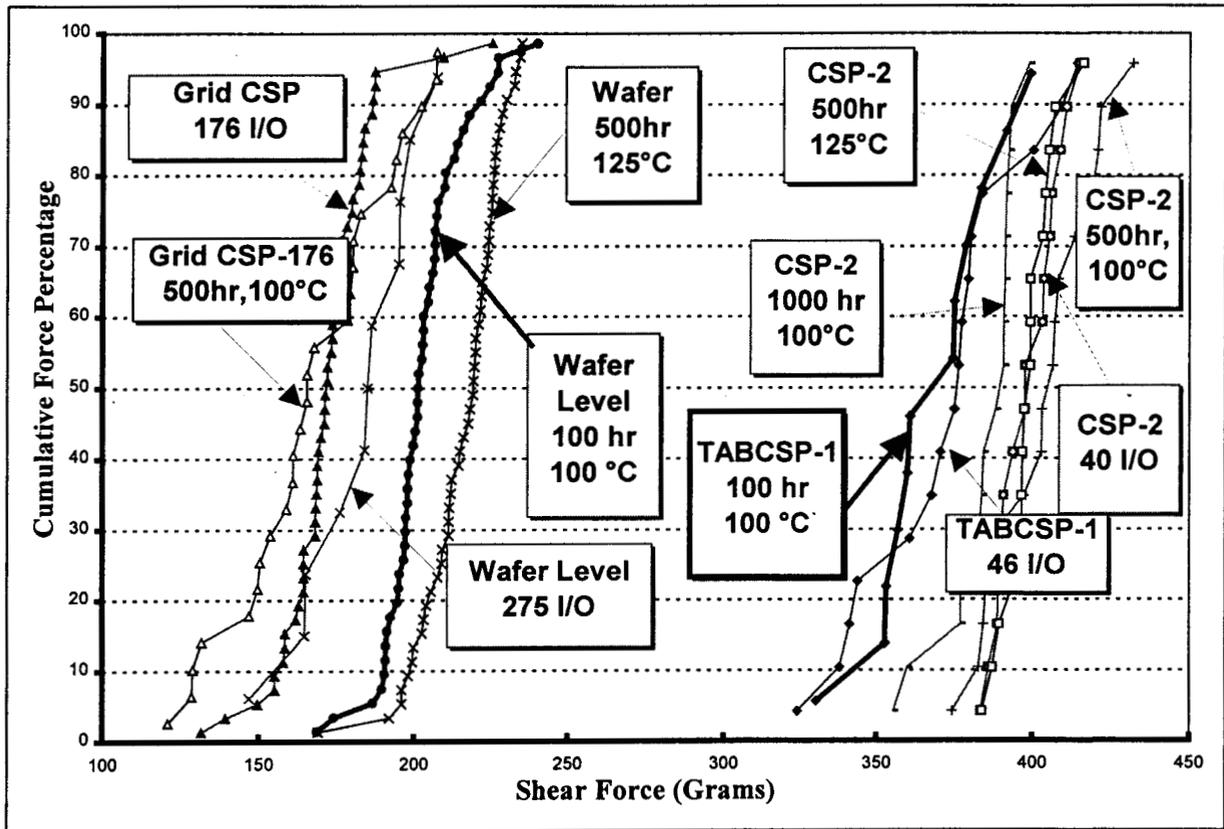


Figure 4 Cumulative Percentage Versus Shear Force in Gram for Various Grid CSPs

Table 1 Shear Force and Stress for Various CSPs

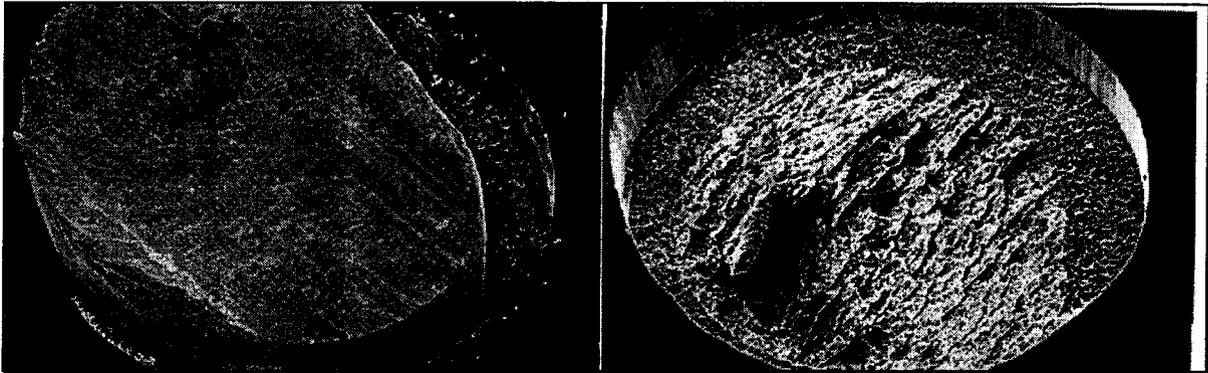
Package Type	I/O	Shear Diameter (mm)	Shear Force (g) at 50%	Shear Stress (Kg/mm ²)	Shear Force 1000 Hr at 100°C
TAB CSP-1	46	0.320	376	4.7	405
TAB CSP-2	40	0.30	397	5.7	390
Wafer Level	275	0.250	185	3.8	221
Grid CSP (Wire Bond on Flex-2)	176	0.170	172	7.6	N/A

SEM of Shear Failures

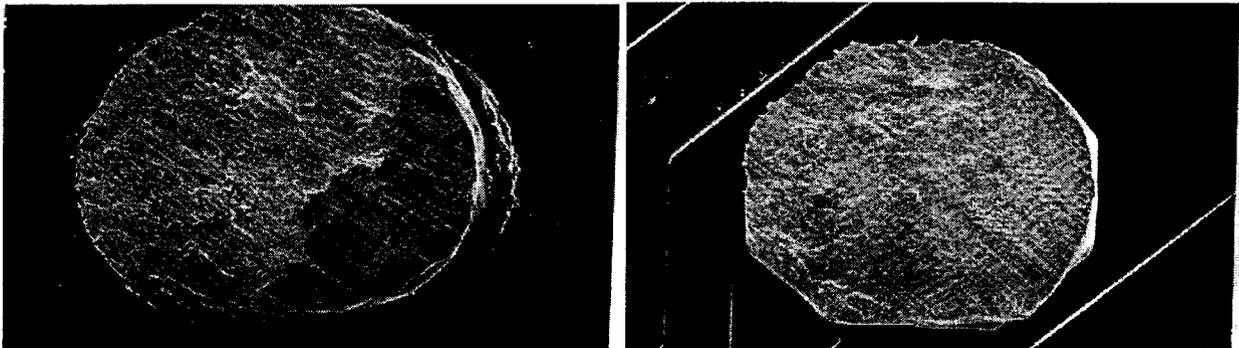
SEM photomicrographs for three CSPs are shown in Figure 5. Generally failures were ductile and were from the balls to package pad interfaces. Two of the balls from the CSP-1 failed in the traces (see right photo of (a)). The non-uniformity in interface failures for CSP-1 might be the reason for this package's wider force distribution plots in Figure 4.

Shear Forces after Isothermal Exposure

Results for those exposed to 1000 hours at 100°C are also shown in Table 1. The wafer level package showed improvement after exposure. The most probable cause of this improvement is microstructural changes which could have reduced the processing residual stresses. This was not verified.



(a) SEM Photomicrographs of Failure Surface after Shear Test for TABCSP-1



(b) SEM Photos Failure Surface after Shear Test for TABCSP-2 (left) and Wafer level

Figure 5 SEM Photos of Failure Surface after Shear Tests for Various CSPs

Thermal Cycling Test Results

Seven trial #1 test vehicles were assembled to optimize the assembly process and profile. The lowest stencil thickness, 4 mil, was used to determine the worst condition, that is, solder starving condition on a leadless package. A stencil thickness of 6 mil is the recommended thickness for assembly of leadless packages. One test vehicle was assembled double sided. Five of the PWBs had OSP surface finish, and two had HASL. All PWBs including the PWBs with HASL finish, were successfully assembled. As expected, working with HASL was much more difficult than OSP.

The five trial test vehicles with the OSP finish were subjected to thermal cycling in the range of -30 to 100°C (A condition). Both PWB and assembly conditions were not optimum for the trial test. Therefore, thermal cycling results may well suggest potential areas where the process can be optimized for the production test vehicle assemblies. Results are not valid for reliability and failure statistic analyses because of low number of test samples and no-optimum condition.

Resistances were measured manually before and at different thermal cycling intervals to check for electrical opens (solder joint failure). Automatic monitoring was impossible since connections to the ground plane were missed during file translation. This has been corrected and for full production assemblies, these daisy chains will be monitored continuously.

Table 2 shows resistances before and at different thermal cycles. Assemblies were periodically removed from the chamber and checked at room temperature for resistance (Ω). Resistance are different for different daisy chain patterns, but are approximately the same for the same package on various test vehicle assemblies. It is interesting to note that even for non-optimum conditions, the majority of solder joint assemblies survived to 500 cycles. These packages included four low I/O CSPs, leadless and grid CSPs, one high I/O CSP, and a TSOP. The high I/O CSP was underfilled.

The test vehicle with identification 21-1 and 21-A was the board with the double sided packages. The microvia side (21-A) was reflowed first, and the standard side (21-1) was reflowed next. Therefore, the microvia joints were exposed to two reflows, but the standard side only once. One failure of a leadless package was observed between 100 and 300 cycles (21-A, daisy chain 1) on the microvia side. This package was also the only package which exactly overlapped the package on the double side with 90 degree rotation.

The first failure location was at a two cross-over corners. The criticality of solder disturbance at the crossing corners will be verified in the full production test vehicle build. Early joint failure is qualitatively in agreement with other investigators' findings (Sharp, ECTC '98). The number of cycles-to-failure was reduced to almost half for double sided assemblies with the mirrored package assemblies. The number of cycles-to-failure was increased as double sided package assemblies moved away from the mirror position.

The other failures of 21-1, daisy chain 6-1 and 6-2, and 19-1, daisy chain 5, were considered to be defects related either to the package or the PWB or both. One was due to the use of preproduction package (not the same as the one to be used for full production), and the other due to package and process anomalies. Via misregistration and solder mask coverage on the pads could have been the potential cause of joint failure on the PWB. Recall that these test vehicles were from the trial run, the chief purpose of which was to understand the critical issues with of PWB fabrication, process optimization, and daisy chain verification.

**Table 2 Daisy Chain Resistances of Assembled CSPs
at Various Number of Cycles at Condition A (-30/100°C)**

PWB ID	Package ID-Daisy	Cycle 0	Cycle 100	Cycle 300	Cycle 400	Cycle 500	Cycle 600
22-1A	1	2.8	2.8	Open	Open	Open	Open
22-1A	2	4.6	4.7	5.4	4.8	4.8	4.8
22-1A	3	9.3	9.2	9.5	9.3	9.4	9.5
22-1A	4	6.8	6.6	7	6.8	6.8	6.6
22-1A	5	5.8	5.7	6	6.2	5.7	5.9
22-1A	6-1	20.9	20.7	21.2	21.1	21.2	21.1
22-1A	6-2	23.7	23.5	23.8	23.7	23.6	23.7
22-1	1	2.3	2.3	2.6	2.7	2.6	2.4
22-1	2	4	4.1	4.1	4.3	4.2	4.1
22-1	3	9.3	9.3	9.4	9.4	9.2	9.2
22-1	4	5.9	6.3	5.9	6.2	5.8	5.8
22-1	5	6.1	6.2	6.9	6.6	6.9	6.3
22-1	6-1	Open	Open	Open	Open	Open	Open
22-1	6-2	28.6	Open	Open	Open	Open	Open
29-1	1	2.8	2.8	2.9	3	2.9	2.8
29-1	2	4.6	4.8	5.1	4.9	4.9	4.8
29-1	3	9.7	9.6	9.6	9.7	9.7	9.6
29-1	4	6.7	6.8	7	7	6.8	7
29-1	5	5.6	5.7	5.7	5.6	5.7	5.7
29-1	6-1	21.6	21.6	21.7	21.8	21	21.6
29-1	6-2	24.5	24.6	24.6	24.7	23.5	24.8
3-1	1	2.8	2.8	2.9	2.9	2.9	2.6
3-1	2	4.7	4.7	4.9	5.1	4.8	4.7
3-1	3	9.5	9.4	9.6	9.7	9.6	9.8
3-1	4	6.8	6.7	7	7	7.1	6.9
3-1	5	5.7	5.6	6	5.9	5.9	5.6
3-1	6-1	19.2	19.1	19.4	19.2	19.8	19.1
3-1	6-2	22.8	22.6	22.9	22.9	22.7	22.6
19-1	1	2.8	2.7	2.9	3.2	2.9	STOP
19-1	2	4.8	4.7	5	4.6	4.7	STOP
19-1	3	10	10	10.1	10.3	10.6	STOP
19-1	4	6.8	6.8	6.9	6.7	6.5	STOP
19-1	5	7.8	Open	Open	Open	Open	STOP
19-1	6-1	23.3	23.3	23.3	23.7	24.7	STOP
19-1	6-2	24.8	24.7	24.8	25	23.3	STOP

Conclusions

- Ball shear forces were differ for different CSPs. Shear force distributions for the same package type differ for two suppliers.
- Difference in shear forces depended on many variables including interface area, metallurgy, solder mask defined or non defined, and failure mechanisms.

- Slight improvement in shear force or narrower distribution was observed after packages exposure at 100°C for 100 hr. Improvement may be due to stress relaxation by annealing.
- Mixed technology assembly may not easily permit the use of optimum solder volume to achieve the highest reliability. This is probably true for an SM mixture of fine pitch and leadless packages and become challenging with the addition of no-lead (leadless) and grid CSPs. CSPs, reliability may be degraded in a mixed technology assembly, especially for no-lead CSPs.
- Low lead small wafer level CSP packages exhibited poor quality. Three out of 62 failed after assembly and another failed after 100 condition A cycles.
- The trial test vehicles assembled for process optimization (non-optimum condition) were subjected to cycling (A condition). The solder joints on double sided assembly were the first to fail among many leadless and grid CSPs. This agrees with other investigators' test results which shown deleterious effects of double sided assemblies on solder joint reliability.
- Traditionally, solder joint failure was considered to be the weakest link in the microelectronics attachment reliability. This might not be true for CSPs with an innovative design.
- Cycling temperature range in some cases might be severe and introduce failure mechanisms that are not representative of field applications. Complimentary tests and failure analyses need to be performed to build confidence in assembly reliability results.
- Understanding the overall philosophy of testing to meet system requirements as well as detecting new failure mechanisms associated with the miniaturized CSPs is the key to collecting meaningful test results.

References

1. Ghaffarian, R. "CSP/BGA Board Level Reliability," The NEPCON West '99 Proceedings, March 1-5, '98

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