

# CSP CONSORTIA ACTIVITIES: PROGRAM OBJECTIVES AND STATUS

E.J. Simeus, S. Stegura, R. Smedley- Raytheon Systems Company  
I. Sterian, C. Quan, A. Chen, R. Mohabir- Celestica Inc.  
M. Chan, T. Buschor, D. Norton , Harris  
R. Ghaffarian, J. K. Bonner- JPL/CalTech  
Reza.Ghaffarian@JPL.NASA.Gov, (818) 354-2059

## ABSTRACT

The JPL-led MicrotypeBGA consortium of enterprises representing government agencies and private companies have joined together to pool in-kind resources for developing the quality and reliability of **Chip Scale Packages (CSPs)** for a variety of projects. This paper will present specifically the experience of four consortium team members on technology implementation challenges, design and build of standard and **microvia boards**, assembly of two types of test vehicles, and the most current package **isothermal aging** and **thermal cycling** test results. In addition, it includes experience of a team member that join consortium with a test vehicle unique to their needs. The paper will provide an overview and independent articles provided by team members.

## CSP IMPLEMENTATION CHALLENGES:

### CSP Definition

Emerging Chip Scale Packages (CSPs) are competing with bare die assemblies and are becoming the package of the choice for size reduction applications. These packages provide the benefits of small size and performance of the bare die or flip chip, with the advantage of standard die packages. CSPs are defined as packages that are up to 1.2 or 1.5 times larger than the perimeter or the area of the die. Many manufacturers now refer to CSP as the package that is a miniaturized version of its previous generation.

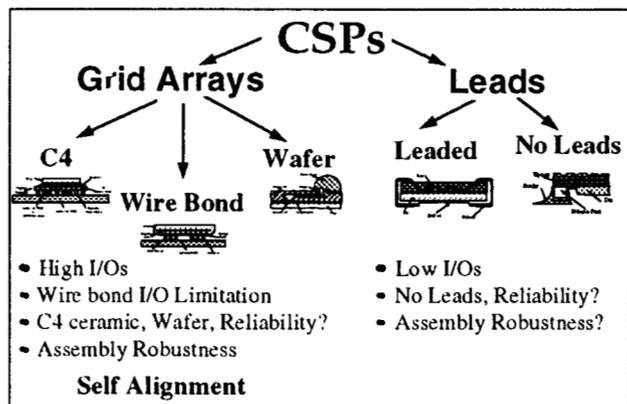


Figure 1: Two Chip Scale Package Categories

Two concepts of CSPs are shown in Figure 1. The concepts presented include: (1) Grid CSPs with wire bond and C4 (Control Collapse Chip Connection) technology (rigid or flex interposers), and wafer level molding assembly and redistribution.

(2) Leaded and no leads for low I/O applications.

## CSP Investigation

In the process of building the consortium CSP test vehicles many challenges were identified regarding various aspects of technology implementation. Details for design, build, assembly are discussed in Part A: to Part C with the following subjects:

- Part A: Design of consortia test vehicle #1 and Printed Circuit (PWB) fabrication
- Part B: Design, Assembly and Environmental Evaluation of CSP consortia Test Vehicle #2
- Part C: Assembly of CSP Consortia Test Vehicle #1 and #2 and Other Issues

The overall program objectives and technology aspects are discussed below. Key challenges are summarized as follows:

**Maturity and availability** — Availability of CSPs for use and attachment reliability evaluation was the most challenging issue at the start of program in early 1997. There were numerous publications on a wide range of CSPs, but most packages were at their early development stage and lacked package reliability data. Assembly reliability data were rare. Most packages were available in prototype forms and this did not guarantee the package similarity to production version or even their availability in future. More than six month delay on package delivery date was the norm. Four packages dropped from program and one delayed almost a year. Although many suppliers promoted their package and reliability, they were not willing to submit their packages for an independent evaluation possibly because of lack of their confidence.

**Lack of Design Guideline Standards**—Guidelines and standards on various elements of CSPs were not available. For our design, guidelines developed by the package suppliers were used when available. Otherwise,

available knowledge and engineering judgment were considered.

**PWB Build** — The standard PWB design could be used for low I/O CSPs. Build up (microvia) board technology is required for higher I/O CSPs in real application with active die. For daisy chain package, it is possible to design high I/O on standard board. Board design guidelines are needed, especially for the build up (microvia) configuration.

**Applications** — There were a number of packages from low I/O (<50) to higher I/Os (about 500) for characterization. It became apparent that for the near future, 1-3 years, the dominant packages would be those with less than 50 I/Os. Specific application requirements could utilize packages with much higher I/Os. Mixture of conventional SM packages, direct chip attachment, BGAs, and CSPs on one board is another expected design and assembly challenge. The mixed technology being considered for the next test vehicle under the CSP consortium.

#### CSP Test Vehicle Design

The consortium agreed to concentrate on the following aspects of CSP technology after numerous workshops, meetings, and weekly teleconferences.

**Package** — Numerous packages from leaded and leadless to grid CSPs were selected for evaluation. I/Os ranged from 12 to 540 to meet the short and longer term applications. The 540 I/O package was dropped by manufacturer prior to the trial test vehicle assembly. Therefore the maximum I/O package now is 275 I/O. See Table or section A???

**PWB Materials and Build** — Both FR-4 and BT (Bismaleimide Triazine) materials were available in the resin copper coated form for evaluation. High temperature FR-4 and thermound also evaluated. The boards were two sided, standard and microvia. With our design, direct reliability comparison between two board technology as well as double side processing is possible. In design of daisy chains, it became apparent that the standard PWB technology could not be used for routing the majority of packages.

**Daisy Chain** — Packages had different pitches, solder ball volumes and compositions, and daisy chain patterns. In most cases, these patterns were irregular and much time and effort was required for design. This was especially cumbersome for packages with higher I/Os and many daisy chain mazes development.

**Surface finish** — At least four types of surface finishes were considered. OSP, HASL, Au/Ni (two thickness),

and immersion silver. The majority were OSP finish. Three types of solder pastes evaluated: no clean, water soluble and RMA.

**Underfill** — Packages with underfill requirements were evaluated both with and without underfill to better understand the reliability consequence of not using underfill.

**Double Side Assembly** — PWBs were double sided and several boards with double sided packages were assembled to compare reliability of single sided to double sided test vehicles as well as standard versus microvia technology.

**Solder Volume** — Three stencil thickness were evaluated, high, standard, and low. The two extreme thickness were 4 and 7 mils with different aperture design depending on the pad size. The standard which was used for the majority of test vehicles had 6 mil thickness.

**Test Vehicle Feature** — The test vehicle was 4.5 by 4.5 inches and divided into independent regions. For single side assembly, most packages could be cut for failure analysis without affecting the daisy chains of other packages. All packages were daisy chained and they had up to two internal chain patterns.

**Environmental testing** — At least three conditions were considered; -30 to 100°C (A cycle) and -55 to 125°C, to link our data to those generated for the Ball Grid Arrays. The A cycle profile is show in Figure 2. Also, thermal cycling will be performed between 0 and 100°C to meet the needs of commercial team members. In addition, mechanical vibration and shock will be performed and theoretical modeling will be carried out as needed.

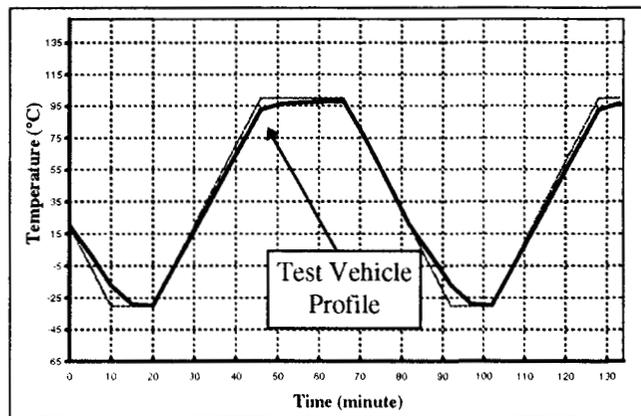


Figure 2 Thermal Profile for Condition A Thermal Cycling (-30°C to 100°C)

## CSPs ISOTHERMAL AGING CHARACTERISTICS

### Shear Test Before and After Aging

To understand potential failure mechanisms of the packages, particularly solder ball attachment, the grid type packages were subjected to environmental exposure. The CSP packages were subjected to visual inspection and scanning electron microscopy (SEM) to characterize their joint quality, solder ball metallurgy, and elemental compositions.

They were then subjected to ball shear testing, before thermal aging. After initial testing, these CSPs were subjected to isothermal aging at two different temperatures for two intervals. The exposed packages were then subjected to inspection, SEM, and shear

testing, and the levels of damages documented. Preliminary results were presented elsewhere<sup>[1]</sup>.

Figure 3 shows the most current shear test result before and after isothermal aging with the cumulative percentage versus shear forces for four grid CSPs. The median ranking  $[(i-0.3)/(n+0.4)]$  was used to calculate cumulative percentages. It is interesting to note the significant difference in shear forces for different packages. Distributions for the same packages, but different suppliers are also different.

Table 1 give a summary of the fifty percentile shear forces and their respective shear stresses. Shear forces after 1,000 hours of isothermal aging at 100°C are also presented. Most CSPs showed increase in shear with aging at 100°C.

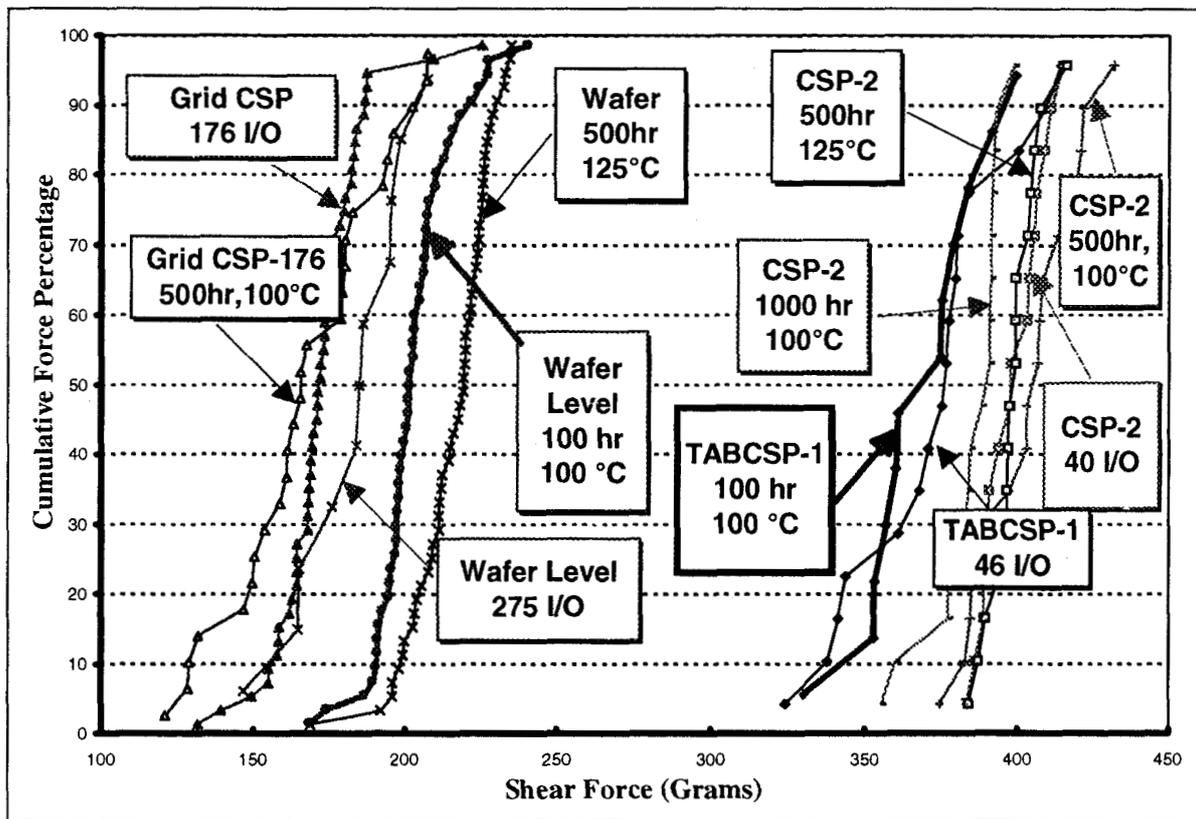


Figure 3 Cumulative Percentage Versus shear Force in Gram for Various Grid CSPs

Table 1 Shear Force and Stress for Various CSPs

Package Type	I/O	Shear Diameter (mm)	Shear Force (gram) at 50%	Shear Stress (Kgram/mm <sup>2</sup> )	Shear Force 1000 Hours at 100°C
TABCSP-1	46	0.320	376	4.7	405
TABCSP-2	40	0.30	397	5.7	390
Wafer CSP	275	0.250	185	3.8	221
GridCSP	176	0.170	172	7.6	N/A

### Tin Leach of Aged Solder

Figure 4 shows SEM photo micrograph a CSP package after 500 hours of isothermal aging at 100°C (no steam). The diffused out particles surrounding the sheared ball were Tin detected by EDX elemental analyses. This was a unique case. The same package and all other packages exposed to 100°C or to 125°C did not show tin leakage. Tin leakage of a grid CSP was observed by another investigator (S. Greathouse, SMI '96, p. 213) when it was subjected to steam aging at 121°C, 2 Atm, for 168 hours. It stated that this is a common phenomenon to plastic package with tight pitch or bumps that are exposed to condense water on the surface. For conventional packages, brushing has been used to eliminate tin traces, but this is can not be done adequately for grid BGAs and CSPs without damaging the solder ball themselves.

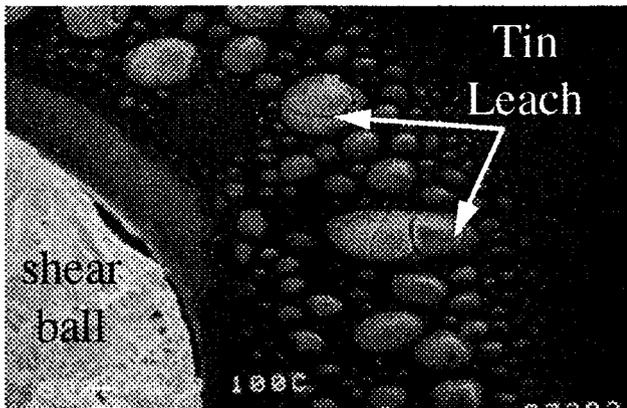


Figure 4 Tin Leach After 500 Hours of Isothermal Aging at 100°C

No steam in our experiment. The reason for tin leaching with no steam to dissolve tin from the eutectic ball followed by its deposition is not well understood. If it is assumed that leaching occurs in the presence of moisture and volatile, then the package state of moisture condition, underlying ball materials, and residue from process of attachment are key potential causes.

Except for a few number of CSPs with low moisture sensitivity (level 1), the majority of plastic CSPs are at level 3 and higher. This means that most of these packages after elapse of week exposure on floor must be baked. Baking could cause the initial tin leaching. Subsequent assembly and exposure to high temperature and moisture could further increase the amount of leaching. The effect on performance is not well established yet.

### ASSEMBLY

Consortium assembled seven trial test vehicles of #1 and 30 test vehicles of #2. Ball grid arrays are known to be robust in manufacturing, but there are disagreement on

the acceptable offsets for CSPs. No defects were observed when thirty test vehicle of #2, each with 4 grid CSPs with 46 I/Os, were assembled.

### Quality of Solder Joints

Figure 5 shows SEM of solder joint for a TAB CSP and a low I/O wafer level (8 I/O) package on board. It was difficult to inspect visually or by SEM the quality of these joints because the low package height. Three of these wafer packages showed poor quality joint with signs of cracking. Package poor quality was the reason for existing of microcracks after assembly. Subsequently, this package was not included for the test vehicle #1 assembly.

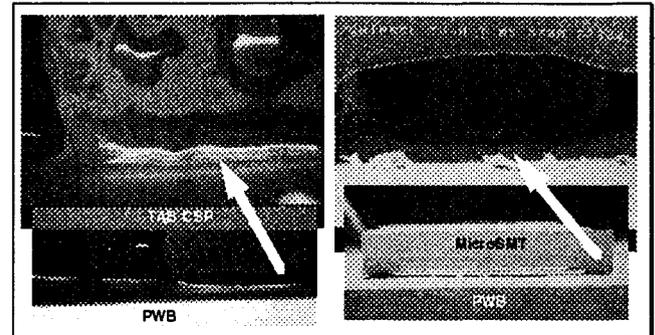


Figure 5 Good Quality of a Grid CSP and Poor Quality of Low I/O Wafer Level Solder Joint

### Grid CSP Shear Forces

One of the trial test assembly #2 was subjected to shear test to determine the shear strength of solder joint. Low I/O wafer level assemblies could be sheared by shear tester, but not the assembled TABCSP. Therefore four of these were subjected to pull testing to failure. Test results are as follows:

- The low I/O wafer level packages failed at 312, 249, 175, and 158 grams., These values are low and is of concern. Die penetrant indicated existence of cracks prior to shear.
- TABCSP-1 assemblies detached by pulling from the package. No solder joint failure was observed. Failure were from the ball interface traces in the package. The tensile forces for four were 28, 25, 22, and 13 lb. These values are in the range of 280 to 600 grams for a ball tensile load. Ball shear forces for the same package were in the range of 320 to 400 grams (see Figure 3).

### THERMAL CYCLING TEST RESULTS

Seven trial test vehicles #1 were assembled to optimize assembly process and profile. The lowest stencil thickness, 4 mil, was used to determine the worst condition especially the effect of solder starving

condition on leadless package. The stencil thickness of 6 mil is recommended for assembly of leadless packages. One test vehicle was assembled double sided. Five of PWBs had OSP surface finish and two HASL. All including PWBs with HASL finish were successfully assembled. As expected, working with HASL was much more difficult than OSP.

The five trial test vehicles with the OSP finishes were subjected to thermal cycling in the range of -30 to 100°C (A condition). Both PWB and assembly conditions were not optimum for the trial test. Therefore thermal cycling results might indicate potential areas that process must be optimized for the production test vehicle assembly. Results are not valid for reliability and failure statistic analyses.

Resistances were measured manually before and at different thermal cycling intervals to check for electrical opens (solder joint failure). Automatic monitoring was impossible since connections to the ground plane were missed during file translation. This was corrected. For full production assemblies, these daisy chains will be monitored continuously.

Table 2 include resistances before and at different thermal cycles. Assemblies removed from chamber and check at room temperature for resistance. Resistances are in  $\Omega$  (ohms). Resistance are different for different daisy chain pattern, but are approximately the same for the same package on various test vehicle assemblies. It is interesting to note that even for non-optimum conditions, the majority of solder joint assemblies survived to 500 cycles. These packages included four low I/O CSPs, leadless and grid CSP, one high I/O CSP, and a TSOP. The high I/O CSP was underfilled.

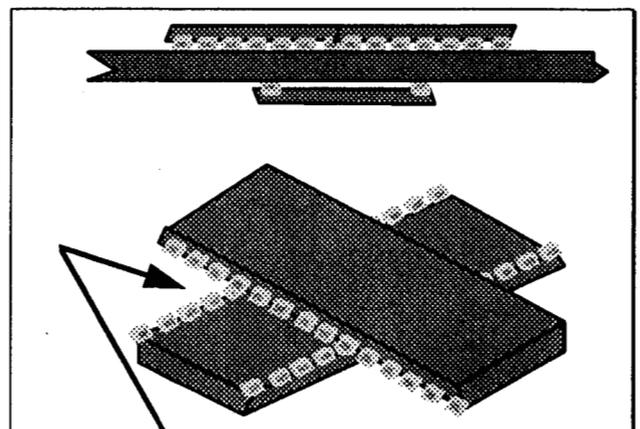
The test vehicle with identification 21-1 and 21-A was the board with double sided packages. The microvia side (21-A) was reflowed first and the standard side (21-1) reflowed next. Therefore, the microvia joints exposed to two reflows and the standard side only once. One failure of leadless package was observed between 100 and 300 cycles (21-A, daisy chain 1) on microvia side. This package was also the only package which exactly overlapped the package on the double side with 90 degree rotation.

Figure 3 shows schematically the first failure location solder joint termination. It was at a two cross-over corner. Criticality of solder disturbance at the crossing corners will be verified in full production test vehicle build. Early joint failure is qualitatively in agreement with other investigators' findings. The number of cycles to failure reduced to almost half for double side assemblies with the mirrored package assemblies. Cycles

to failures were increased as the two side package assemblies moved away from the mirror position.

**Table 2 Daisy Chain Resistance of Assembled CSPs at Various Number of A Cycle Condition (-30/100°C)**

PWB ID	Package ID-Daisy	Cycle 0	Cycle 100	Cycle 300	Cycle 400	Cycle 500	Cycle 600
22-1A	1	2.8	2.8	Open	Open	Open	Open
22-1A	2	4.6	4.7	5.4	4.8	4.8	4.8
22-1A	3	9.3	9.2	9.5	9.3	9.4	9.5
22-1A	4	6.8	6.6	7	6.8	6.8	6.6
22-1A	5	5.8	5.7	6	6.2	5.7	5.9
22-1A	6-1	20.9	20.7	21.2	21.1	21.2	21.1
22-1A	6-2	23.7	23.5	23.8	23.7	23.6	23.7
22-1	1	2.3	2.3	2.6	2.7	2.6	2.4
22-1	2	4	4.1	4.1	4.3	4.2	4.1
22-1	3	9.3	9.3	9.4	9.4	9.2	9.2
22-1	4	5.9	6.3	5.9	6.2	5.8	5.8
22-1	5	6.1	6.2	6.9	6.6	6.9	6.3
22-1	6-1	Open	Open	Open	Open	Open	Open
22-1	6-2	28.6	Open	Open	Open	Open	Open
29-1	1	2.8	2.8	2.9	3	2.9	2.8
29-1	2	4.6	4.8	5.1	4.9	4.9	4.8
29-1	3	9.7	9.6	9.6	9.7	9.7	9.6
29-1	4	6.7	6.8	7	7	6.8	7
29-1	5	5.6	5.7	5.7	5.6	5.7	5.7
29-1	6-1	21.6	21.6	21.7	21.8	21	21.6
29-1	6-2	24.5	24.6	24.6	24.7	23.5	24.8
3-1	1	2.8	2.8	2.9	2.9	2.9	2.6
3-1	2	4.7	4.7	4.9	5.1	4.8	4.7
3-1	3	9.5	9.4	9.6	9.7	9.6	9.8
3-1	4	6.8	6.7	7	7	7.1	6.9
3-1	5	5.7	5.6	6	5.9	5.9	5.6
3-1	6-1	19.2	19.1	19.4	19.2	19.8	19.1
3-1	6-2	22.8	22.6	22.9	22.9	22.7	22.6
19-1	1	2.8	2.7	2.9	3.2	2.9	STOP
19-1	2	4.8	4.7	5	4.6	4.7	STOP
19-1	3	10	10	10.1	10.3	10.6	STOP
19-1	4	6.8	6.8	6.9	6.7	6.5	STOP
19-1	5	7.8	Open	Open	Open	Open	STOP
19-1	6-1	23.3	23.3	23.3	23.7	24.7	STOP
19-1	6-2	24.8	24.7	24.8	25	23.3	STOP



**Figure 6 The First Failure Solder Joint in Double Sided Assembly**

The other failure of 21-1, daisy chain 6-1 and 6-2, and 19-1, daisy chain 5, were considered to be defect related either to package or PWB or combination. One due to use of reproduction package (not the same as the one to

be used for full production) and the other due to package and process anomaly. Via misregistration and solder mask coverage on pad could have been the potential cause of joint failure by PWB. Note again, that these test vehicles were from the trial run for the purpose of understanding issues with PWB fabrication, process optimization, and daisy chain verification.

**Table 3 Number Joint Failure for Low I/O Wafer Level Assemblies before and up to 500 thermal cycles (-30 to 100 °C)**

Package	Total of TV	U1 Site	U2 Site
As Assembled	31	0	3
0 Cycles	10	0	1
100 Cycles	10	0	2
200 Cycles	10	0	2
300 Cycles	10	0	2+ 1 Resistance 13.1Ω
400 Cycles	10	0	2+ 1 Resistance 13.7Ω
500 Cycles	10	0	2+ 1 Resistance 16.4Ω

### CSP TECHNOLOGY RANKING METRICS

Currently, there are nearly 50 CSPs within different categories. Each type has its strong features and characteristics. The CSPs attributes cannot easily be quantified since they are influenced by many factors including supplier approach and user requirements. Qualitatively comparison of different technology is possible. Table 4 shows such comparison. As benchmark, it include the flip chip technology.

CSPs were ranked for their features including cost, yield, availability, reliability, and testability. The highest ranking is for CSPs with flex interposer and the lowest for wafer distribution. CSPs with leads/no leads were ranked the same as the rigid interposer packages. Reworkability and reliability of leads/no lead with a very low I/O was considered to be better whereas CSPs with rigid interposers better accommodate higher I/O requirement.

**Table 4 Different CSP Technology Ranking Compare to Flip Chip**

Package Types-> Merits	Wafer	Lead/ No Lead	Interposer		Wafer Redist	Flip Chip
			Flex	Rigid		
Cost Device	3	3	9	9	3	3
Cost PWB/PWA	9	9	9	9	1	1
Yield	9	9	9	9	3	1
Compatability	9	9	9	9	3	1
Availability/Multiple Sources	1	9	9	9	3	1
Flexibility	1	3	9	9	3	3
Testability	9	9	9	9	3	3
Reworkability	3	9	9	3	1	1
Reliability	3	9	9	3	1	1
I/O	4<>64	10<>64	10<>400		100<>2000	100<>2000
	<b>47</b>	<b>69</b>	<b>81</b>	<b>69</b>	<b>21</b>	<b>15</b>

**9 = Good, 3 = Fair, 1 = Poor**

### CONCLUSIONS

- Ball shear forces varied for different CSPs and were in the range of 100-400 gram/ball. Shear values depend on many parameters including interface area, metallurgy, and failure mechanisms.
- Improvement in shear forces or narrower distributions were observed after package exposure at

100°C for up to 1000 hours. Improvement may be due to stress relaxation by annealing.

- Assembly handling could be an issue especially for small CSPs. Wafer package with low I/O (8 Leads) required low shear failure forces (about 20 gram/lead), which were much lower than 100-400 gram/ball for grid CSPs. The small I/O CSPs might

require underfill to improve handling, reliability, and resistance to shock and vibration.

- Tin leaching due to moisture absorption/desorption is another concern for CSPs.
- BGAs and grid CSPs align themselves during reflow process and therefore are more robust than fine pitch leaded packages. Acceptable placement offset values depend on many parameters including package type, size, ball material, and weight of package.
- Mixed technology assembly may not permit the use of optimum solder volume for highest reliability. This is true for an SM mixture of fine pitch and leadless and become challenging with addition of no-lead and grid CSPs. CSPs reliability may be degraded in a mixed technology assembly, especially for no-lead CSPs.
- Low lead small wafer level CSP package had poor quality. Three out of 62 failed after assembly and one additional after 100 A cycles.
- The trial test vehicles assembled for process optimization (non-optimum condition) were subjected to A cycle condition. The solder joint on double side assembly was first to fail among many leadless and grid CSPs. This is in agreement with other investigators' test results who had shown deleterious effects of double sided assemblies on solder joint reliability.
- Visual inspection has been common to characterize solder quality and reject nonconformance to specification for Aerospace applications. Inspection

for acceptance is still a challenge for BGAs. The challenges are further magnified for the inspection of grid CSPs with smaller features in addition to hidden solder joints. Stringent process controls are acceptable for commercial, but additional joint integrity verifications is needed for high reliability applications. Joint integrity verification is critical for space missions.

- Understanding the overall philosophy of testing to meet system requirements as well as detecting new failure mechanisms associated with the miniaturized CSPs is key to collecting meaningful test results.

## REFERENCES

1. Ghaffarian, R. "Chip Scale Package Joint Integrity Under Isothermal Aging," Proceedings of Chip Scale International, San Jose, May 6-7, 1998

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