

Session: Robotic and Semirobotic Ground Vehicle Technology (or37)

Session Chairs: Grant R. Gerhart and Ben Abbott

Monolithic Microprocessor and RF Transceiver for Low-Power Mobile Applications

Erik A. McShane, University of Illinois, Chicago, IL Krishna Shenai, University of Illinois, Chicago, IL Leon Alkalai, Jet Propulsion Laboratory, Pasadena, CA Eric Holmberg, Jet Propulsion Laboratory, Pasadena, CA
Elizabeth Kolawa, Jet Propulsion Laboratory, Pasadena, CA

In recent years the demand has surged for low-power and small form-factor wireless communications devices. Coupled with the migration of desktop computing to mobile computing, a new market is emerging for portable products that combine wireless communications and high-performance computing.

The evolution of semiconductor device technology toward the deep submicron regime is enabling the development of CMOS RF communications circuits which are amenable to monolithic integration with existing mixed-signal processes.

A 1.2-micron bulk CMOS process has been used to develop a monolithic architecture consisting of an 8-bit RISC microprocessor, a 256-byte on-chip SRAM memory, power management, and a 400-MHz RF transceiver. The logic portion of the IC operates at 50 MHz, and the RF transceiver achieves a data transmission rate of 16 kb/sec with a 100 kHz bandwidth. On-chip power regulation eliminates supply glitches due to logic switching, and power management is provided to minimize the standby power dissipation of idle components. This IC demonstrates the potential of CMOS to deliver a low-power architecture for computing and wireless communication.