A Single-chip Programmable Digital CMOS Imager with Enhanced Low light Detection Capability

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INTRODUCTION

Low-power, low-cost, miniature and integrated digital imaging systems are expected to be widely used in consumer electronics in the near future. While CMOS technology has been responsible for the phenomenal growth in consumer electronics, micro-processors, memory, audio systems, and radio-frequency circuits (e.g. cellular phones), till recently, the video technology remained outside this mainstream. Over the years, the incumbent technology in electronic imaging for consumer, commercial, and scientific applications has been charge coupled devices (CCD). The predominance of CCD in electronic imaging was due to its superior sensitivity, dynamic range, uniformity, low noise, and small pixel size. However in order to achieve high (0.999999) charge transfer efficiency, CCDs require specialized silicon processing that is not compatible with CMOS technology. Furthermore, CCDs are high capacitance devices, requiring multiple non-standard and high voltage clocks and biases, while providing only serial output (no random access is provided). High device capacitance, large clock swing, need for DC-DC converters, and inability to integrate control & processing electronics on the imager chip make the CCD-based imaging system bulky and power-hungry (camcorder CCD power dissipation is around 10 W). Incompatibility with CMOS technology is a major barrier to realizing low-power, low-cost, digital, integrated system-on-a-chip using CCDs.

Despite several efforts in the decade of eighties and earlier, CMOS imaging performance lagged behind that of CCD. Availability of near or sub-micron CMOS technology, maturity of CMOS processing, in conjunction with the advent new low noise active pixel sensor (APS) concepts have altered the situation in the decade of the nineties [1, 2, 3]. APS approach enables high quality CMOS imagers with performance rivaling those of CCDs, drawing video technology into the mainstream of CMOS system-on-a-chip development.

The primary advantages of CMOS APS are low-cost, low-power (100-1000x lower than CCDs), simple digital interface, random access, simplicity of operation (single CMOS compatible power supply), high speed (>1000 frames per sec.), miniaturization (10-100x smaller) through system integration, and smartness by incorporating on-chip signal processing circuits. In this paper, we report a single-chip, large format, high quality fully digital, fully programmable, ultra-low power electronic imager and a single-chip digital camera. We report the design, operation, and performance of the single-chip imager, with special emphasis on simultaneously improving imager linearity at low-light levels and achieving low noise and zero image lag.

IMAGER ARCHITECTURE & OPERATION

Unlike a CCD imager that requires multiple chips for imager realization, multiple high and non-standard voltages for operation, CMOS imaging technology enables a single-chip digital imager realization. The integration of timing & control functions, programming functions, reference generation functions, analog-to-digital converters (ADC), and the analog signal chain along with the CMOS pixel array enables the realization of a single-chip, programmable low-power, digital imager. Figure 1 shows the schematic of the CMOS APS digital imager, consisting of the above mentioned blocks. A set of input registers enables the user to select between different modes of operation such as the analog or the digital mode, video or the snap-shot imaging mode, and program in the exposure time, electronic pan & zoom setting, speed & bias control.

While system integration and miniaturization is natural to a CMOS imager, a great deal of attention needs to be paid in order to achieve ultra-low power for portable applications and to maintain high imaging speed and high imaging performance. Figure 2 shows the unit cell of an active pixel imager along with the column signal chain that feeds into the ADC or the analog signal chain. The pixel consists of a reverse-biased p-n junction where the photons are converted into photoelectrons and are collected, a reset transistor (M_{rst}) that is used to periodically reset the cell, a source-follower input transistor (M_{SF}) and a select transistor (M_{SEL}) that is common to that row of pixels. Unlike a CCD, an APS pixel produces a voltage output over the column bus, and hence provides random-access. The load (M_{load}) of the source-follower is located at the bottom of the column. Each pixel source follower feeds into two capacitors (C_S and C_R) located at the bottom of the column. These capacitors are used to temporarily store the signals from each pixel before they are processed. The signal chain also consists of two transistors (M_{drop} and M_{short}) in each column that allows highly linear response at low-light-levels and low noise operation. RST and ROW are row-decoded signals, and HTS, SHS and SHR are global clocks that are common to all columns.

The imager operates in a column-parallel (row-wise) fashion, with each pixel being read out differentially. Following the exposure of a row of pixels for an integration time (T_{int}), it is selected by pulsing ROW high as shown in figure 3. The potential at the sense node (PD) reflects the amount of photoelectrons accumulated during the integration time. It is buffered out over the column bus, and sampled and held on C_S by momentarily pulsing SHS high. This is followed by resetting the pixel by momentarily pulsing RST high causing the sense node potential rise up to a reference level, which is approximately Vdd-VT, where VT is the threshold voltage of the reset transistor.

The reset potential is also buffered out and sampled on the other capacitor, C_R. The voltage difference between the potentials (V_R and V_S respectively) on the two capacitors is the measure of the amount of light collected by the pixel. The HTS pulse allows pixel operation with highly linear response, and will be explained in the next section. Differential readout of the pixel enables cancellation of pixel-to-pixel offsets due to MOSFET threshold (V_T) mismatches, as well as reduction of flicker noise.

The exposure time in digital still imaging or in slow-scan imaging can vary over a large scale - from 100 μsec. to very long (> 10 sec.). In order to set the exposure time and the frame-read time independently, and to achieve variable exposure time, the imager is designed to operate with a two-pointer addressing scheme, a pointer being a decoded row address. The first pointer causes a row of pixels to begin integration, and the second pointer causes it to end integration, and execute a row-read sequence. Thus, the exposure time (T_{int}) is determined by the temporal spacing of the integration and read pointers for the same row. Since integration and readout of different rows are interleaved, a typical row phase consists of four sub-phases: i) initiation of integration for row m, ii) pixel readout for row m-k, iii) parallel digitization of the row of pixels, and iv) digital data out, as shown in figure 3. Since, an imager frame is essentially a concatenation of a series of row phases, it is important to keep the same duration of all the row phases, so that there is no image distortion. However, there are situations where one or more of the sub-phases are not necessary. For instance, in still imaging mode, for times $t < T_{int}$ after the exposure has begun, sub-phases ii through iv are absent, since none of the rows will have begun readout. In order to preserve equality of row phase duration, none of the sub-phases are ever eliminated, but no control signals are generated during those times. The total frame time (t_{fr}) is given by:

$$t_{fr} = N \cdot t_{row} = N \cdot \left(t_{pix} + t_{ADC} + N \cdot t_{read}\right);$$ where N is the imager format.

Frame time is primarily determined by the output clocking speed (t_{read}), with t_{pix} and t_{ADC} being a small fraction of t_{row}, especially if the digital imager is read out in serial mode. Overlapping of phases (pipelined operation) allows higher operating speed, only at the cost of unacceptable degradation of image quality due to digital noise. The two-pointer addressing scheme is also essential for simultaneously supporting both video and still-imaging modes. Without two pointers, interleaving of integration and readout phases for separate rows (as shown in figure 3) will not be possible, preventing video mode of operation [4].

PIXEL NOISE AND LINEARITY

Each pixel is reset in a "soft-reset" mode. Soft-reset refers to resetting with both drain and gate of the n-channel reset transistor kept at the same potential, causing the sense node (PD) to be reset using sub-threshold MOSFET current. The reset level is approximately a threshold voltage below Vdd, since that is where the strong inversion conduction stops. To maximize the pixel dynamic range, both analog and digital power supplies are set to their maximum allowable values, leading naturally to the soft-reset mode of operation. set FET. One of the important advantages of soft-reset is the reduction in reset noise. Reset noise arises from the random variations in the reset level from one frame to another, the random variations being the outcome of the stochastic nature of the transport process of the electrons through the reset transistor. It has been shown that with soft reset, the reset noise in electrons is given by [5]: $\sigma^2 = \frac{1}{2\beta \cdot q^2}\left[1 - e^{-2\beta \Delta n} + 2\beta e^{-2\beta \Delta n}\sigma_0{}^2\right]$ (1)

where $\beta = q^2/mkTC_{PD}$, q is the electronic charge, m is the non-ideality factor, C_{PD} is the sense node capacitance, k is the Boltzmann constant, and T is the temperature in degrees Kelvin. σ_o^2 is the variance at the onset of the reset process, and Δn is the average amount of electrons added to the sense node. For a photodiode type APS under soft-reset, $\sigma_o^2=0$ for a given frame, and the variance is approximately expressed as:

$$(q \cdot \sigma)^2 = \begin{cases} \Delta n \; ; & \text{for} \quad \beta \cdot \Delta n << 1 \\ mkTC_{PD}/2 \; ; & \text{for} \quad \beta \cdot \Delta n >> 1 \end{cases} \tag{2}$$

Equation 2 indicates that when the imager is in dark, the variance is essentially the shot noise in the number of electrons transferred to the sense node, and can be extremely small (~ 10 e^-). On the other hand, even when a large number of electrons are transferred to the node, the reset noise is a factor of 2 lower than the conventional kTC reset noise. The reduction in reset noise is due to a feedback inherent in the reset mechanism. For an exponential current flow over the barrier, instantaneous current flow is decreased sooner there is an increase in the node potential. As a result, the distribution of electrons narrows, causing sub-kTC reset noise. An additional advantage of soft reset is high Power Supply Rejection Ratio (PSRR). This results from the absence of a reverse current, preventing power supply fluctuations to interact with the sense node.

However, lowering of noise is achieved only at the expense higher image lag and low-light-level non-linearity. For still imaging mode or for high-speed video imaging modes, the pixels remain in idle state (T_{idle}) for a considerable amount of time, as shown in figure 4, that shows the pixel timing diagram without the HTS pulse. The

second reset pulse in the timing diagram marks the beginning of the actual integration time by clearing the sense node of the charges accumulated during the idle phase, and the third reset pulse marks the end. If the reset level is kept high during idle, as shown by the dotted line, the imager response exhibits significant non-linearity in form of a response "dead-zone". The dead-zone arises out of the soft-reset. Under soft-reset the sense node keeps charging up slowly in a logarithmic fashion, so that during the idle phase, the sense node charges up to a level that is higher than what is nominally achieved when the reset clock is momentarily pulsed. As a result, when the imager is operated with pixels reset for a long time in idle state, the subsequent reset pulses have no effect on the sense node, since the current flow is only in one direction. Thus, a differential pixel measurement yields a near zero value.

Holding the reset level low during idling does not solve the problem either. The actual reset level in soft-reset depends upon the initial potential on the node. This can be clearly seen from the SPICE simulation results shown in figure 5. For simulation purposes, both T_{int} and T_{idle} is kept the same, except that the photoelectrons collected during T_{idle} is 5 times that during T_{int}. The simulation clearly shows that the reset levels at the end of idle and integration phases are different, the difference itself being dependent on the signal strengths. In other words, the reset pulse at the beginning of T_{int} does not remove all photoelectrons from the sense node, the excess electrons being responsible for response non-linearity at low-light-levels, as shown in figure 5b.

The response non-linearity at low-light-levels can be removed by using HTS-reset scheme shown in figure 3. Nominally, HTS is low, so that M_{short} shown in figure 2, connects the drains of the pixel transistors to Vdd. When HTS goes high (with a row selected), M_{short} is shut-off, and the diode-connected M_{drop} conducts current causing the drain of the reset transistor to drop by more than VT, allowing the pixel to be reset completely. When HTS goes low again, with RST held high, the pixel resets in a soft-reset mode. However, the soft-reset occurs with the same initial condition due to the use of HTS pulse, as shown in figure 6. Hence, unlike soft-reset, the reset level using HTS reset scheme always reaches the same potential, eliminating non-linear response at low-light-levels. Thus, HTS reset scheme allows imager operation with high linearity, zero-image lag, and low-noise. The performance enhancements are achieved by using column-based circuits only, leaving the pixel circuit unchanged. As a result, HTS scheme does not adversely affect any other imaging metric such as the quantum efficiency, dark current, responsivity, etc.

The flicker noise contribution from the unit cell source follower is minimal to the use of temporal difference sampling. The white noise in the source follower transistors is shaped by the sample-and-hold operation to produce

an output-referred noise given approximately by: $\left\langle v_n^2 \right\rangle \approx \frac{kT}{C_S}(1+\beta)$, where β is the transconductance ratio between the load and the input transistor. The charge-to-voltage conversion gain given by q/C_{PD} is high (~ 5-10 $\mu V/e^-$), resulting in small input-referred noise in electrons given by: $(q \cdot \sigma)^2 \approx kT \cdot C_{PD} \frac{C_{PD}}{C_S}(1+\beta)$. By choosing a large-enough value for C_S (~ 2-3 pF), noise contribution of the source-follower is rendered insignificant. An important observation with regard to noise performance is that in CMOS APS noise behavior is governed by the pixel noise [6]. Since the pixel sample time is relatively constant, APS imager noise, unlike CCD, is relatively independent of data rate, enabling high-speed, low-noise applications.

ANALOG-TO-DIGITAL CONVERTER DESIGN

Low-power imaging considerations require digitization of photogenerated signals as close to the pixels as possible in order to eliminate the high power consuming driver amplifiers. Moreover, ADC power needs to be minimized. However, even at moderate frame rates of 30 FPS, conversion rate of a single ADC for a 1024^2 sized imager is 100 MHz. High speed high resolution ADC design is not only difficult, but is also very power hungry. Both these considerations dictate the use of a column-parallel architecture, where the analog output from each column is connected to its own ADC. The parallelism in this architecture enables minimization of power without sacrificing data rates, by allowing individual ADCs to operate at much lower speeds - N times slower than what would be required if a single ADC were to be used, where N is the number of columns. Thus, only a 100 kHz conversion rate is required for a 1024^2 imager operating at video rate. It has been shown that a column-parallel ADC approach leads to a significantly lower power implementation, since, unlike in digital circuits, power dissipation in analog circuits increases super-linearly with the operating frequency [7]. Therefore, the combined power dissipation in N ADC circuits is considerably less than that in a single ADC circuit running N times faster.

Another major disadvantage of a single ADC architecture for digital imager implementation arises from the need for a high speed clock. Commonly available data acquisition systems limit the master clock rate, and hence the imager output data to around 10-20 MHz. Digitization with a single ADC requires a much higher speed internal clock, leading to severe clock phase synchronization problems, as well as problems of increased substrate noise.

On the other hand, a major concern with column-parallel architecture is the layout challenges due to severe

space restriction in column direction (limited to pixel pitch), although vertical dimension can extend to a few mm. The space constraint usually precludes the use of active circuits (e.g. opamps) for ADC implementation. Moreover, any mismatch between adjacent ADCs shows up as annoying bar patterns on the image, also known as the fixed pattern noise (FPN).

For ultra-low-power digitization, an all-capacitor successive-approximation ADC algorithm is implemented. The implementation is not only compatible layout constraints of column-parallel architecture, but features built-in offset correction providing low FPN, and allow operation with <200 μW/Mconv./sec. The 10-bit column-ADC circuit schematic along with the bit cell [B(i)] circuit is shown in figure 7. The ADC consists of two branches of capacitors on which the reset and signal levels from the pixels are sampled. The capacitor (C_S) on the signal side is comprised of N_b (equal to ADC resolution) binary-scaled capacitors (C_i). If C_{MSB} is the largest sized capacitor used, each capacitor in the bank follows the relation: $C_i = \frac{C_{MSB}}{2^i} \Rightarrow C_S = 2 \cdot C_{MSB}$. Each bit cell consists of a latch that controls the potential at the bottom-plate of the capacitor connected to it. Pulsing the bottom plate of a capacitor C_i to V_{ref} raises the voltage on C_S by the capacitive divider ratio or equal to $V_{ref}/2^i$. The capacitors are buffered by two source-followers before being fed to the comparator circuit.

The ADC operates as follows. First, the reset (V_R) and signal (V_S) values are sampled with respect to ground respectively on C_R and C_S. The ADC operation consists of successively adding binary-scaled voltages to the signal side (V_S) to allow it to catch up to V_R, and registering the digital codes necessary to generate the voltage pattern. If at the i-th cycle, voltage on C_S is greater than that on C_R, the i-th bit cell output is latched to a logic level "1" by pulsing set, and the voltage on C_S is returned to its original value. Otherwise, the bit cell logic latches the output to logic "0". The comparator output is also stored in the appropriate data latch at the bottom of the column. Digitization is completed after N_b repetitions, with bit cells representing digital code. Since the ADC digitizes the difference of V_R and V_S, it is inherently immune pixel threshold mismatches.

In order to cancel the offset generated by the buffer source followers and the comparator, a calibration phase is used. During this phase, the same signal is sampled on both capacitors, and then digitized. Ideally the digital code is "0". Thus, the ADC output in the calibration phase is the digital representation of the offset between the two branches. The ADC outputs are stored in offset latches at the bottom of the column. By subtracting the offset code from the pixel ADC code during data readout, offset free digitization is realized, and FPN is minimized.

The bias and reference generation block consists of 6 multiplying DACs (MDACs) to provide the required reference voltages and bias currents. A 5-bit DAC is sufficient, since accurate reference is not needed, as long as they are low noise, and have sufficient drive to allow fast-settling and slew. The MDACs are realized by selectively summing outputs of binary-scaled current mirrors, the current source selection being carried out by appropriate MDAC input bits.

ADC noise consists mostly of switching noise associated with C_{bi}. Summing noise contributions from each switched bit cell in quadrature, the total voltage noise is estimated to be: $\frac{\pi kT}{4C}$, which is negligible (~ 15 μV), for C ~ 8 pF. Typically, the imager response is limited by the ADC quantization noise.

CONVERSION ACCURACY

In order achieve high precision digitization, very careful power and ground line routing is necessary in order to prevent d.c. resistive drop by connecting the power and ground lines in a star configuration. The DAC circuits also need large drivers in order to ensure that signals on the capacitive nodes settle when prebar signal is activated. Due to column parallel implementation, total capacitance of all ADC's is large, being around 4 nF. A low impedance DAC is needed to settle signals on an effective 4 nF capacitance in short time intervals of around 300 nsec. Although the effective capacitance reduces with every cycle, the amount of charge to be transferred is code dependent. Hence each bit duration is kept the same, with the intent of handling the worst case settling requirements.

The remaining ADC inaccuracy is determined by the relative errors in capacitor matching, and by voltage-dependent comparator offset. The latter can be made insignificant by buffering the comparator input, that prevents capacitive "kickback". The error in capacitor matching is reduced by careful layout and through the use of large sized capacitors. Minimum capacitance is 14 fF, making the largest capacitance C=7.16 pF. To improve matching, each capacitor is implemented by concatenating a set of base capacitors. This method reduces relative errors both by randomization of errors in base capacitor, and by minimization of fringe field. Moreover, the three largest capacitors are also organized in a common-centroid geometry, further randomizing the mismatch errors. Taking relative error into account, cell capacitance is: $\tilde{C}_i = \frac{C}{2^{i-1}} \cdot (1 + \varepsilon_i)$, where ε_i is the relative error, and $\varepsilon_1 = 0$. The maximum error occurs for the code transition [011...1] to [100...0]. Assuming sufficient randomization, the worst case differential

non-linearity (DNL) for an r.m.s. error $\langle \varepsilon_i \rangle = \varepsilon$ is given by: $\varepsilon_{best} = \left[\left\{ \frac{C^2}{\sum_1^N \tilde{C}_i^2} \right\} - \left\{ \frac{\sum_2^N \tilde{C}_i^2}{\sum_1^N \tilde{C}_i^2} \right\} \right]^{0.5} \cdot V_{ref} \approx \frac{3 \cdot \varepsilon^2 \cdot V_{ref}}{4}$. To achieve DNL < 0.5 LSB, maximum tolerable relative error is only $\sqrt{\frac{1}{3 \cdot 2^{N_b - 2}}}$ or as high as 3.6 %. Although it is not possible to achieve perfect randomization, the error margin is large enough for 10-bit digitization with DNL < 0.5 LSB.

POWER DISSIPATION

Low average power is achieved by temporarily turning off tail currents in circuit blocks with no activity. Although instantaneous power in the V_{ref} generating DAC, as well as the pixel amplifiers is high, current flow occurs only for a fraction (~ 1-10 %) of the row time. The digital control logic power is negligible, since except for column scan, the entire state machine runs off a slow row clock. Average power in different blocks of the imager, operated in analog and digital modes, are given below.

$$P_{adc} = \frac{t_{adc}}{t_{row}} \cdot N \cdot V_{ref}^2 \cdot \frac{1}{t_{bi}} \Sigma C_{bi} = 2 \cdot FPS \cdot N^2 \cdot Nb \cdot C \cdot V_{ref}^2; \quad C_{bi} = \frac{C \cdot (2C - C_i)}{2C}$$

$$P_{pix} = FPS \cdot N^2 \cdot t_{pix} \cdot I_{pix} \cdot V_{dd}; \quad P_{dac} = 2 \cdot FPS \cdot N^2 \cdot C \cdot V_{ref} \cdot V_{dd};$$

$$P_{dig\text{-}rdo} = 0.5 \cdot FPS \cdot N^2 \cdot C \cdot V_{dd}^2; \quad P_{anlg\text{-}rdo} = I_{out} \cdot V_{dd}$$

Figure 8 is a log-log plot of the total analog and digital power dissipation, along with power dissipation in DAC, pixel, and ADC. The plot reveals that the average power dissipation is higher (more than 4 times at video rates) when the imager is operated in analog than in digital mode, even after including ADC power. This is due to the fact that most of power dissipation occurs during readout, and for high data rates analog power varies as the square of the data rate (due to accurate settling requirements), while digital power rises only linearly. Measured power dissipation from the imager chip closely follows the relationship presented above, as shown by the open dots in figure 8, deviating from the theoretical curve only at very low frame rates. This deviation is caused by insufficient DAC resolution, preventing generation of small currents.

IMAGER PERFORMANCE

Figure 9 shows the die photograph of the 512x512 digital camera-on-a-chip. The chip occupies an area of 10 mm x 15 mm, with the imager area being 6 mm x 6 mm, and the ADC area is 6 mm x 5 mm. The pixel pitch is 12

μm, with drawn optical fill-factor of 38%. The ADC array takes up a large amount of area since accurate capacitance matching is desired. The chip provides digital video data (8 Mpix/s) at an ultra-low power of 6 mW, while producing high quality image. Figure 10 is a reproduction of the image of a portion of a dollar bill captured with the digital imager. Unlike other CMOS imagers, no image artifacts such as column-to-column fixed pattern noise (FPN) are visible, and the pixel response non-uniformity is less than 1 % (typical of a camcorder-type imager). The column-to-column FPN, measured from a flat field, is less than 1.0 LSB across the array at low-light levels.

By employing HTS reset scheme, good optical response with excellent low-light-level response linearity is achieved. Figure 11 shows the measured response linearity using the HTS scheme and without it. As expected, soft-resetting the pixel without the HTS pulse causes significant response non-linearity. On the other hand, using the HTS reset technique, a 30 dB improvement in low-light-level linearity is achieved. Imager response is also non-linear for large signals, due to the non-linear nature of the p-n junction capacitance. However, this does not pose any significant problems, since gamma correction (a non-linear transform) is routinely used in imaging applications. In order to measure image lag, the imager was exposed with a bright flash in one frame followed by a dark frame. No residual signal was measured in the dark frame, indicating imaging with zero image lag. The peak quantum efficiency at 550 nm is 42 %, indicating good optical collection. The measured ADC is highly linear, with most of the non-linearity shows up at major transition codes, but is less than ± 0.5 LSB over the entire input range. The CMOS imager performance, summarized in table 1, is commensurate with high quality imaging requirements.

A digital micro-miniature camera was implemented using the CMOS one chip digital imager. The total volume of the camera including optics is 3 cm^3, and is comprised mostly of optics. The optics size can be further reduced, allowing "wrist-watch" type cameras. The micro-miniature programmable camera consists of a miniature lens glued on to a single digital imager chip that interfaces with only 4 wires (Vdd, Gnd, clock, and serial Din/Dout). The camera requires only one power supply to operate and dissipates less than 10 mW of power driving a standard RS232 interface.

CONCLUSIONS

In summary, we have presented for the design and performance of a large format, ultra-low power, single-chip CMOS digital imager capable of reproducing high quality images. A new HTS reset scheme allows imager operation high linearity at low-light-levels and without any observable image lag, and extends the operational

dynamic range. We have presented the design considerations and trade-offs for reproduction of high quality images in CMOS technology, while minimizing power and increasing data rates. The 512x512 digital imager requires a single power supply (3.3 V), consumes only 6 mW of power at video rates, is capable of operation with read noise < 40 e^- in photodiode mode. The one-chip digital imager will find ready use in a number of commercial portable applications where low-power and the availability of a simple, digital interface is of great importance.

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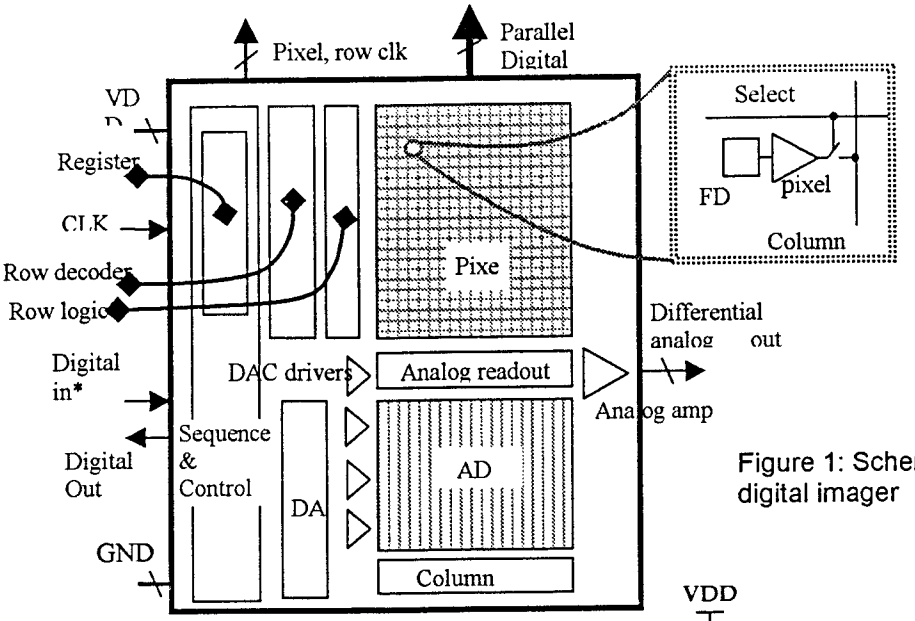

Figure 1: Schematic of the one-chip digital imager

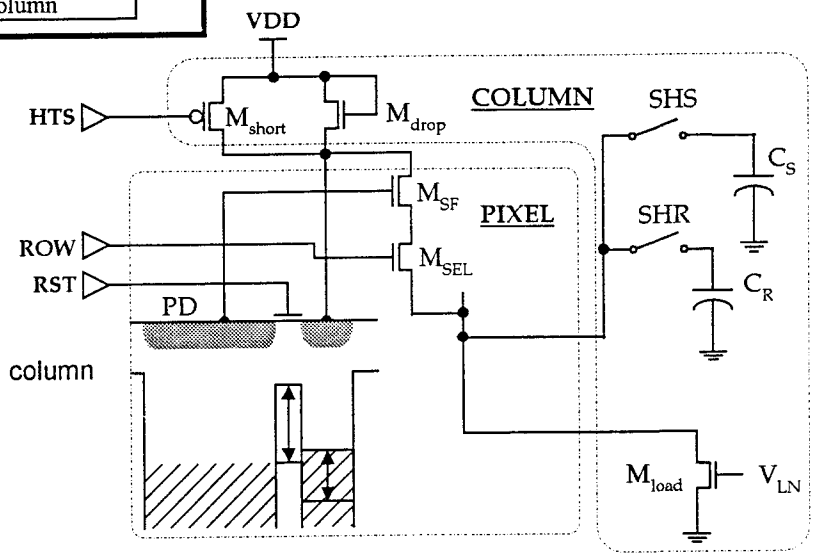

Figure 2: Schematic of the pixel and column signal chain of the digital imager

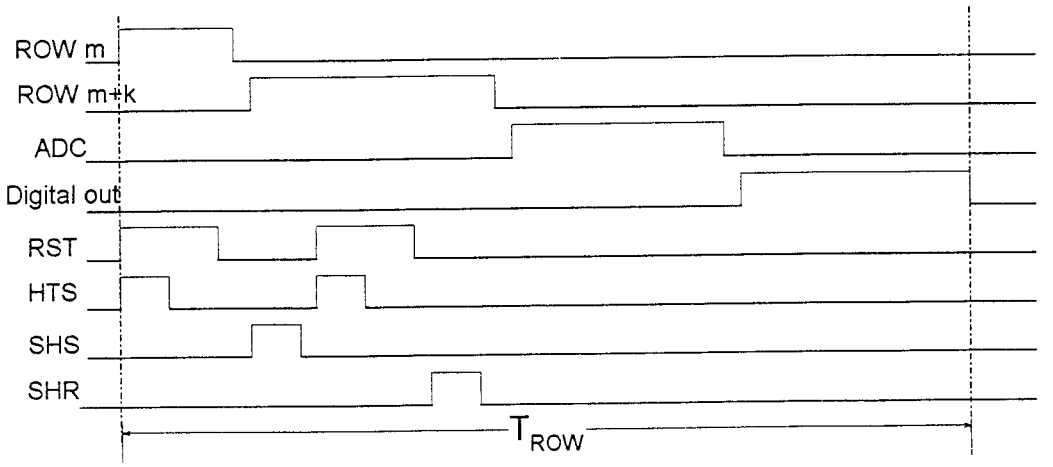

Figure 3: Pixel and row timing diagram

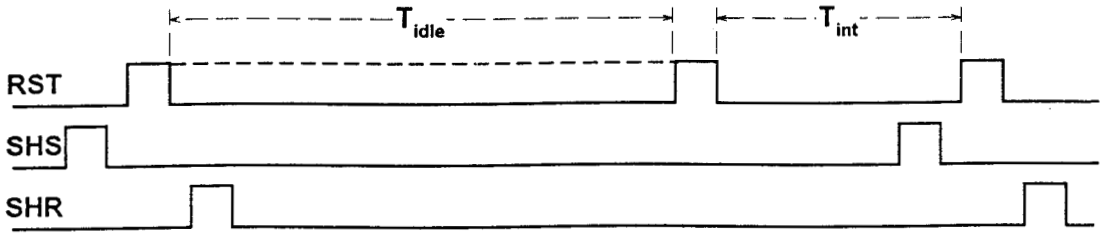

Figure 4: Timing diagram for still or high-speed video mode imaging (No HTS pulse is used)

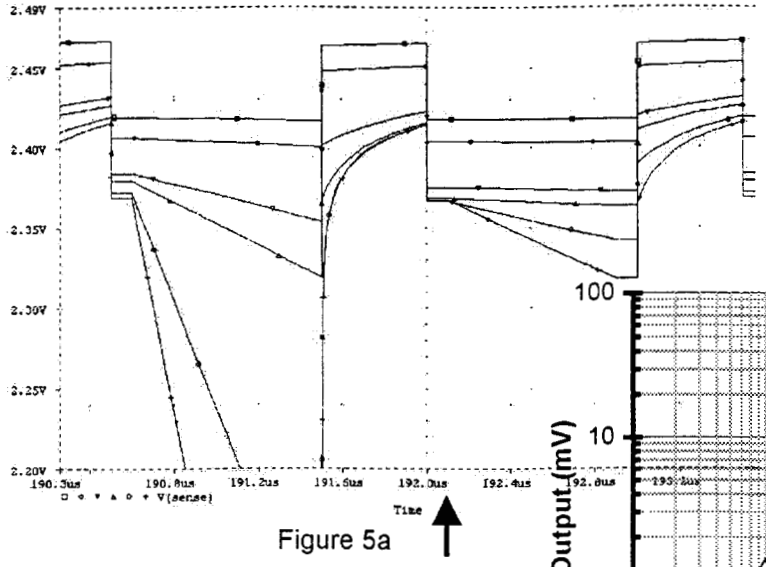

Figure 5a

Potential at the sense node:
Signal 50 - 10,000 e⁻ for T_{int}

Figure 5b

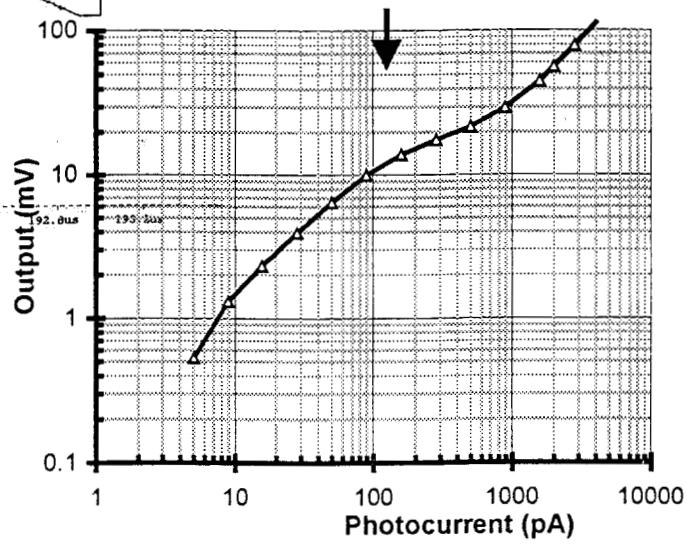

Figure 5: Simulated sense node potentials & Simulated pixel response at low-light-levels

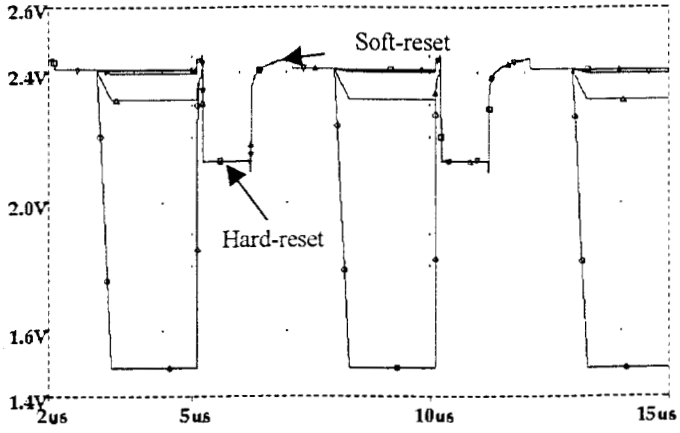

Figure 6: Simulated sense node potentials for HTS reset scheme

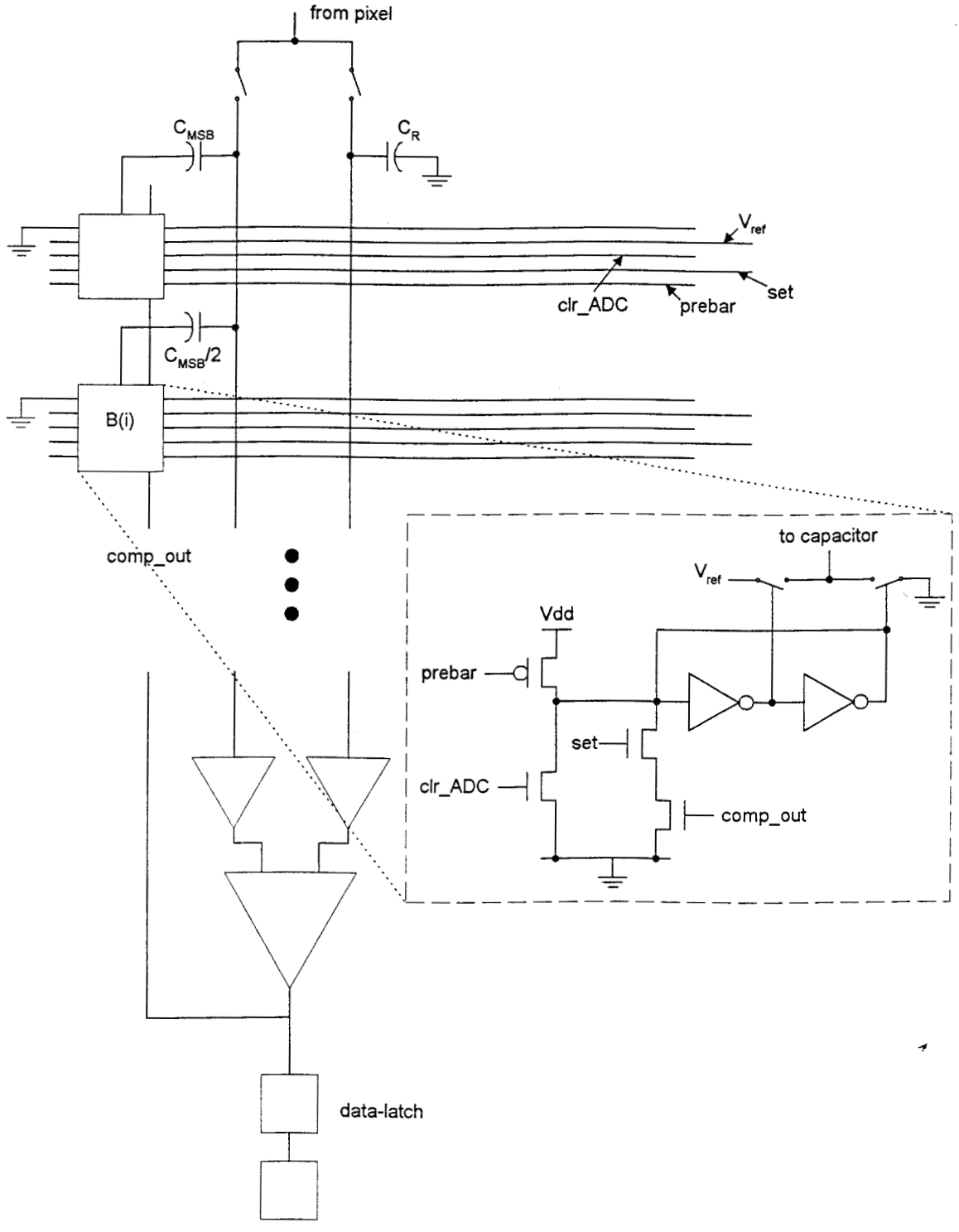

Figure 7: All-capacitor successive-approximation ADC implementation with the bit-cell circuit

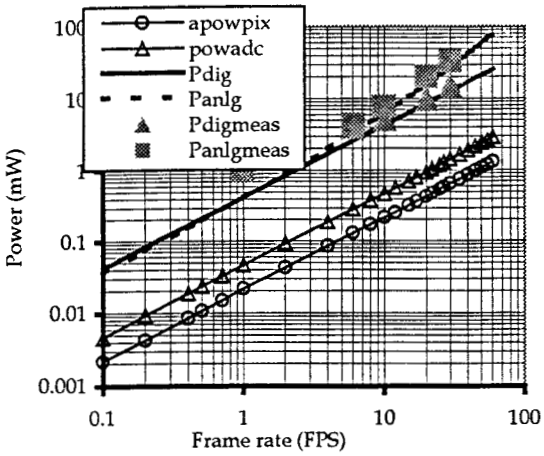

Figure 8: Power dissipation and its components as function of frame rate

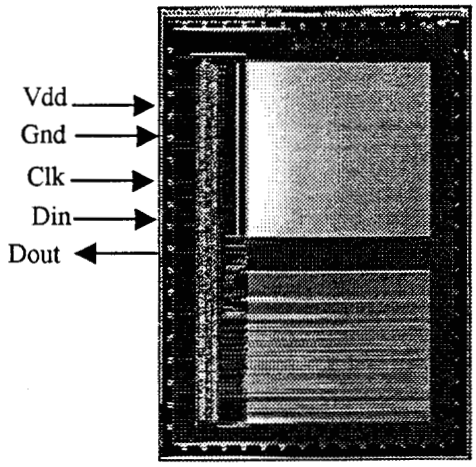

Figure 9: Microphotograph of the one-chip digital imager

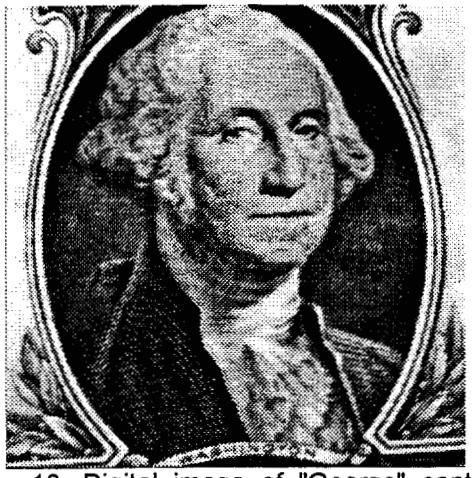

Figure 10: Digital image of "George" captured with the one-chip imager

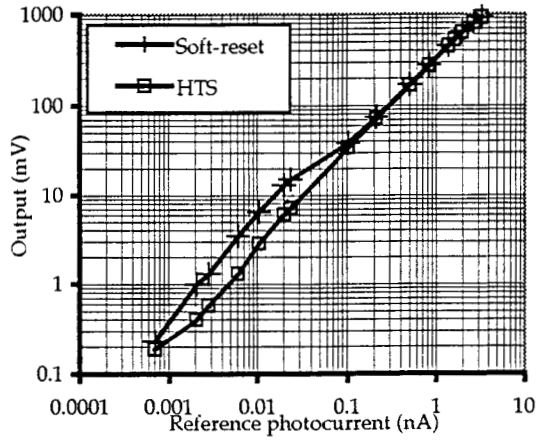

Figure 11: Measured response for soft and HTS reset

Table 1: APS camera-on-a-chip performance summary

Imager characteristics	Values	Comments
Technology	CMOS, 0.5 μm	
Outputs	Analog & digital	
Format	512 x 512	
Pixel size	12 μm x 12 μm	
Responsivity	4 μV/photon	@ 550 nm
Quantum efficiency	42 %	For the total pixel
Dark current	500 pA/cm^2 for PD	
Noise	40 e$^-$ for PD	
Full well	250,000 e$^-$ for PD	
ADC resolution	10 bits	9.3 effective bits
ADC DNL max.	0.46 LSB	
Power	6 mW	@ 8 Mpix/sec.
Power supply	3.3V	Single power supply
Timing and control	on-chip	